System description

ABB Procontic T300

Multiprocessor Control System

Hardware

Order number
GATS 1315 01 R2002 part 2
replaces
Publication number
D AT 1612 88 E

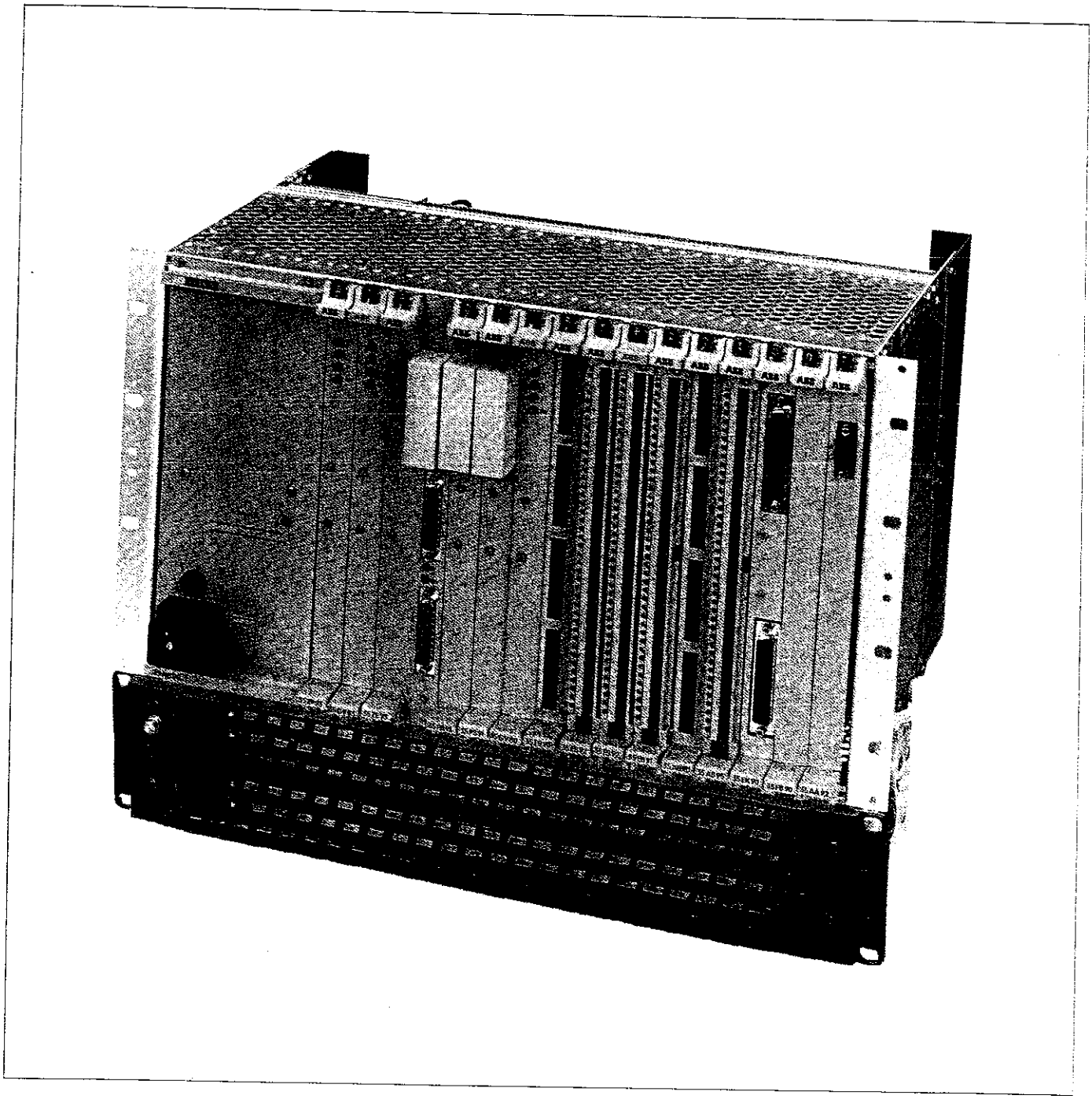

ABB Schalt- und Steuerungstechnik GmbH

ASEA BROWN BOVERI

Regulations

Regulations Concerning the Setting up of Installations

Apart from the basic "Regulations for the Setting up of Power Units" VDE* 0100 and for "The Rating of Creepage Paths and Air Gaps" VDE 0110 the regulations "The Equipment of Power Units with Electrical Components" VDE 0160 in connection with VDE 0660, part 500, have to be taken into due consideration. Further attention has to be paid to VDE 0113 in case of the control of working and processing machines. If operating elements are to be arranged near shock-hazard parts with protection against electrical shock, VDE 0106, part 100, is relevant.

The user has to ensure that the units as well as the associated components have to be installed according to these regulations. Respectively valid safety regulations, e.g. regulation for the prevention of accidents and the law concerning technical working material, are valid for machines and units connected as well.

ABB Procontic units have been built according to VDE regulation 0160. The protection against direct touching as demanded by chapter 5.5.1 of this VDE regulation has to be satisfied by the user, e.g. at installing of switch cabinet.

ABB Procontic units have been designed for operation according to insulation class A of VDE 0110. If considerable polution is expected during operations, the units have to be installed in housings of the respective kind of protection.

* VDE stands for "Association of German Electrical Engineers".

Note: Please observe the national regulations for the installation of electrical equipments, which are valid in your country.

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1 General part

This is a description of the system concept, the system structure, the bus signals, the electrical characteristics and the ambient conditions of the ABB Procontic T300.

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1.1 System overview

1.1.1 System concept

ABB Procontic T300 is a **universal, extendable component system** for building up control systems for the entire automation technology. The basis for this is a modular, standardized hard-/software system, which completely exhausts the technological possibilities by using microprocessors and complex periphery switch circuits, on the one hand, and, on the other hand, gives the user sufficient choice in the selection of the system blocks.

The field of application of the ABB Procontic T300 system stretches from processing operating information (programmable controller) via the control of actuators and variable-speed drives through to numerical path creation for separate and linked machines. Control systems for complex applications can be built up with a combination of standard blocks due to the modular structure.

Moreover, the modular concept allows a longer lifetime of the system, since control systems can be constantly kept up-to-date functionally and technologically according to the state of development by retrofits, new function units and new, digital components.

A prerequisite for a modular control system is the division of the control task into greatly independent partial tasks. The possibility of communication between these function units must be given to combine various partial tasks on several function units into an entire control. Since ABB Procontic T300 is designed as a block system, the communication requires clearly defined hardware interfaces but also more importantly software interfaces as a prerequisite, as well as methods to coordinate the function software of the separate blocks, so that the separate units can fulfill the given control task altogether.

The description and determination of the hardware interfaces to the module limits led to the development of a standardized bus system (multiprocessor-based control bus = MPST), which is **independent of the microprocessor** and which enables an effective data exchange between the modules within the system.

The determination of the software includes the definition of a hierarchal software structure as well as of an order method based on this in order to be able to coordinate the sequence of the software of the individual function units. Moreover, interfaces for the exchange of information between the function units were defined, whereby two levels of the exchange of information were considered. On the one hand, interfaces for the exchange of subscriber data were created and, on the other hand, interfaces for the exchange of information concerning the development of the order method.

1.1.2 Development of the MPST system

The MPST system was developed by the MPST working committee, which was composed of institutes of further education, control manufacturers and machine manufacturers. The development was promoted within the framework of the 3rd data processing program of the BMFT, under the responsibility of the nuclear research company in Karlsruhe (Kernforschungsgesellschaft Karlsruhe).

The activities of the MPST working committee were transferred to the newly founded MPST committee (registered association) (MPST-Kreis e.V.) after the general completion of the development of the MPST concept.

The interface determination in the MPST has appeared as a standard (DIN 66264, to be requested from Beuth Verlag GmbH, Berlin 30), whereby part 1 of this standard describes the parallel bus and part 2 the information interfaces.

1.2 System structure

1.2.1 Hardware structure

The hardware structure of the modular MPST system, ABB Procontic T300 is based on the MPST parallel bus with data, address and control lines. A subscriber is a function unit which is realized by one or several printed boards. A characteristic of the subscriber is that it can be addressed via the MPST parallel bus.

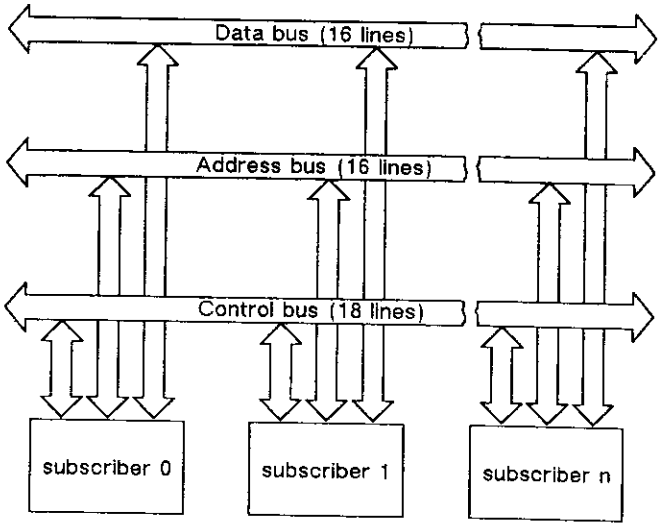


Fig.1-1 Hardware structure

The system distinguishes between active and passive subscribers.

Active subscribers

Active subscribers can address other subscribers, like processor units, for example, and exchange data with them. The active subscriber carries out read and write operations with other subscribers independently.

Example:Processor card with PLC software

Passive subscribers

A passive subscriber, like an in- or output unit, for example, is addressed by an active subscriber.

Example: Memory card 35 PS 91

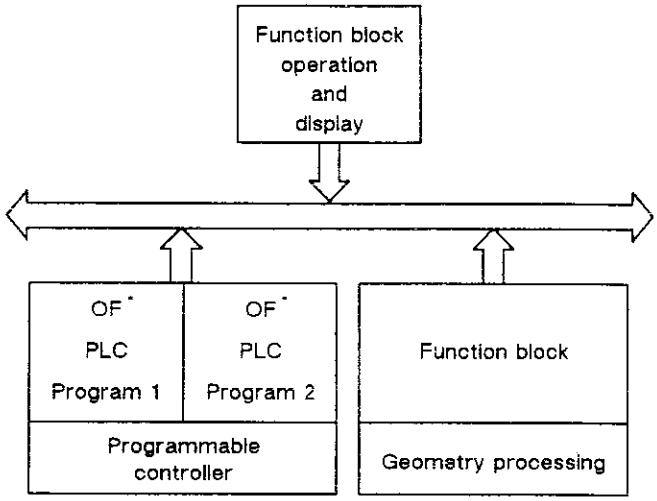
1.2.2 Software structure

If you examine a given control task with functional points in mind, function blocks can first be defined, which undertake a fixed task in the entire system.

Machine control example: Operating and display block, control blocks, diagnosis block, etc.

The distinction between the separate function blocks is chosen, so that **the amount of data** as well as **the frequency** of the exchange of data with other function blocks is kept to a minimum, if possible. Each function block is divided into functions in the next stage (geometry block example: interpolation, position control, override, etc.). The functions can be composed again of general program blocks by using a program library (arithmetic routines, algorithms, code conversion routines, string operations, etc.).

A uniform software interface was created for the communication between the function blocks based on this hierarchal software structure. From the subscriber's point of view, the smallest activity within a function block, which can be recalled, is the orderable function (OF; geometry block example: reference point movement). This function can be compared with the "task" concept. Assigning orders to an OF occurs by filling in control blocks. Since the structure of these control blocks was standardized for the ABB Procontic T300 system, all functions can be addressed and executed in the system by means of a uniform access algorithm.



*OF = orderable function

Fig. 1-2 Software structure

The orderable functions (OF) address single functions (SF), to which a fixed task is assigned. The single functions cannot be directly addressed externally, however, and are the smallest units of the software structure.

1.3 Description of the MPST parallel bus

1.3.1 Requirements

The MPST parallel bus is a **multiprocessor bus system**. The interests of the automation technology were in the forefront during its development. The structure of modern semiconductor components, especially that of microprocessors, was also taken into account.

A **direct exchange of data** between bus subscribers should be possible, whereby the amounts of data to be transmitted are composed of single bits, single words and data blocks (list transfers). Events with high priority require a fast alarm transmission.

The bus supervision is carried out via the central control unit (CCU). The CCU has as a subscriber the address 0 for the bus transfers. It also creates the control clock, CC.

A bus structure designed for a microprocessor is required in order to minimize the interface expenditure for the function unit to be connected to the bus. A free selection of the processor must be guaranteed with a view to the further development. The mixed operation of **8 bit processors** and **16 bit processors** is supported by the bus system.

Special weight was given to the possibility of a cheap serial production as well as on the field of application in an inclement environment. The control electronics is generally concentrated in a unit cabinet for controls for machining or processing devices. A bus length of 2 m is therefore sufficient.

1.3.2 Bus signals

The individual signals are described in the following.

Address bus

The 16 address lines are bi-directional bus lines. The address bit A00 is the address bit with the lowest value. The smallest bit, which can be addressed, is a byte. The driver outputs for the addresses have a high resistance, when they are not active, and the bus signals are logically one (2.3 V ... 5.25 V).

The subscriber is directly addressed by the address setting in the subscriber.

Data bus

The 16 data lines are bi-directional bus lines. The data bit D00 is the data bit with the lowest value. The driver outputs for the data have a high resistance, when they are not active, and the bus signals are logically one (2.3 V ... 5.25 V).

Control bus

The meaning of the signals is explained in the following.

WO:
The signal WO (word transfer) codes the format of the data on the data bus (word/byte).

A00	WO	Address
0	0	even numbered byte address. Data in the lower byte (D00 to D07) are valid
1	0	odd numbered byte address. The data in the higher byte (D08 to D15) are valid
0	1	word address. The data in the lower and higher bytes (D00 to D15) are valid
1	1	not defined

$\overline{W}$:
Writes a word or byte under a given address. The entire address bus is valid.

$\overline{R}$:
Reads a word or byte from the address given on the address bus. The entire address bus is valid.

$\overline{R}$	$\overline{W}$	Meaning
0	0	invalid
0	1	Read
1	0	Write
1	1	only valid with ACK during interrupt operation

$\overline{I/O}$:
The signal $\overline{I/O}$ (Input/Output memory area) codes the address area of 64 x 1024 addresses for the passive subscribers.

$\overline{BB}$:
The signal $\overline{BB}$ (Bus Busy) shows the bus occupation by an active subscriber.

$\overline{RBB}$:
The signal $\overline{RBB}$ (Resetting Bus Busy) displays that the bus is to be released immediately for the CCU (central control unit).

$\overline{BOV}$:
The signal $\overline{BOV}$ (Bus Operation Valid) codes a bus operation as valid.

RDY:
The signal RDY (Ready) displays to the sending subscriber, that the data were written or that they can be read. It is the acknowledgement signal for $\overline{BOV}$.

$\overline{SRQ}$:
The signal $\overline{SRQ}$ (Service Request) informs the CCU of one or more valid interrupts (collective interrupts). The identification of the subscriber sending the interrupt is carried out by means of the signals $\overline{HSRQ}$ and ACK. The evaluation is carried out, when an interrupt vector is read by the CCU. A bus assignment is generally carried out afterwards by the CCU.

$\overline{HSRQ}$:
The signal $\overline{HSRQ}$ (Hold Status Service Request) displays to the subscribers, that an interrupt treatment is initiated. The interrupt status may no longer be changed.

ACK:
The signal ACK (Acknowledge) is output by the CCU for the identification of the subscriber giving the interrupt with the highest priority.For this, the signal is looped through all the subscribers and creates a priority chain, whereby it is only handed on to the next subscriber by the previous subscriber, if it has not had its own wish for an interrupt.

$\overline{DMARQ}$:
The signal $\overline{DMARQ}$ (DMA Request) applies for a direct memory access at the CCU.

DMACK:
The signal DMACK (DMA Acknowledge) is created by the CCU. It is the acknowledgement signal of $\overline{DMARQ}$.

$\overline{SYNC}$:
The signal $\overline{SYNC}$ (Synchronisation Signal) starts subscribers maskable with the one-zero edge asynchronously to the bus operation.

$\overline{RS}$:
The signal $\overline{RS}$ (Reset) is used in order to bring all the subscribers to their starting status at the same time.

CC:
The signal CC (Central Clock) is a central clock, which is formed on the CCU. Its frequency lies between 1 and 5 MHz, its pulse duty factor between 25% and 75%.

$\overline{PFD}$:
The signal $\overline{PFD}$ (Power Failure Detect) codes a voltage failure.

1.3.3 Addressing the subscribers

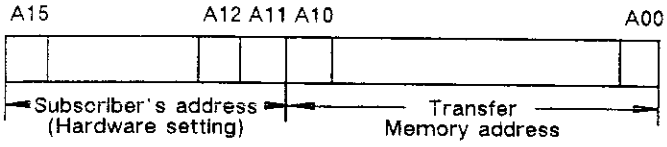
The distinction between addressing passive and active subscribers is made by the signal $\overline{I/O}$.

Addressing active subscribers

Every active subscriber includes a transfer memory area to communicate in the ABB Procontic T300 sys-

tem. Active subscribers are addressed via A11 to A15 ($\overline{I/O}$ = 1). A00 to A10 addresses a memory position in the transfer memory area of the active subscriber (2 kbytes).

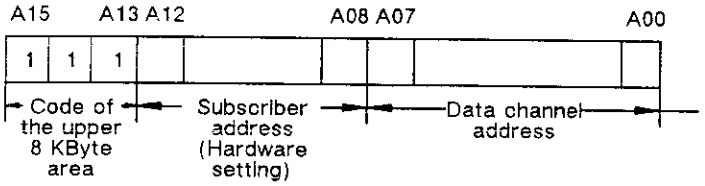
If a subscriber requires a larger transfer memory area (n times 2 kbytes), it can occupy several subscriber addresses.



Addressing passive subscribers

Passive subscribers are addressed by A00 to A15 ($\overline{I/O}$ = 0). The addresses smaller than **56 x 1024** are reserved **for addressing the memory** of the address area of 64 x 1024 addresses. The upper **8 x 1024 addresses** are foreseen **for data channels** of passive subscribers; A08 to A12 therefore include the address of the respective subscriber.

The subscriber address of A05 to A12 or of A02 to A12 can be set for passive subscribers, which require a smaller address area for data channels.



1.3.4 Bus operations

The following bus operations are foreseen for the MPST bus:

- Writing
- Reading
- DMA transfer
- Interrupt transfer

The exact sequences of the bus accesses are defined independently of the manufacturer in the MPST standard, DIN 66264 part 1.

1.3.5 Exchange of data and access priority

Seen from the front of the subrack, the processor in the extreme right-hand slot has the highest priority as concerns the bus accesses. If a processor carries out a bus access, it cannot be interrupted. A processor can receive the bus access for several operations via the "Lock" mechanism.

The further to the left that a subscriber is slotted in the subrack, the less is its priority concerning bus accesses.

1.4 Electrical characteristics

All levels are measured under load on the plug connector on the respective electronic card.

1.4.1 Voltage supply

+5V DC (U_{B1}), +15V DC (U_{B2}) and -15V DC (U_{B3}) are defined as voltage supplies. The tolerance values amount to +5%, -3%, referring to the nominal value.

1.4.2 Signal levels (bus signals)

The electrical levels of the MPST bus signals are defined as follows:

		Voltage range	Current limit value
Input	logical zero	0 V to 0.6 V	max. 0.5 mA
	logical one	2.1 V to U_{B1}	max. 20 µA with GT max. 60 µA with T, OC
Output	logical zero	0 V to 0.5 V	min. 16 mA
	logical one	2.3 V to U_{B1}	min. 400 µA with GT min. 3.0 mA with T, OC

T = Tristate
OC = Open collector
GT = Realisation with push-pull or OC with a PULL-UP resistor on the module

1. 4.3 Non-specified bus connections

The voltage for these connections may not exceed the limit of ± 42 V. A current of max. 500 mA is permitted.

1.5 Mechanical structure

The subrack must correspond to DIN 41494, part 5. The size amounts to 19 inches, 6 height units. The assembly of the subrack is foreseen for switch cabinets with a depth of $\geq$ 400 mm. The printed boards have the format of 160 mm x 233.4 mm according to DIN 41494, part 2. Two 32-polar plug connectors in accordance with DIN 41612, part 2, in the constructive form C are used.

The corresponding socket connectors in accordance with DIN 41612, part 2, with the constructive form C are to be used as the mating component. The arrangement of the connectors is to be carried out according to DIN 41494, part 5, issue of September 1980, footnote 8.

The increments, which can be used within the subrack, amount to 84 x 5.08 mm. The distance between these slots amounts to 4 increments (20.32 mm) or whole number multiplications of 4. 21 possible slots for subracks result in this way, DIN 41494 A - 6W - 164 - 84.

• Application categories and reliability data	according to DIN 40 040
• Permitted ambient temperature: Operation	0 ... + 55 °C (Letter symbols KV)
• Transport and storage	– 25 ... + 85 °C (Letter symbols HP)
• Relative humidity	≤ 75 % annual average 95 % on 30 days/year (Letter symbol F)
• Permitted operating height	0 ... 2200 m above mean sea level (Letter symbol R)
• Degrees of protection	according to DIN 40 050, part 3
• Subracks, units	IP00
• Cabinets	IP54
• Front of the operating panels	IP65
• Vibration test	according to DIN VDE 0160/5.88
• Radio interference level	according to DIN VDE 0871, limit value category B
• Noise immunity to conducted, transient interference voltages	according to IEC 801-4/draft 12.85
• Communication interfaces	Test category 2 (0.5 kV)
• Supply connections	Test category 3 (2 kV)
• Process in- and outputs 24 V DC	Test category 3 (1 kV)
• Process in- and outputs 220 V AC	Test category 4 (2 kV)

Note: Deviations are listed separately within the description of the subracks/units.

2 Fans and Subracks

34 LU 31 R2: Fan for 220 V AC
35 GS 91 R1: Subrack with power supply unit 35 NE 90 R1, 220 V AC for + 5 V DC/25 A, ± 15 V DC/1 A
35 GS 93 R1: Subrack with power supply unit 35 NE 93 R1, 24 V DC for + 5 V DC/12 A, ± 15 V DC/2 A

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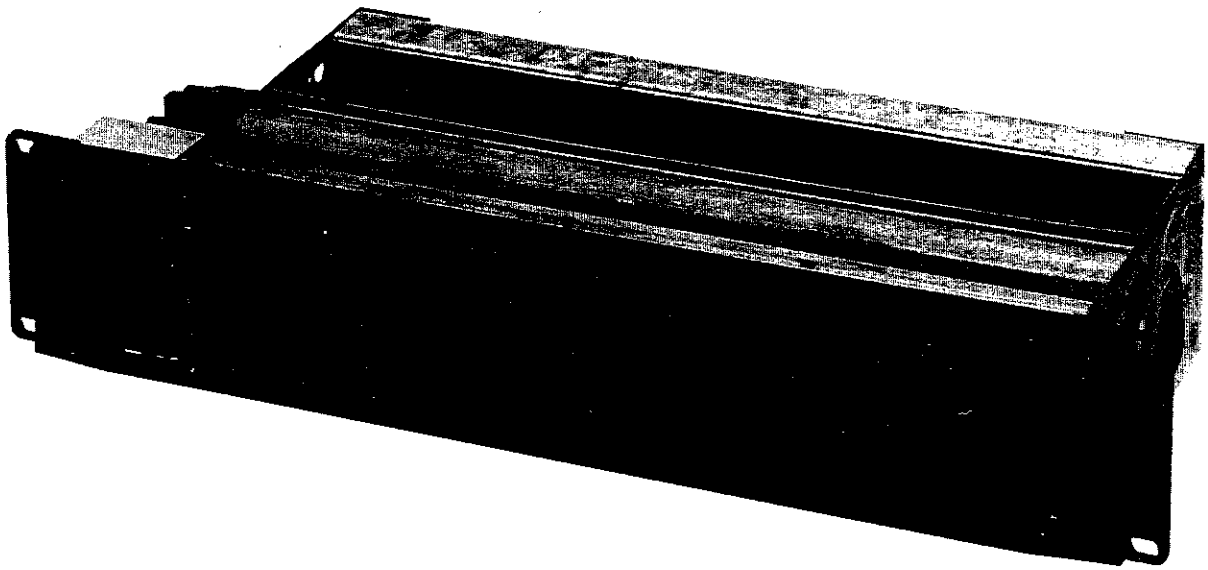
2.1 Fan 34 LU 31 R2



90 01 95

2.1.1 Technical data

Inputs with 220 V AC, 50 Hz	35 W
Inputs with 220 V AC, 60 Hz	45 W
Weight	2.5 kg
Order number	GJV3071301R2

2.1.2 Description

A fan **must** be installed under each basic subrack (see the planning manual, volume 5). The fan 34 LU 31 is designed as a tangential fan with a filter mat and an airflow monitor.

2.1.3 Connecting the fan 34 LU 31

Height of the fan 34 LU 31: 88.7 mm (2 height modules)

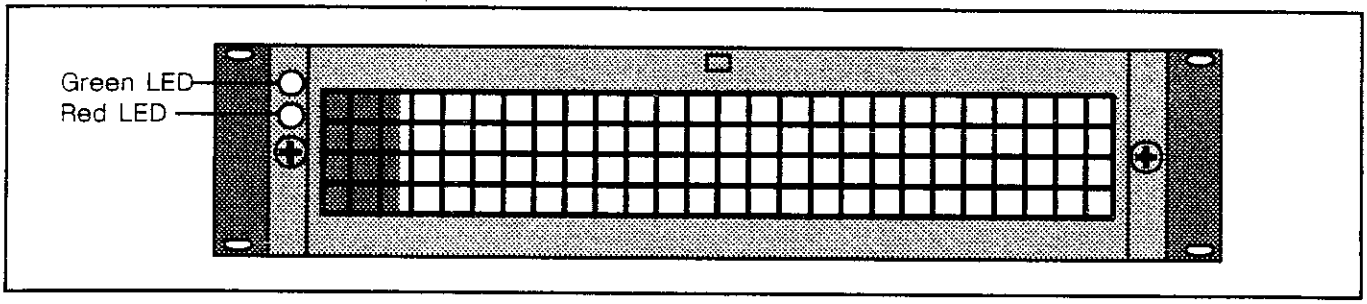


Fig. 2.1-1: Front view 34 LU 31 R2

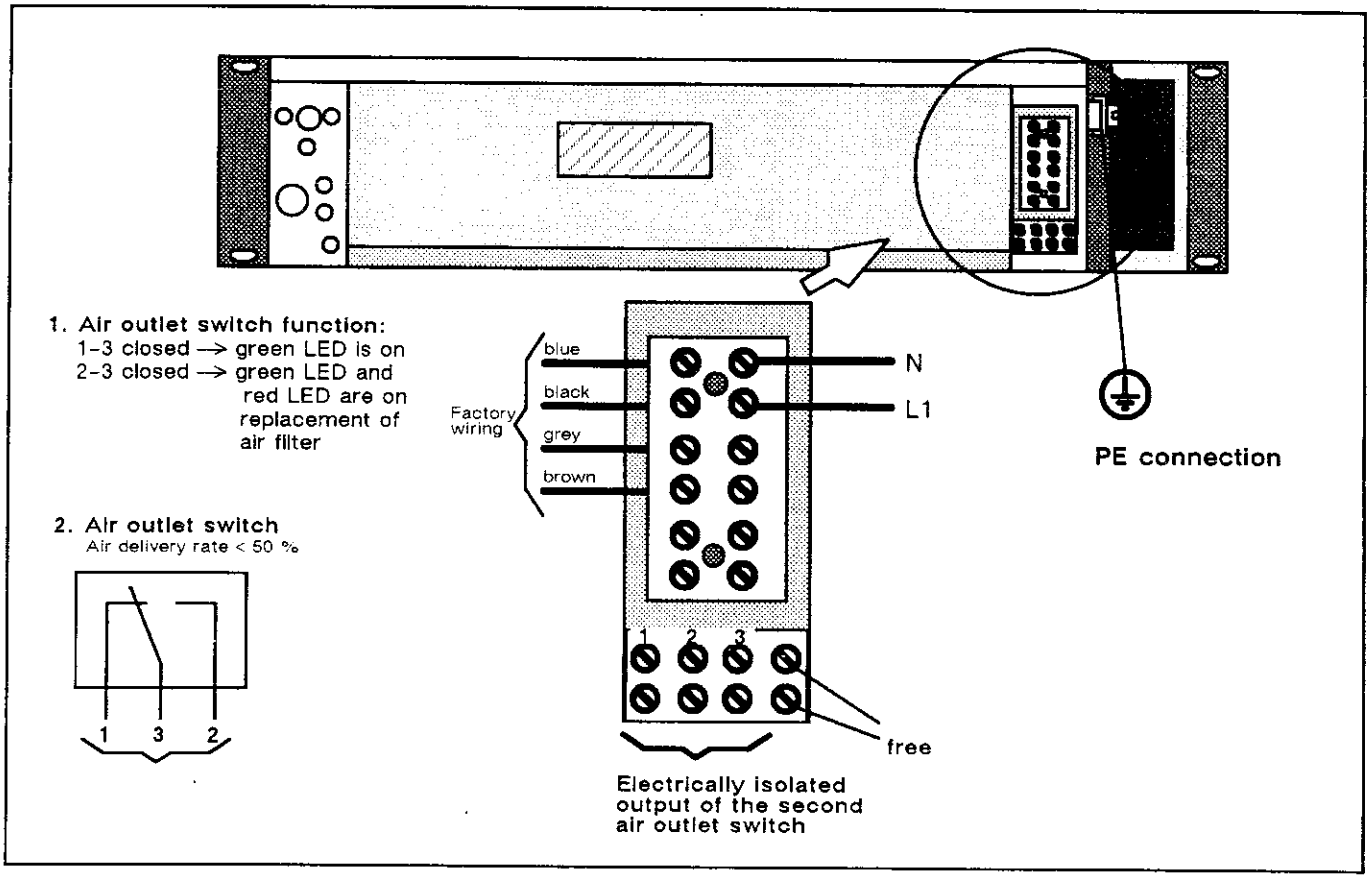
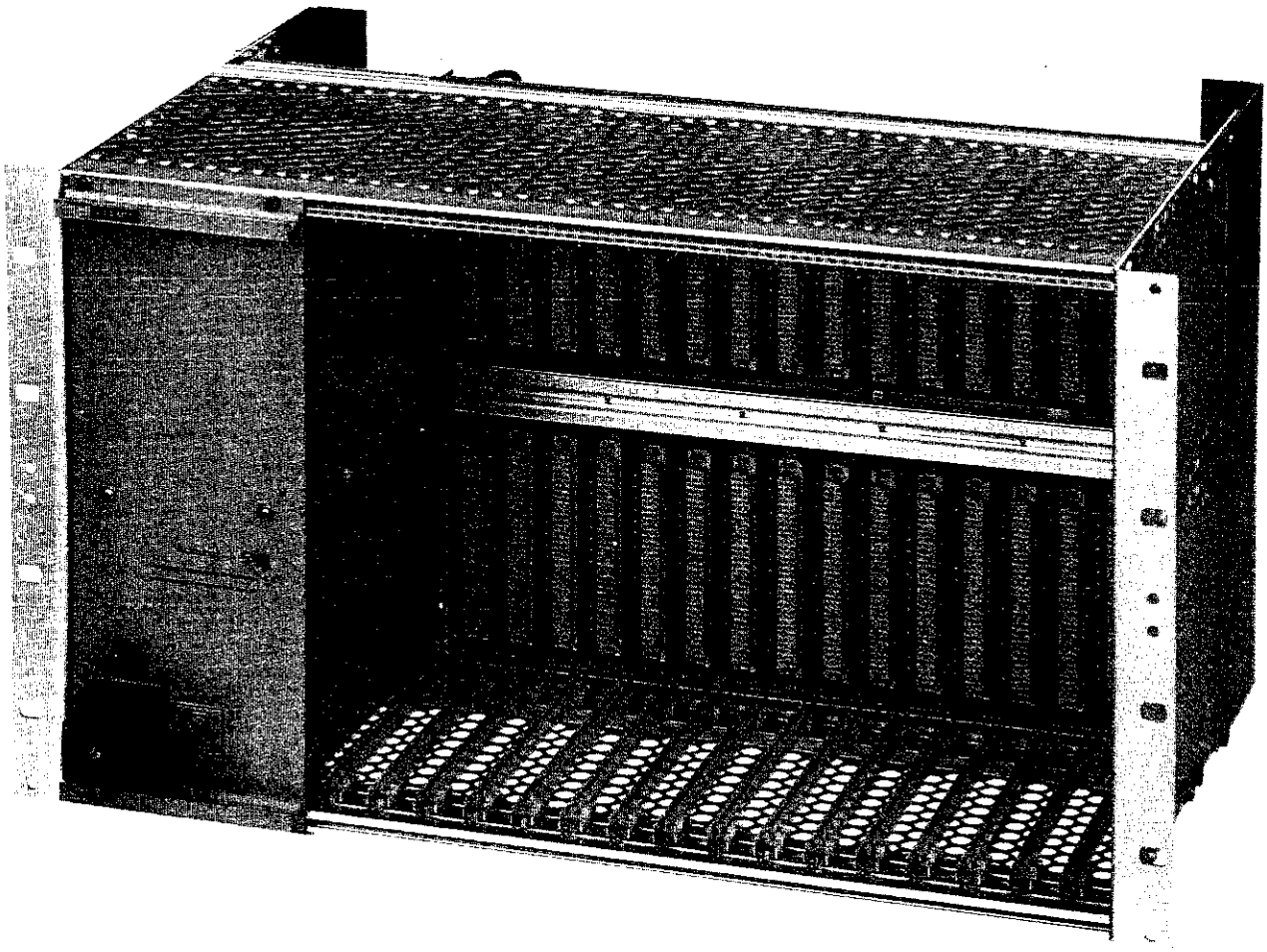


Fig. 2.1-2: Rear view 34 LU 31 R2

Without an ON/OFF switch; green indicator lamp for correct functioning. If the air delivery rate in the fan sinks below 50%, the green lamp stays alight and the red lamp lights up as well, replacement of the air filter. The operating status of the fan can be output on the control via a floating contact (250 V AC and/or DC, 5 A).

2.2 Subrack 35 GS 91 R1 with a power supply unit 35 NE 90 R1 for 220 V AC voltage supply



90 01 97

2.2.1 Technical data

Subrack 35 GS 91 R1:

Component slots	16
Earthing arrangement	Faston 6.3 mm on the subrack
Humidity rating	F according to DIN 40 040 without moisture condensation
Weight (with power supply unit)	8.94 kg
Order number	GJR5136400R1

Power supply unit 35 NE 90 R1:

Supply voltage UP	220 V AC + 10 % / - 15 %
Current input	max. 2 A
Output UB1	+ 5 V DC, 25 A
Output UB2	+ 15 V DC, 1A
Output UB3	- 15 V DC, 1 A
External fuses	3.15 A time-lag
Connection	6.3 mm rear Faston terminal
Weight	3.5 kg
Order number	GJV3180801R1

Accessories:

Fan 34 LU 31 R2	GJV3071301R2

2.2.2 Description

The subrack 35 GS 91 with a bus printed board and a power supply unit is foreseen for connecting ABB Procontic T300 units.

The bus printed board is attached to the subrack, so that the right-hand edges are aligned.

A power supply unit 35 NE 90 is assembled on the left-hand side and requires 5 slots. The power supply unit works for low power dissipation using a primary-switch mode.

If the voltage of the power supply unit fails for longer than 20 ms on the input side, a corresponding signal $\overline{PFD}$ (Power Failure Detect) is generated for the power failure. The output voltage is buffered for at least a further 5 ms, until it falls below the tolerance limit. The monitoring circuit for the output voltage then generates a reset signal ($\overline{RS}$). The controller can rescue information concerning the current status in a buffery memory in the meantime.

A fan **must** be installed under each basic subrack (see the planning manual, volume 5). The fan 34 LU 31 to be integrated is designed as a tangential fan (see chapter 2.1) with a filter mat and an air flow monitoring.

2.2.3 Mechanical structure

The subrack is built for the connection of printed boards in the double-size Eurocard format 233.4 mm x 160 mm x 20.32 mm. It can be installed into a 19" frame in accordance with DIN 41494. The side walls and the longitudinal sections are made from zinc-coated plates, and the guide mats are made from plastic.

2.2.4 Dimensions of the subrack

The dimensions of the subrack are:

Height:	265.9 mm (< 6 height units, 1 height unit = 44.45 mm)
Width:	426.72 mm (84 pitches, 1 pitch = 5.08 mm)
Width with clamps:	482.3 mm
Depth:	276.9 mm

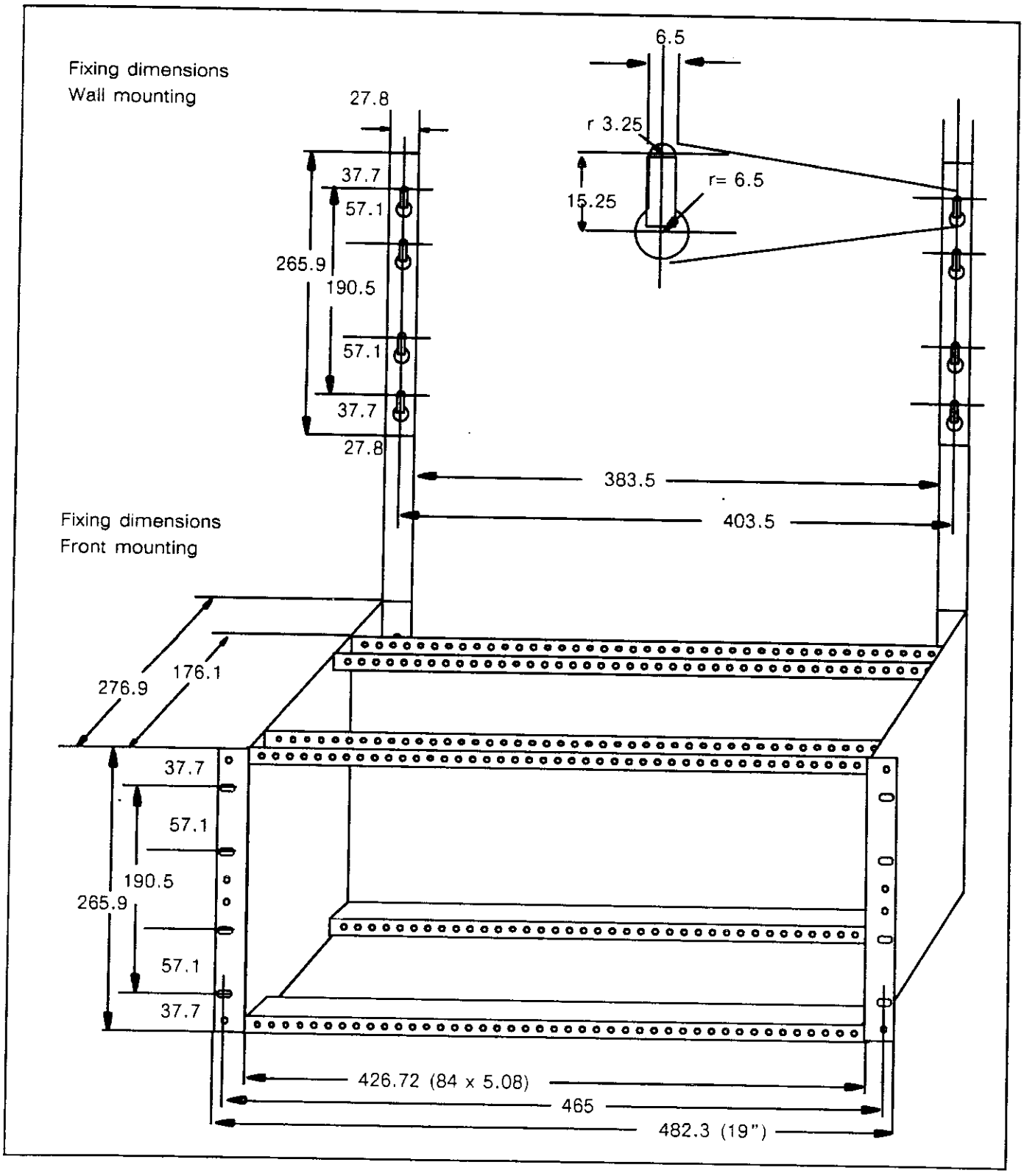


Fig. 2.2-1 Frame of the subrack

2.2.5 0 V DC and earth terminal of the subrack

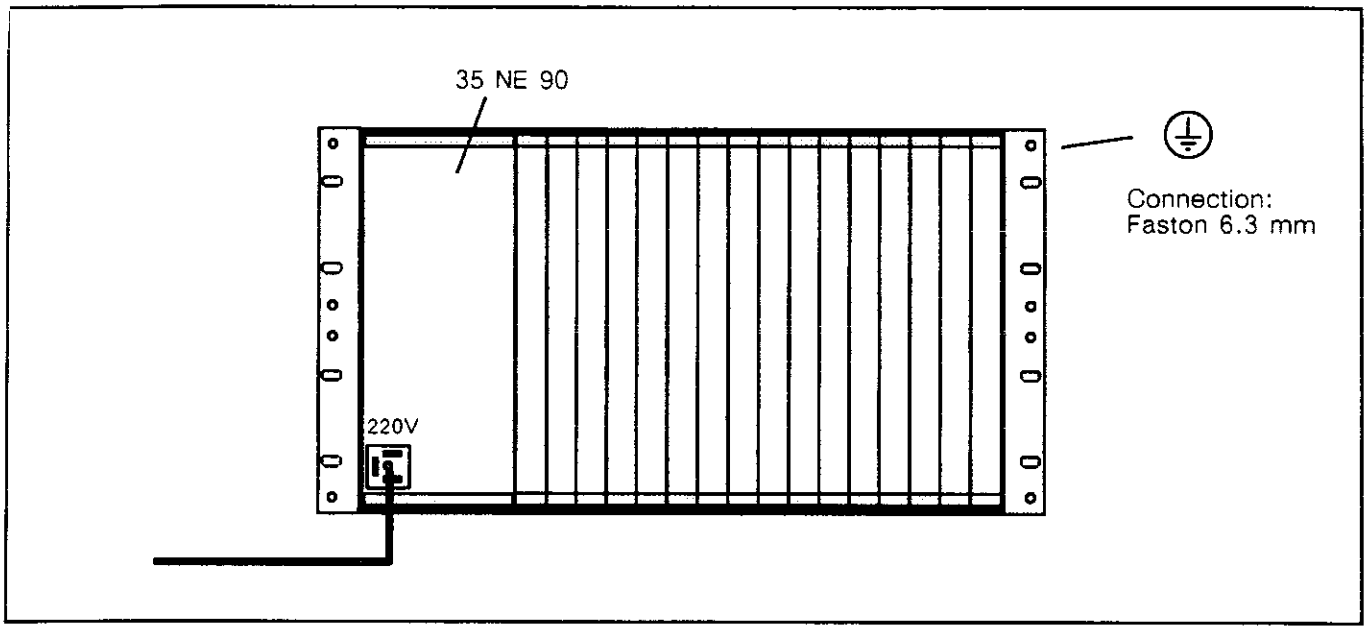


Fig. 2.2-2: 35 GS 91 with a power supply unit 35 NE 90

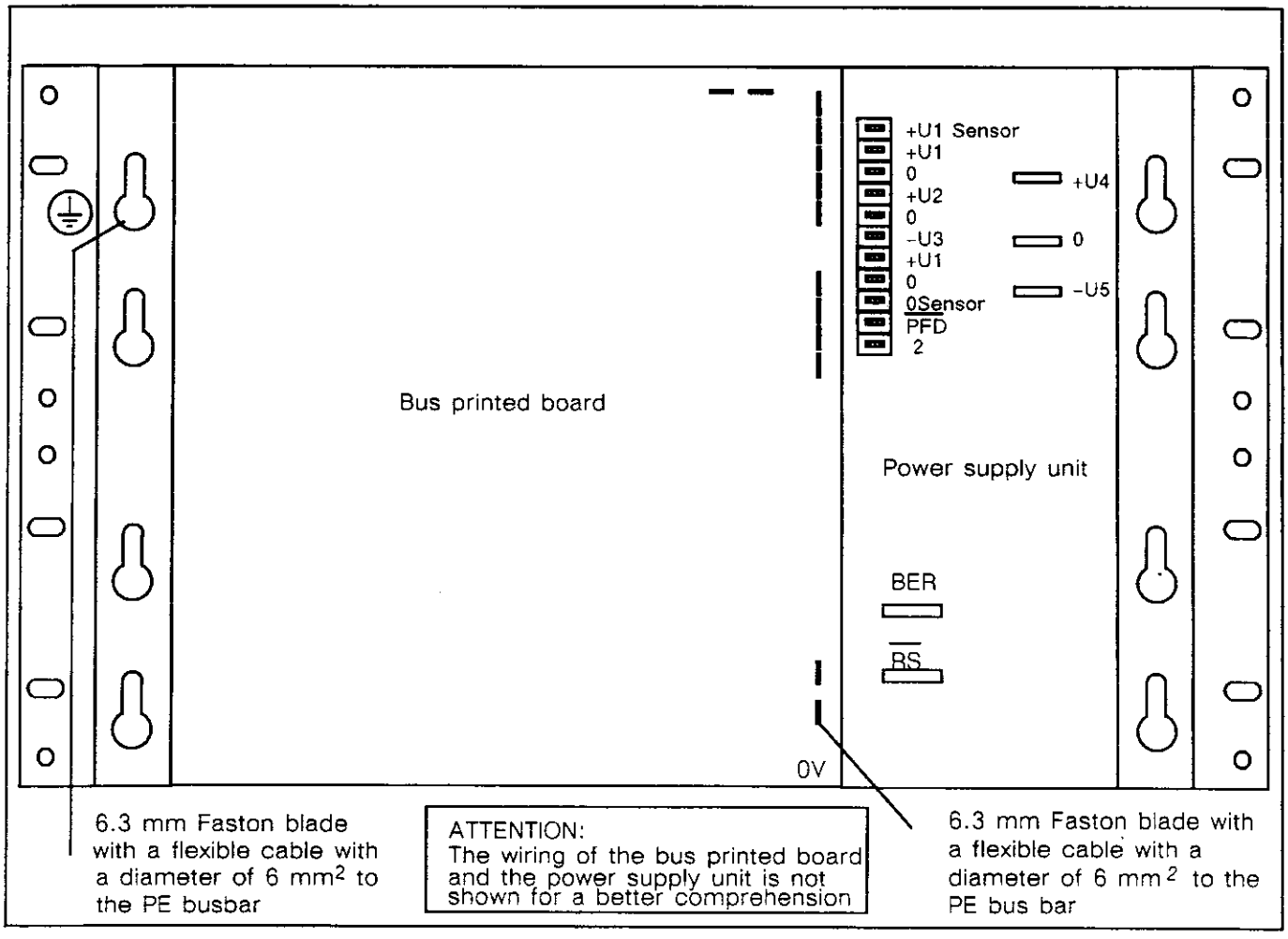
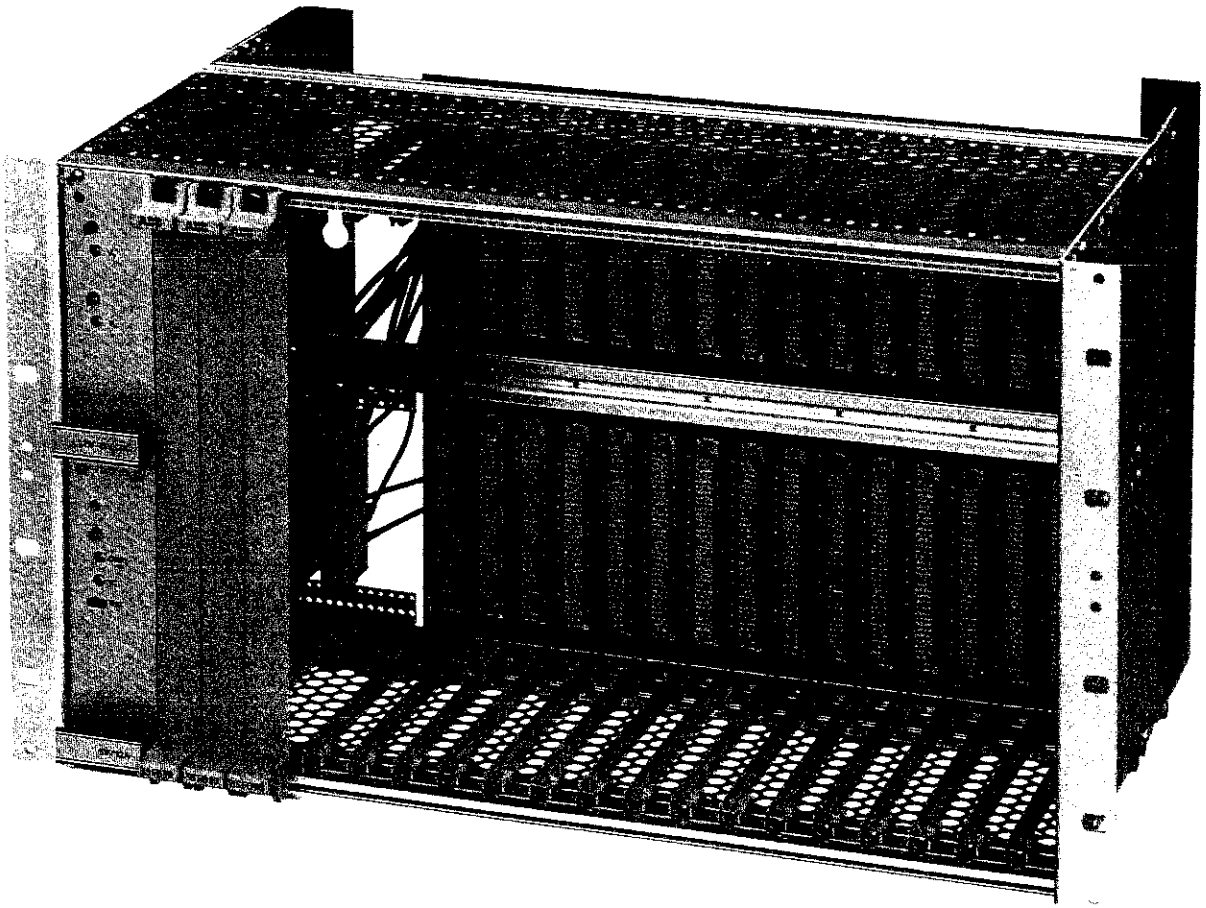


Fig. 2.2-3: Rear view of the subrack 35 GS 91 R1

2.3 Subrack 35 GS 93 R1 with a power supply unit 35 NE 93 R1 for 24 V DC voltage supply



90 01 96

2.3.1 Technical Data

Subrack 35 GS 91 R1:

Component slots	16
Earthing arrangement	Faston 6.3 mm on the subrack
Humidity rating	F according to DIN 40 040 without moisture condensation
Weight (with power supply unit)	7.0 kg
Order number	GJR514400R1

Power supply unit 35 NE 93 R1:

Supply voltage U_P	24 V DC ± 30 %
Current input	max. 6.6 A
Output U_{B1}	+ 5 V DC, 12 A
Output U_{B2}	+ 15 V DC, 2 A
Output U_{B3}	- 15 V DC, 2 A
External fuses	10 A time-lag
Connection	6.3 mm rear faston terminal
Weight	2.0 kg
Order number	GJV3072601R1

Accessories:

Fan 34 LU 31 R2	GJV3071301R2

2.3.2 Description

The subrack 35 GS 93 with a bus printed board and a power supply unit is foreseen for connecting ABB Procontic T300 units.

The bus printed board is attached to the subrack, so that the right-hand edges are aligned.

A power supply unit 35 NE 93 is assembled on the left-hand side and requires 2 slots. The power supply unit 35 NE 93 can supply a partially equipped subrack depending on the current input of the installed units. A second power supply 35 NG 93 can be installed, if necessary. The in- and output voltages of the power supply unit are monitored.

If the voltage of the power supply unit fails for longer than 20 ms on the input side, a corresponding signal $\overline{PFD}$ (Power Failure Detect) is generated for the power failure. The output voltage is buffered for at least a further 1.5 ms until it sinks below the tolerance level. The monitoring circuit for the output voltage then generates a reset signal ($\overline{RS}$). The control can rescue information concerning the current status in a buffer memory in the meantime.

A fan **must** be installed under each basic subrack (see the planning manual, volume 5). The fan 34 LU 31 to be integrated is designed as a tangential fan (see chapter 2.1) with a filter mat and an air flow monitoring.

2.2.3 Mechanical structure

The subrack is built for the connection of printed boards in the double-size Eurocard format 233.4 mm x 160 mm x 20.32 mm. It can be installed into a 19" frame in accordance with DIN 41494. The side walls and the longitudinal sections are made from zinc-coated plates, and the guide mats are made from plastic.

2.3.4 Dimensions of the subrack

The dimensions of the subrack are:

Height:	265.9 mm (< 6 height units, 1 height unit = 44.45 mm)
Width:	426.72 mm (84 pitches, 1 pitch = 5.08 mm)
Width with clamps:	482.3 mm
Depth:	276.9 mm

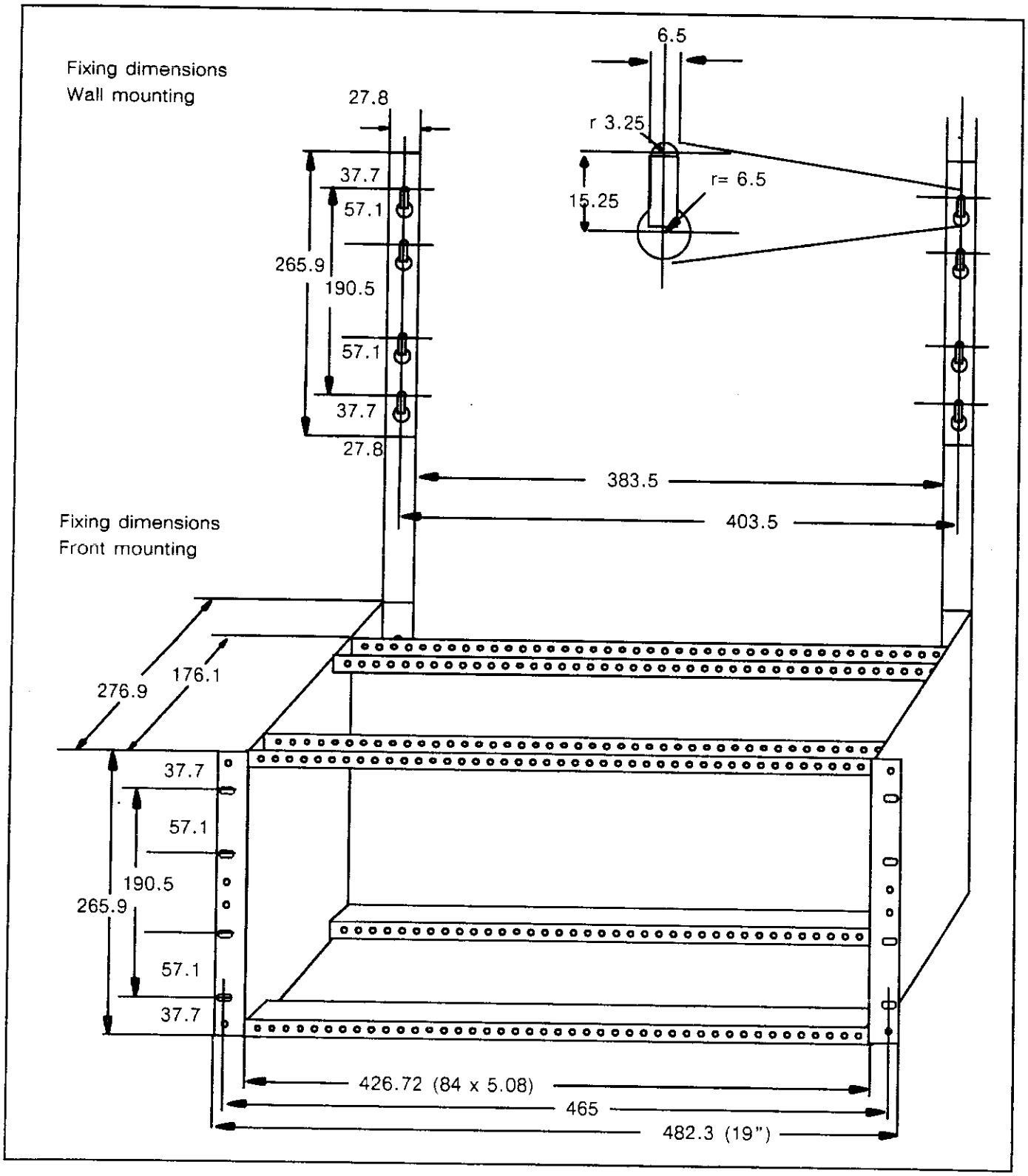


Fig. 2.3-1 Frame of the subrack

2.3.5 Supply voltage and earth connection of the subrack 35 GS 93 R1

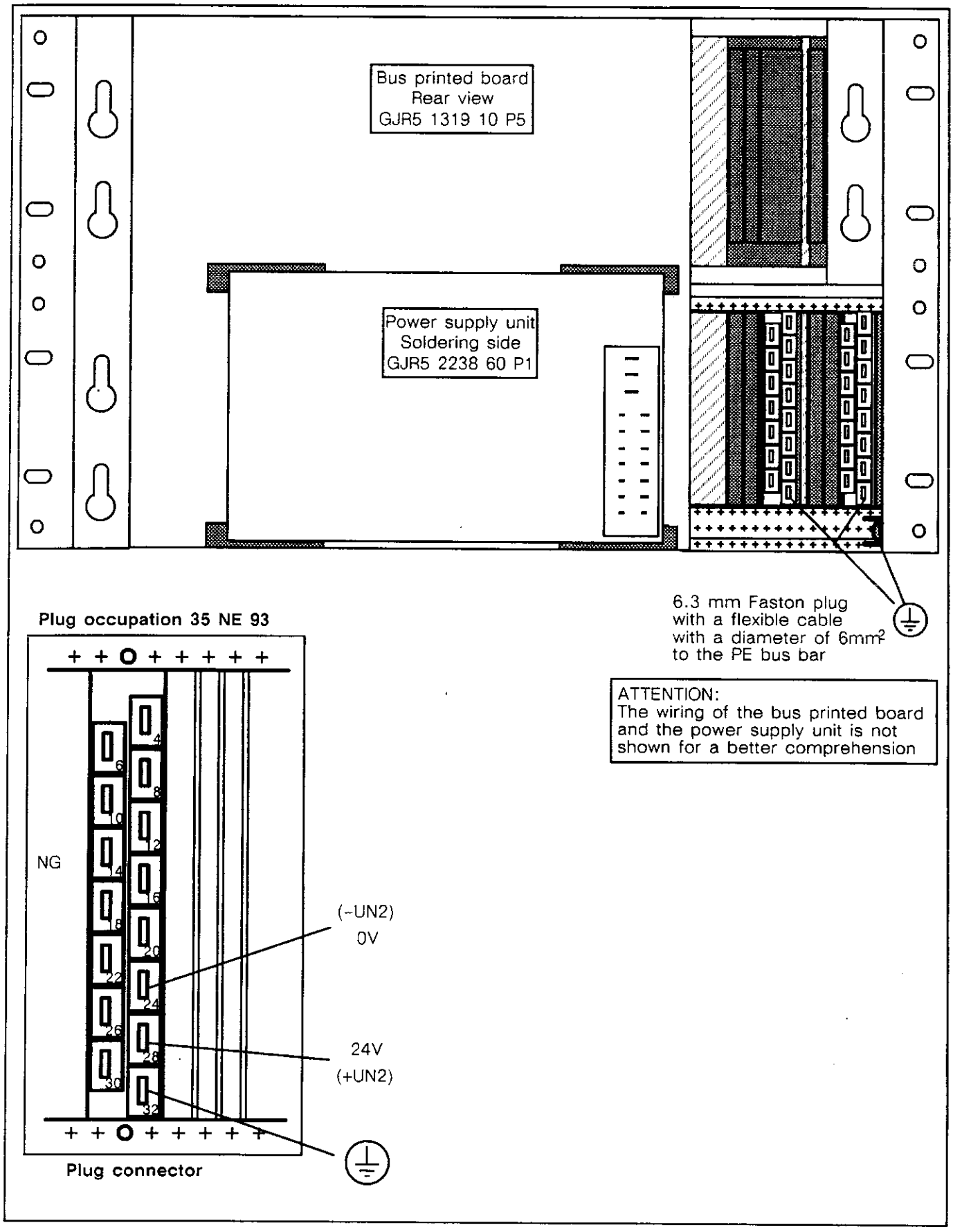


Bild 2.3-2 Rear view of the subrack 35 GS 93 R1

2.3.6 Adjustment regulations when using two power supply units 35 NE 93 R1

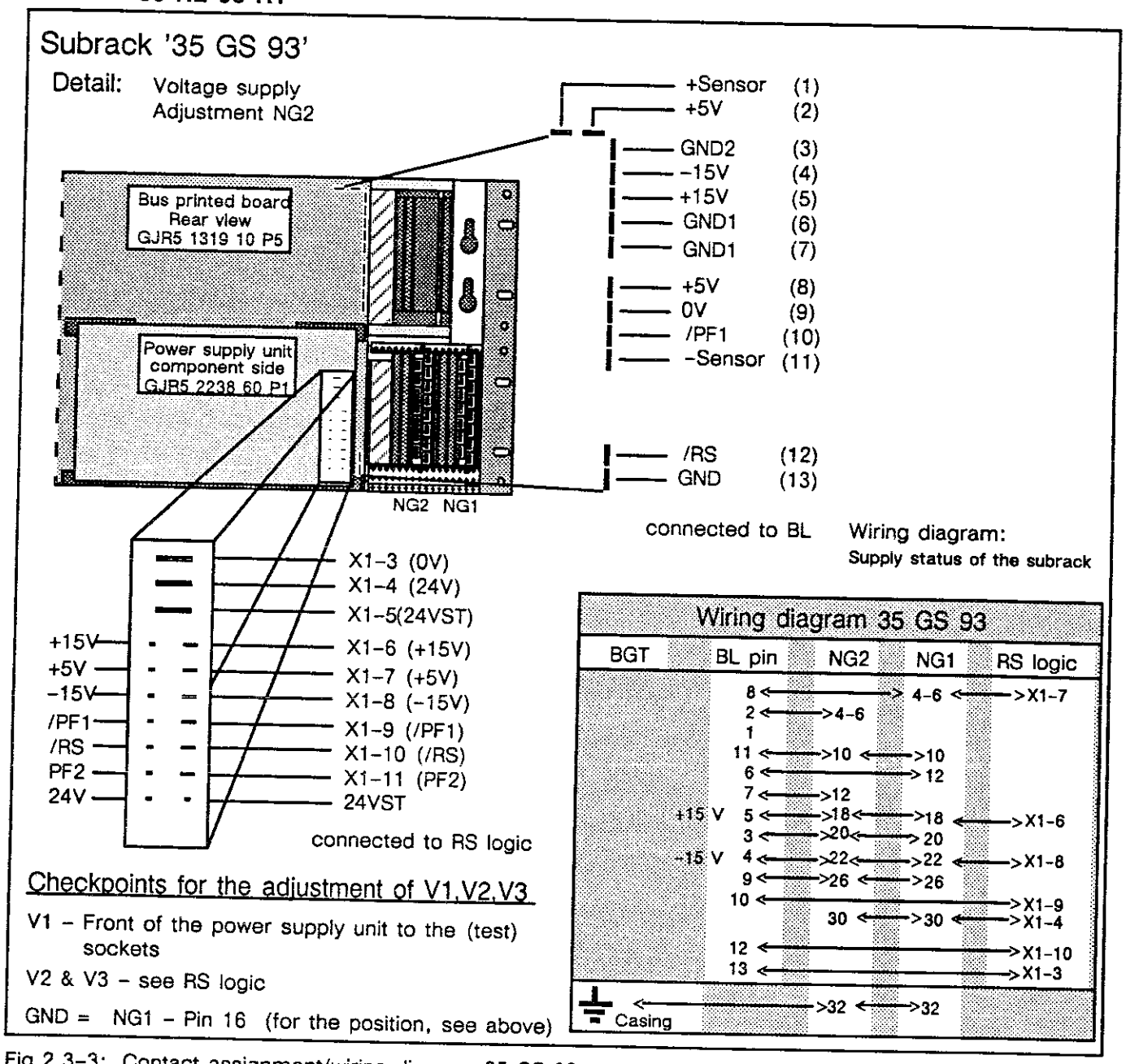


Fig.2.3-3: Contact assignment/wiring diagram 35 GS 93

1. Measure and **note the voltage value 'V_1','V_2','V_3' of the power supply unit** already located in the subrack but without a load. NG1 is the reference unit for the adjustment of NG2.

2. **Swap the power supply units.** The unit NG2 must occupy the left-hand slot of the **subrack** during the adjustment. (Do **not** plug in NG1!)

3. **Adjust the voltage "V_1" of the secondary unit to the determined value** ($\Delta V_1 = V_1 \pm 0{,}1\%$). **The adjustment is carried out with the potentiometer** (V_1), which can be reached through the front panel.

4. The adjustment for V2 and V3 done in the factory is sufficient. In exceptional cases the adjustment is to be done as follows:

   Adjust the voltage "V_2" of the secondary unit to the determined value ($\Delta V_2 = V_2 \pm 0{,}1\%$). **The adjustment is carried out with the potentiometer** (V_2), which can be reached through the front panel.

   Adjust the voltage "V_3" of the secondary unit to the determined value ($\Delta V_3 = V_3 \pm 0{,}1\%$). **The adjustment is carried out with the potentiometer** (V_3), which can be reached through the front panel.

5. **Return the reference unit (NG1) to its previous position.**

6. **Remove the blanking plates and plug in the adjusted power supply unit (NG2) next to the reference unit.**

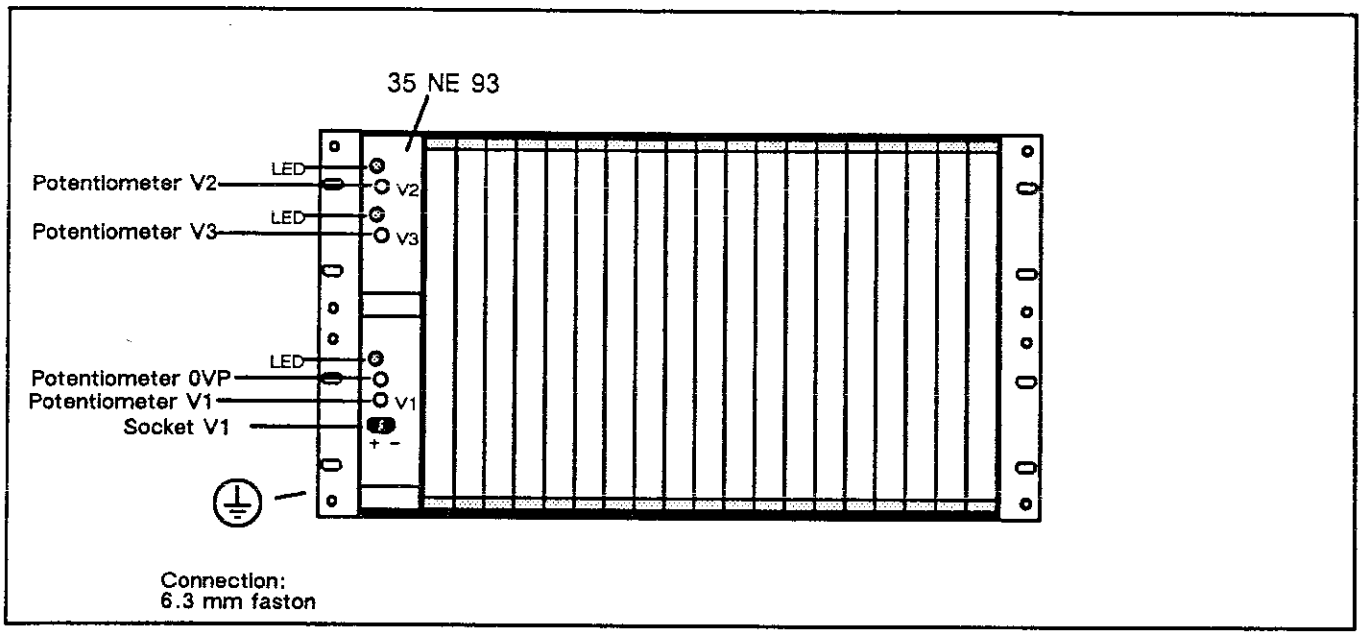


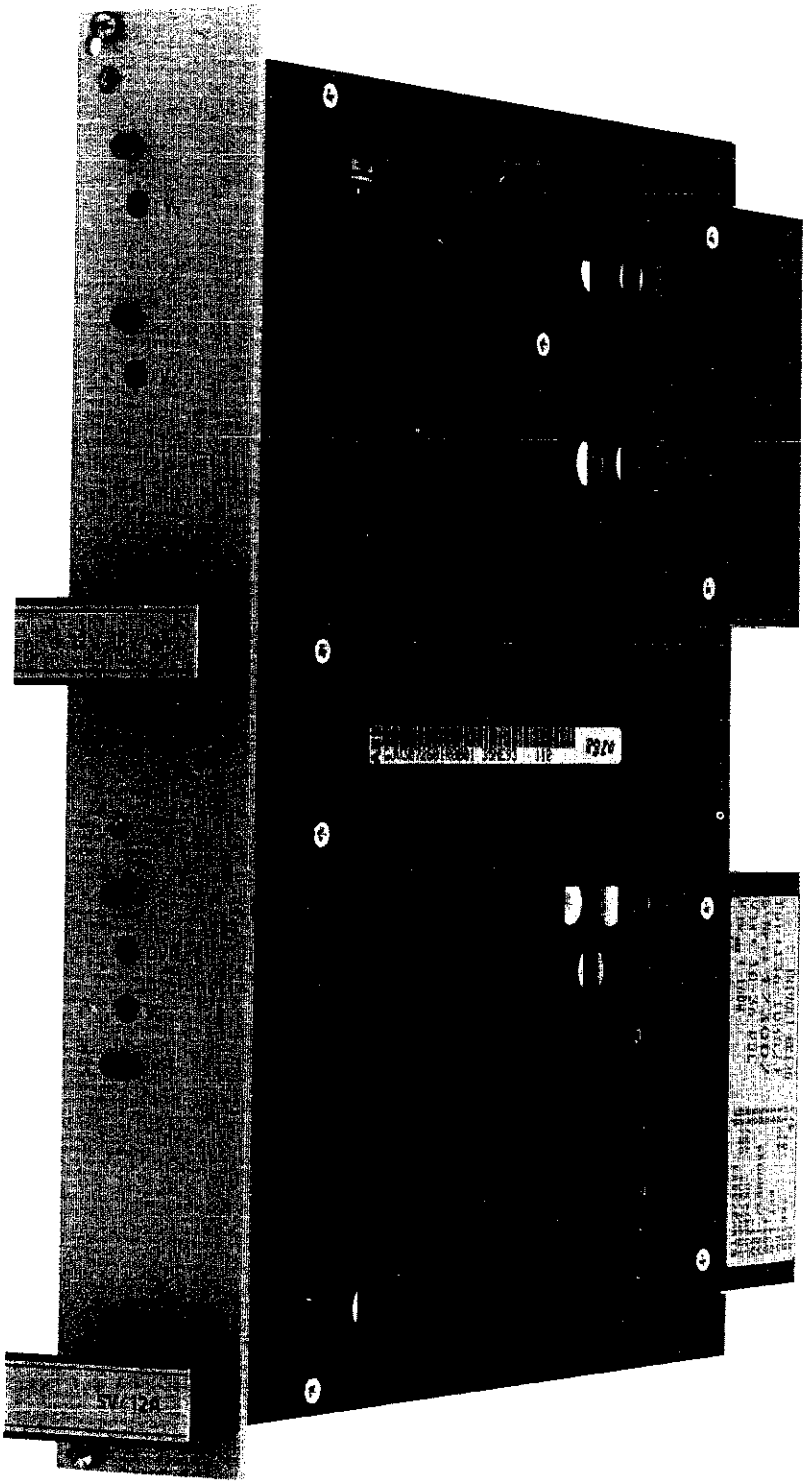
Fig. 2.3-4: 35 GS 93 with the power supply unit 35 NE 93

3 Power supply units

35 NE 93 R1: Power supply unit 24 V DC for + 5 V DC/12 A, ± 15 V DC/2 A

3.1	Power supply unit 35 NE 93 R1 for 24 V DC voltage supply ..	3.1- 1
3.1.1	Technical data	3.1- 2
3.1.2	Description	3.1- 2
3.1.3	Mechanical structure	3.1- 2
3.1.4	Adjustment reguiations when using two power supply units 35 NE 93 R1	3.1- 2

3.1 Power supply unit 35 NE 93 R1 for 24 V DC voltage supply



90 01 92

3.1.1 Technical Data

Supply voltage UP	24 V DC ± 30 %
Current input	max. 6.6 A
Output UB1	+ 5 V DC, 12 A
Output UB2	+ 15 V DC, 2 A
Output UB3	– 15 V DC, 2 A
External fuses	10 A time-lag
Connection	6.3 mm rear Faston terminal
Dimension	2 pitches
Weight	2.0 kg
Order number	GJV3072601R1

3.1.2 Description

A power supply unit 35 NE 93 is assembled on the left-hand side of the subrack 35 GS 93 R1 and requires 2 slots. The power supply unit 35 NE 93 can supply a partially equipped subrack depending on the current input of the installed units. A second mains unit 35 NG 93 can be installed, if necessary. The in- and output voltages of the power supply unit are monitored.

If the voltage of the power supply unit fails for longer than 20 ms on the input side, a corresponding signal $\overline{PFD}$ (Power Failure Detect) is generated for the power failure. The output voltage is buffered for at least a further 1.5 ms until it sinks below the tolerance level. The monitoring circuit for the output voltage then generates a reset signal ($\overline{RS}$). The control can rescue information concerning the current status in a buffer memory in the meantime.

3.1.3 Mechanical structure

Plug-in card of double-size Eurocard format 160 x 233.4 mm, 2 pitches.

3.1.4 Adjustment regulations when using two power supply units 35 NE 93 R1

See section 2.3.6.

4 Bus coupler units

35 EK 90 R1: Bus coupler unit for the basic subrack.
35 EK 91 R1: Bus coupler unit for the extension subrack.
35 SK 96 R1: Connecting cable betweeen the bus coupling units.
Example of a bus coupling.

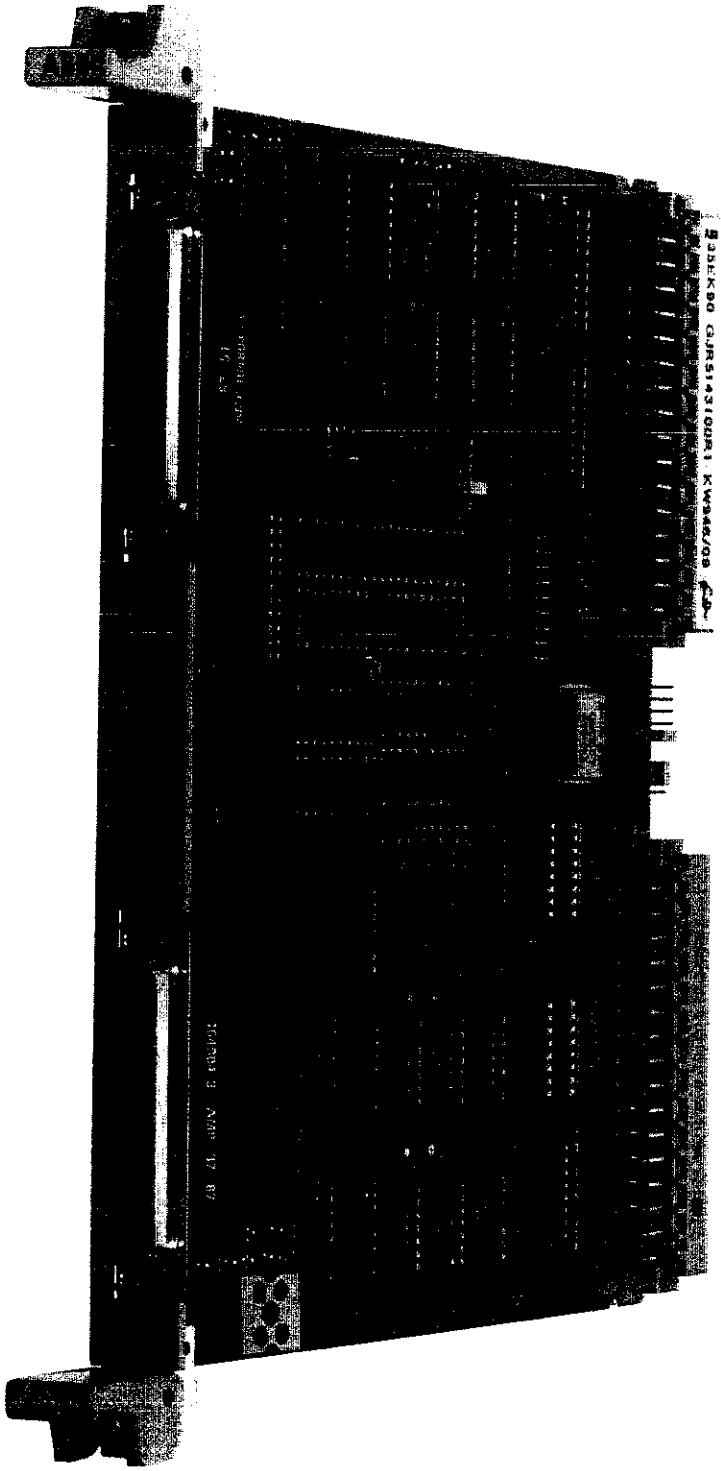
4.1 Bus coupler unit 35 EK 90 R1 for the basic subrack 4.1- 1
4.1.1 Technical data 4.1- 2
4.1.2 Description 4.1- 2
4.1.3 Function 4.1- 2
4.1.4 Example of a bus coupling 4.1- 2
4.1.5 Mechanical structure 4.1- 3
4.1.6 Settings 4.1- 3
4.1.7 Soldering bridges for cable screens 4.1- 3

4.2 Bus coupler unit 35 EK 91 R1 for the extension subrack ... 4.2- 1
4.2.1 Technical data 4.2- 2
4.2.2 Description 4.2- 2
4.2.3 Function 4.2- 2
4.2.4 Example of a bus coupling 4.2- 2
4.2.5 Mechanical structure 4.2- 3
4.2.6 Settings 4.2- 3
4.2.7 Soldering bridges for cable screens 4.2- 3

4.3 Connecting cable 35 SK 96 R1 for bus coupler units 4.3- 1
4.3.1 Technical data 4.3- 2
4.3.2 Description 4.3- 2
4.3.3 Soldering bridges for cable screens 4.3- 2

4.4 Example of a bus coupling with the bus coupler units 35 EK 90, 35 EK 91 and the connecting cable 35 SK 96 ..... 4.4- 1
4.4.1 Description 4.4- 2
4.4.2 Example 4.4- 2

4.1 Bus coupler unit 35 EK 90 R1 for the basic subrack



90 01 63

4.1.1 Technical data

Positive supply voltage U_{B1}	+5 V ± 5 %
Supply current I_{B1} to U_{B1} without a bus terminator	typically 1.0 A, max. 1.4 A
Supply current I_{B1} to U_{B1} with a bus terminator	typically 1.4 A, max. 1.8 A
Ambient temperature	0 °C ... +55 °C
Storage temperature	-25 °C ... +75 °C
Humidity rating	F
Mechanical stress	in accordance with VDE 160 when installed
Dimensions	1 pitch
Weight	1.0 kg
Additional consignment	2 sub-printed boards with matching resistors, 2 dummy plugs for the front plugs, which are not occupied
Order number	GJR5143100R1

Accessories

Bus coupler unit 35 EK 91 R1 for the extension subracks	GJR5143200R1
Connecting cable 35 SK 96 R1 for the bus coupler units	GJR5143700R1

4.1.2 Description

A basic subrack (master) is connected to a maximum of three extension subracks (slaves) by means of the bus coupler units 35 EK 90, 35 EK 91 and the connecting cable 35 SK 96. The subracks to be connected to each other are placed on top of each other. The lowest subrack is connected to a bus coupler unit 35 EK 90 (so that the installation of the above-mentioned fan is possible below) and is thus the basic subrack. The extension subracks are placed above this and equipped with one bus coupler unit 35 EK 91 each.

Note:
The maximum distance between the lower edges of the two subracks amounts to 240 mm caused by the length of the cable 35 SK 96.

The bus coupler unit 35 EK 90 is designed, so that active and passive subscribers can be included in the basic subrack. In the extension subrack only passive subscribers without an interrupt can be included.

The lines of the system cable 35 SK 96 and the connecting lines between the front plugs of the bus coupler units form a bus, the repeater bus. The repeater bus , as an open collector bus, must be terminated on the first and last bus coupler unit with resistors. Sub printed boards, which can be plugged in, are used together with matching resistors. Two sub-printed boards are included as an addition to the delivery scope for the unit 35 EK 90.

The bus operations 'read' and 'write' are possible using the repeater bus.

ATTENTION:
In order to protect the bus coupler units from electrostatic contact, their non-occupied front plugs (X3 or X4) must be provided with dummy plugs. Two of these dummy plugs are also included in the delivery scope of the unit 35 EK 90.

4.1.3 Function

The unit 35 EK 90 extends the writing/reading cycle to 1.8 µs in order to achieve a safe method of transfer. The exchange of data in the I/O area of the MPST bus is only affected here.

The unit behaves like a passive user with a $\overline{BOV}$/RDY delay of 1.8 µs, which occupies all the I/O addresses.

The repeater bus transfers the MPST bus signals A, D, $\overline{I/O}$, $\overline{R}$, $\overline{W}$, WO, $\overline{BOV}$, RDY.

Control signals for the bus drivers in the extension subracks (GTAS and GTDS for slaves) or in the basic subrack (GTAM and GTDM for masters) are also formed as gate signals for addresse and data.

The signals $\overline{PFD}$, CC, $\overline{RS}$ (multiprocessor-based control bus signals) as well as ADET and OUTINH (optional signals) can be addressed directly with the corresponding bus contacts using the jumper zone X6.

4.1.4 Example of a bus coupling

See section 4.4.

4.1.5 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch

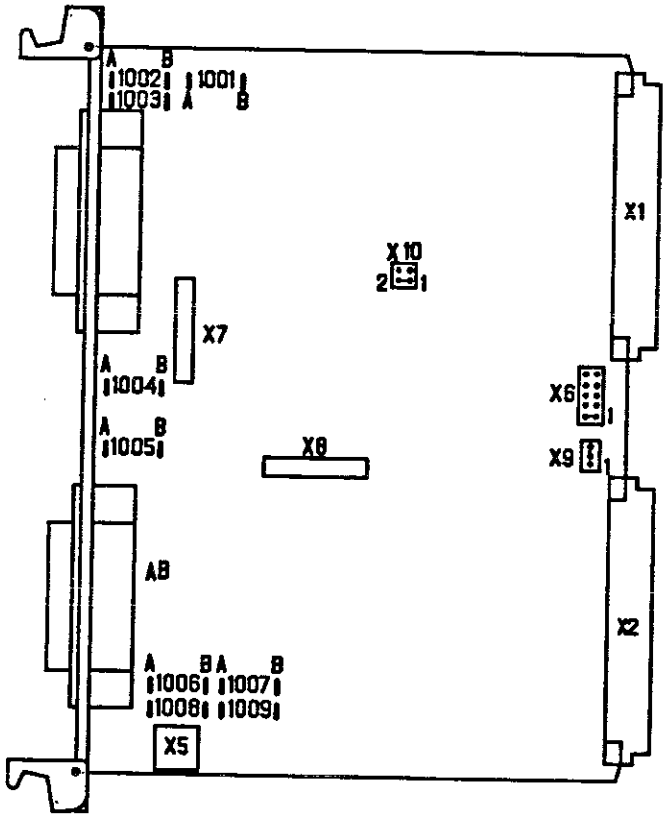


Fig. 4.1-1 Component side (top view)

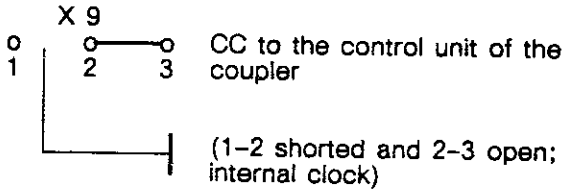
The drawn jumpers correspond to the factory setting; see also section 4.1.6, Settings.

X 1, X 2	Plug connectors with MPST bus signals according to DIN 66264
X 3, X 4	Plug connectors (50-polar) for the repeater bus RB, system cable 35 SK 96 connection, provided with dummy plugs if not occupied
X 5	Optional 0 V terminal
X 6	Disconnectable connection for $\overline{PFD}$, $\overline{RS}$, CC, ADET, OUTINH to the repeater bus
X 7, X 8	Plugs for the matching resistors of the repeater bus
X 9	CC/internal clock switchover
X10	RDY control
1001 ... 1009	wiring as required

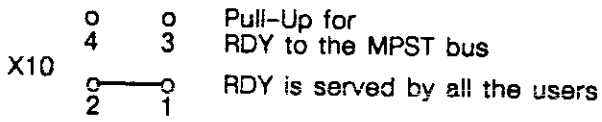
4.1.6 Settings

(Standard setting of the unit is drawn each time)

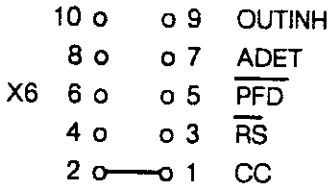
Clock signal setting **X9**:



READY signal setting **X10**:



Various signal settings **X6**:



4.1.7 Soldering bridges for cable screens

The soldering bridges for the 0 V or the front panel connection of the cable screens of the system cable 35 SK 96 are shown in Fig. 4.1-2.

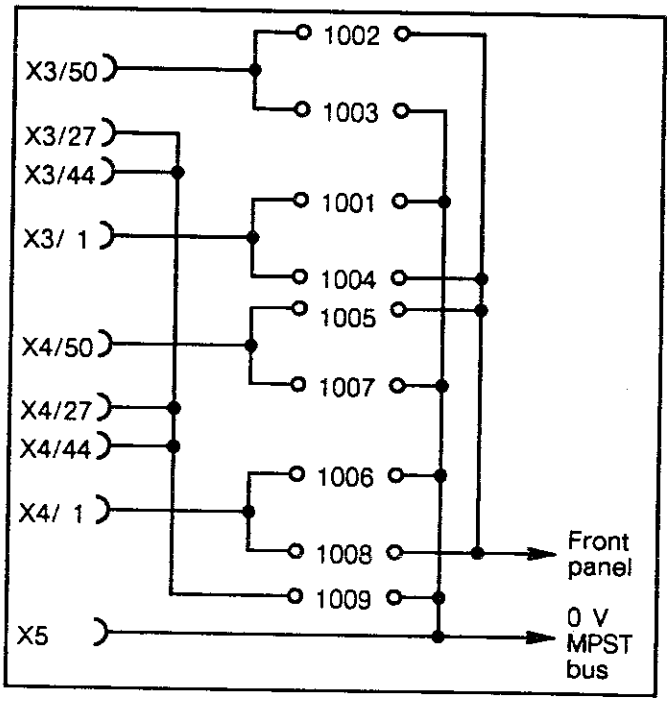
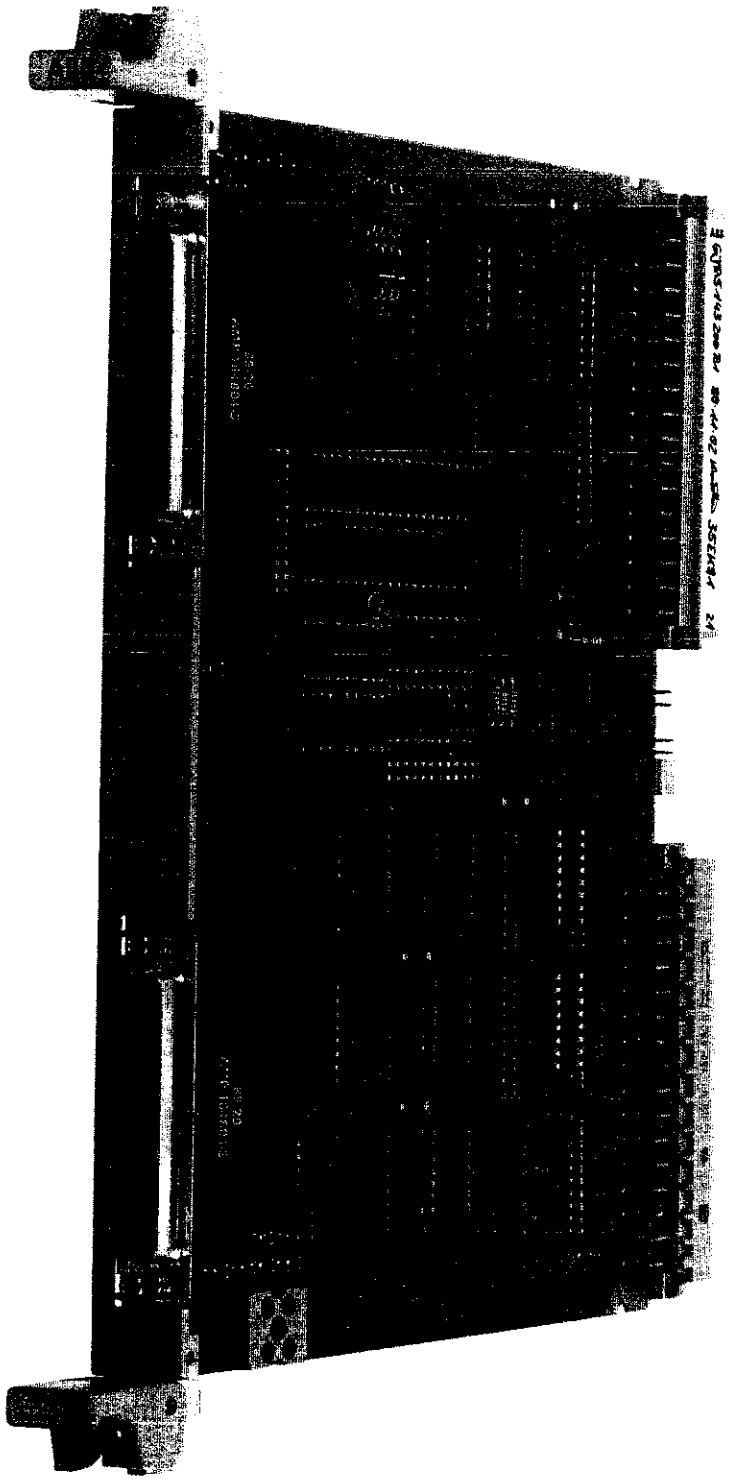


Fig. 4.1-2 Soldering bridges

The assignment of the plug connectors X3 and X4 is as follows:

X*/1	Screen, cable 1
X*/27	0 V, cable 1
X*/44	0 V, cable 2
X*/50	Screen, cable 2

4.2 Bus coupler unit 35 EK 91 R1 for the extension subrack



90 01 60

4.2.1 Technical data

Positive Supply voltage U_{B1}	+5 V +/-5 %
Supply current I_{B1} to U_{B1} without a bus terminator	typically 0.8 A, max. 1.1 A
Supply current I_{B1} to U_{B1} with a bus terminator	typically 1.2 A, max. 1.5 A
Ambient temperature	0 °C ... +55 °C
Storage temperature	-25 °C ... +75 °C
Humidity rating	F
Mechanical stress	in accordance with VDE 160 when installed
Dimensions	1 pitch
Weight	1.0 kg
Order number	GJR5143200R1

Accessories

Bus coupler unit 35 EK 90 R1 for the extension subracks	GJR5143100R1
Connecting cable 35 SK 96 R1 for the bus coupler units	GJR5143700R1

4.2.2 Description

A basic subrack (master) is connected to a maximum of three extension subracks (slaves) by means of the bus coupler units 35 EK 90, 35 EK 91 and the connecting cable 35 SK 96. The subracks to be connected to each other are placed on top of each other. The lowest subrack is connected to a bus coupler unit 35 EK 90 (so that the installation of the above-mentioned fan is possible below) and is thus the basic subrack. The extension subracks are placed above this and equipped with one bus coupler unit 35 EK 91 each.

Note:
The maximum distance between the lower edges of the two subracks amounts to 240 mm caused by the length of the cable 35 SK 96.

The bus coupler unit 35 EK 91 is designed, so that only passive subscribers without an interrupt transfer can be included in the extension subrack.

The lines of the system cable 35 SK 96 and the connecting lines between the front plugs of the bus coupler units form a bus, the repeater bus. The repeater bus, as an open collector bus, must be terminated on the first and last bus coupler unit with resistors. Sub-printed boards, which can be plugged in, are used together with matching resistors. Two sub-printed boards are included as an addition to the delivery scope for the unit 35 EK 90.

The bus operations "reading " and "writing" are possible using the repeater bus.

ATTENTION:
In order to protect the bus coupler units from electrostatic contact, their non-occupied front plugs (X3 or X4) must be provided with dummy plugs. Two of these dummy plugs are also included in the delivery scope of the unit 35 EK 90.

4.2.3 Function

The unit 35 EK 90 extends the writing/reading cycle to 1.8 µs in order to achieve a safe method of transfer. The exchange of data in the I/O area of the MPST bus is only affected here.

The unit behaves like a passive subscriber with a $\overline{BOV}$/RDY delay of 1.8 µs, which occupies all the I/O addresses.

The repeater bus transfers the MPST bus signals A, D, $\overline{I/O}$, $\overline{R}$, $\overline{W}$, WO, $\overline{BOV}$, RDY.

Control signals for the bus drivers in the extension subracks (GTAS and GTDS (for slaves) or GTAM and GTDM (for masters) as gate signals for addresses and data).

The signals $\overline{PFD}$, CC, $\overline{RS}$ (MPST bus signals) as well as ADET and OUTINH (optional signals) can be addressed directly with the corresponding bus contacts using the jumper zone X6.

4.2.4 Example of a bus coupling

See section 4.4.

4.2.5 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

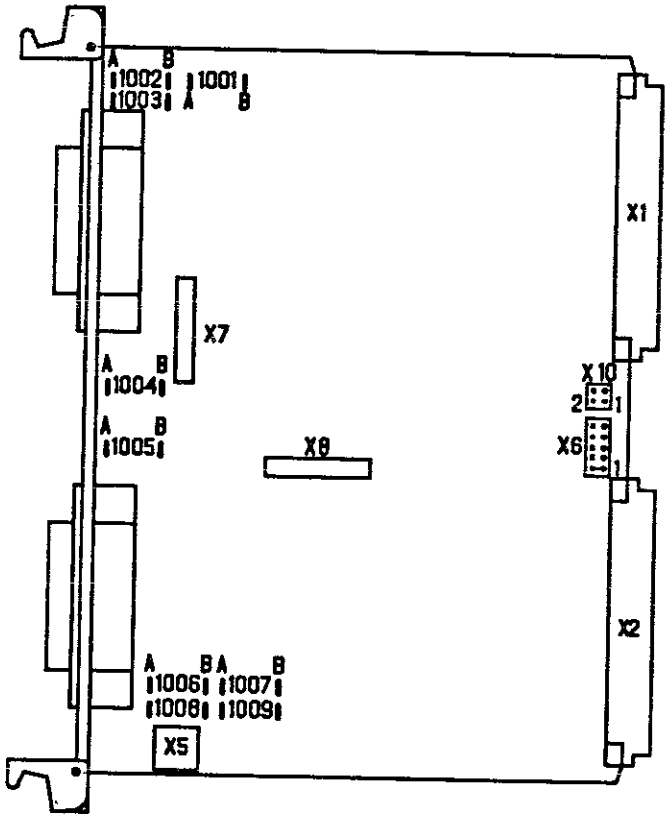


Fig. 4.2-1 Component side (top view)

The drawn jumpers correspond to the factory setting, see also section 4.2.6, Settings.

X 1, X 2	Plug connectors with MPST bus signals according to DIN 66264
X 3, X 4	Plug connectors (50-polar) for the repeater bus RB, system cable 35 SC 96 connection, provided with dummy plugs if not occupied
X 5	Optional 0 V terminal
X 6	Disconnectable connection for $\overline{PFD}$, $\overline{RS}$, CC, ADET, OUTINH to the repeater bus
X 7, X 8	Plugs for the matching resistors of the repeater bus
X 9	CC/internal clock switchover
X10	RDY control
1001 ... 1009	Wiring as required

4.2.6 Settings

(Standard setting of the unit is drawn each time)

READY signal setting **X10**:

X10: o 4 o 3 — Pull-Up for RDY to the MPST bus
o 2 o 1 — RDY is served by all the users

Various signal settings **X6**:

X6: 10 o o 9 OUTINH; 8 o o 7 ADET; 6 o o 5 $\overline{PFD}$; 4 o o 3 $\overline{RS}$; 2 o—o 1 CC

4.2.7 Soldering bridges for cable screens

The soldering bridges for the 0 V or the front panel connection of the cable screens of the system cable 35 SK 96 are shown in Fig. 4.2-2.

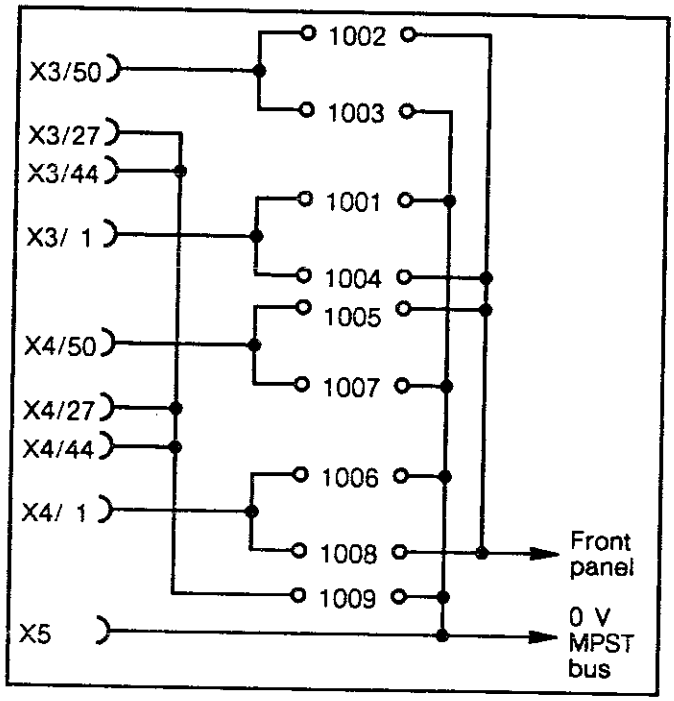
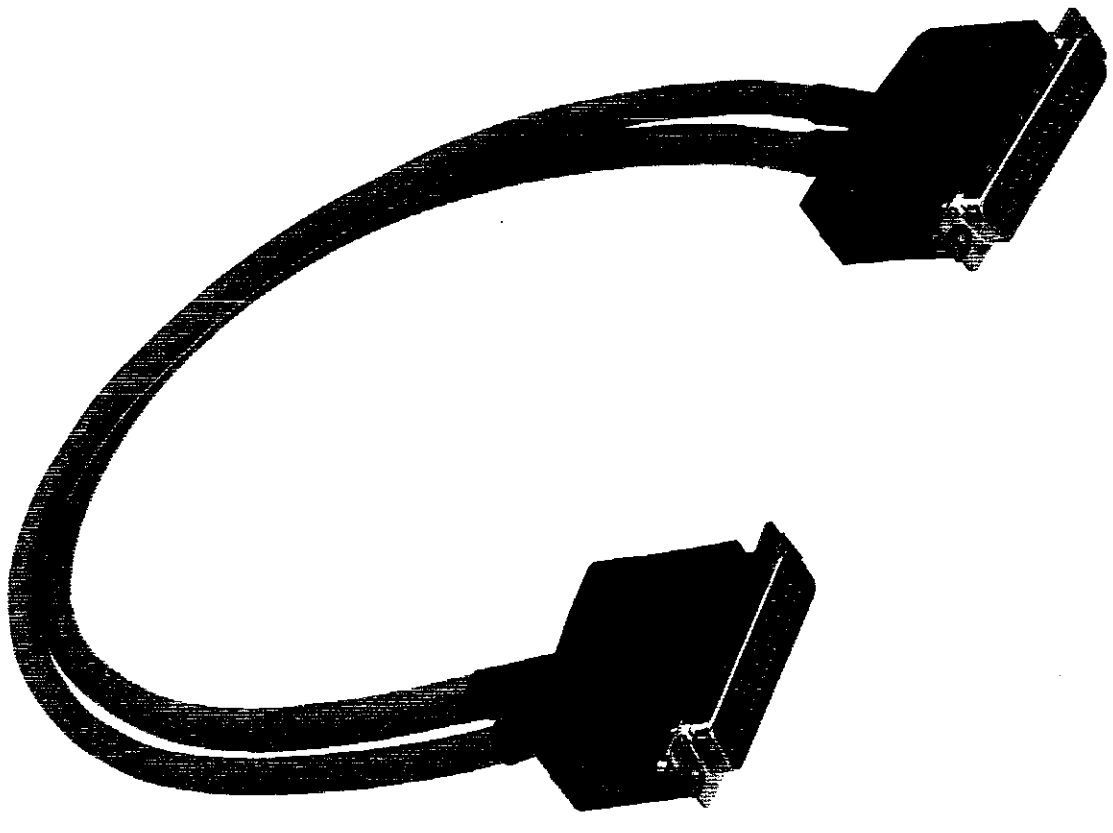


Fig. 4.2-2 Soldering bridges

The assignment of the plug connectors X3 and X4 is as follows:

X*/1	Sreen, cable 1
X*/27	0 V, cable 1
X*/44	0 V, cable 2
X*/50	Screen, cable 2

4.3 Connecting cable 35 SK 96 R1 for the bus coupler units



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4.3.1 Technical data

Cable with	SUB D plug, 50-polar
Weight	0.1 kg
Order number	GJR5143700R1

Accessories

Bus coupler unit 35 EK 90 R1 for the basic subrack	GJR5143100R1
Bus coupler unit 35 EK 91 R1 for the extension subrack	GJR5143200R1

4.3.2 Description

A basic subrack (master) is connected to a maximum of three extension subracks (slaves) by means of the bus coupler units 35 EK 90, 35 EK 91 and the connecting cable 35 SK 96. The subracks to be connected to each other are placed on top of each other. The lowest subrack is connected to a bus coupler unit 35 EK 90 (so that the installation of the above-mentioned fan is possible below) and is thus the basic subrack. The extension subracks are placed above this and equipped with one bus coupler unit 35 EK 91 each.

The lines of the system cable 35 SK 96 and the connecting lines between the front plugs of the bus coupler units form a bus, the repeater bus. The repeater bus, as an open collector bus, must be terminated on the first and last bus coupler unit with resistors. Sub printed boards, which can be plugged in, are used together with matching resistors.

The bus operations 'read' and 'write' are possible using the repeater bus.

The repeater bus transfers the ABB Procontic T300 control signals A, D, $\overline{I/O}$, $\overline{R}$, $\overline{W}$, WO, $\overline{BOV}$, RDY.

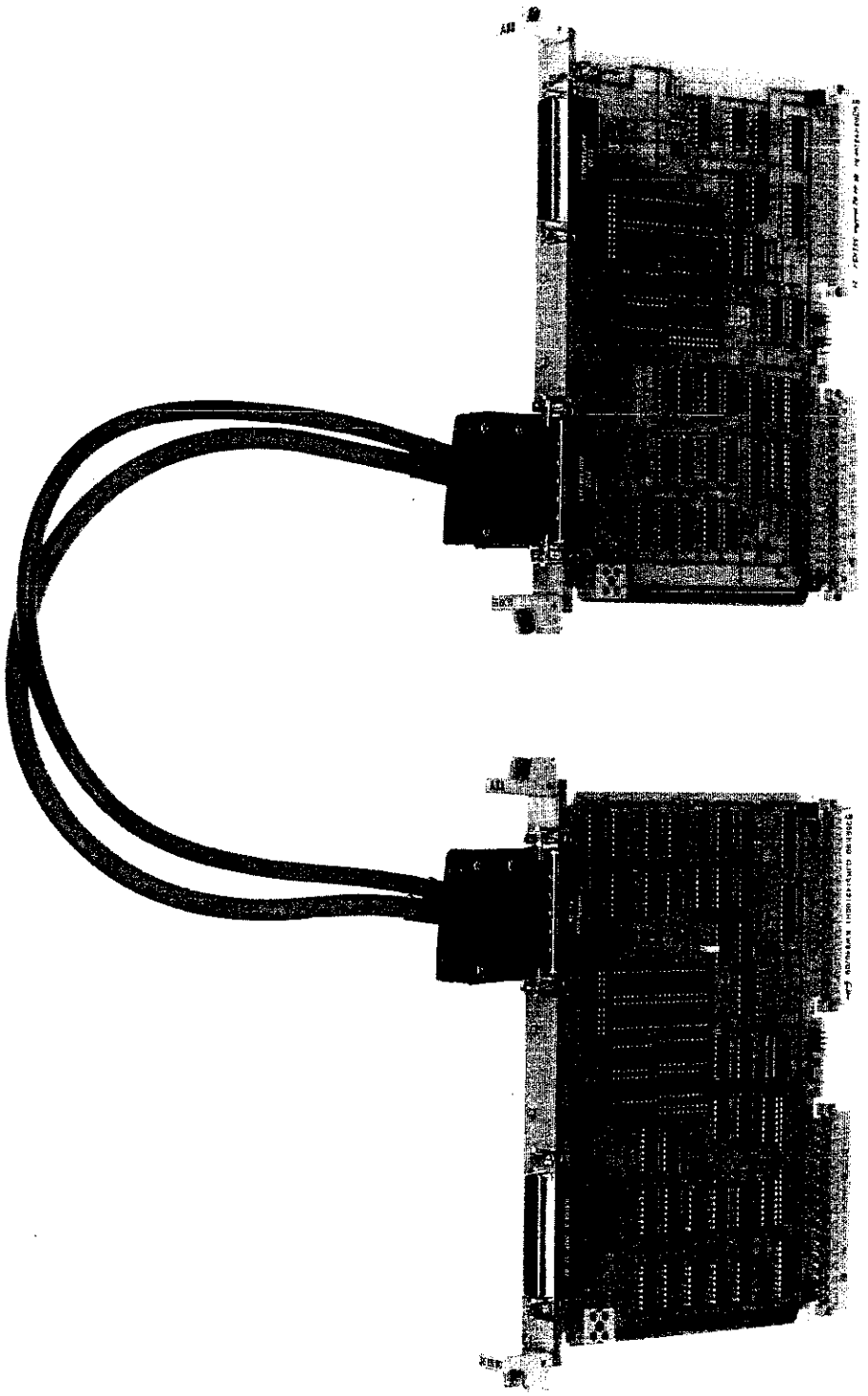
Control signals for the bus drivers in the extension subracks (GTAS and GTDS (for slaves) or GTAM and GTDM (for masters) as gate signals for addresses and data).

Note:
The maximum distance between the lower edges of the two subracks amounts to 240 mm caused by the length of the cable 35 SK 96.

4.3.3 Soldering bridges for cable screens

The soldering bridges for the 0 V or the front panel connection of the cable screens of the system cable 35 SK 96 are described in sections 4.1 and 4.2.

4.4 Example of a bus coupling with the bus coupler units 35 EK 90, 35 EK 91 and the connecting cable 35 SK 96



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4.4.1 Description

A basic subrack (master) is connected to a maximum of three extension subracks (slaves) by means of the bus coupler units 35 EK 90, 35 EK 91 and the connecting cable 35 SK 96. The subracks to be connected to each other are placed on top of each other. The lowest subrack is connected to a bus coupler unit 35 EK 90 (so that the installation of the above-mentioned fan is possible below) and is thus the basic subrack. The extension subracks are placed above this and equipped with one bus coupler unit 35 EK 91 each.

The bus coupler unit 35 EK 90 is designed, so that active and passive subscribers can be included in the basic subrack. Only passive subscribers without an interrupt transfer can be included in the extension subracks with the bus coupler units 35 EK 90.

The lines of the system cable 35 SK 96 and the connecting lines between the front plugs of the bus coupler units form a bus, the repeater bus. The repeater bus , as an open collector bus, must be terminated on the first and last bus coupler unit with resistors. Sub-printed boards, which can be plugged in, are used together with matching resistors. Two sub-printed boards are included as an addition to the delivery scope for the unit 35 EK 90.

The bus operations 'read' and 'write' are possible using the repeater bus.

ATTENTION:
In order to protect the bus coupler units from electrostatic contact, their non-occupied front plugs (X3 or X4) must be provided with dummy plugs. Two of these dummy plugs are also included in the delivery scope of the unit 35 EK 90.

4.4.2 Example

Example with three extension subracks for one basic subrack.

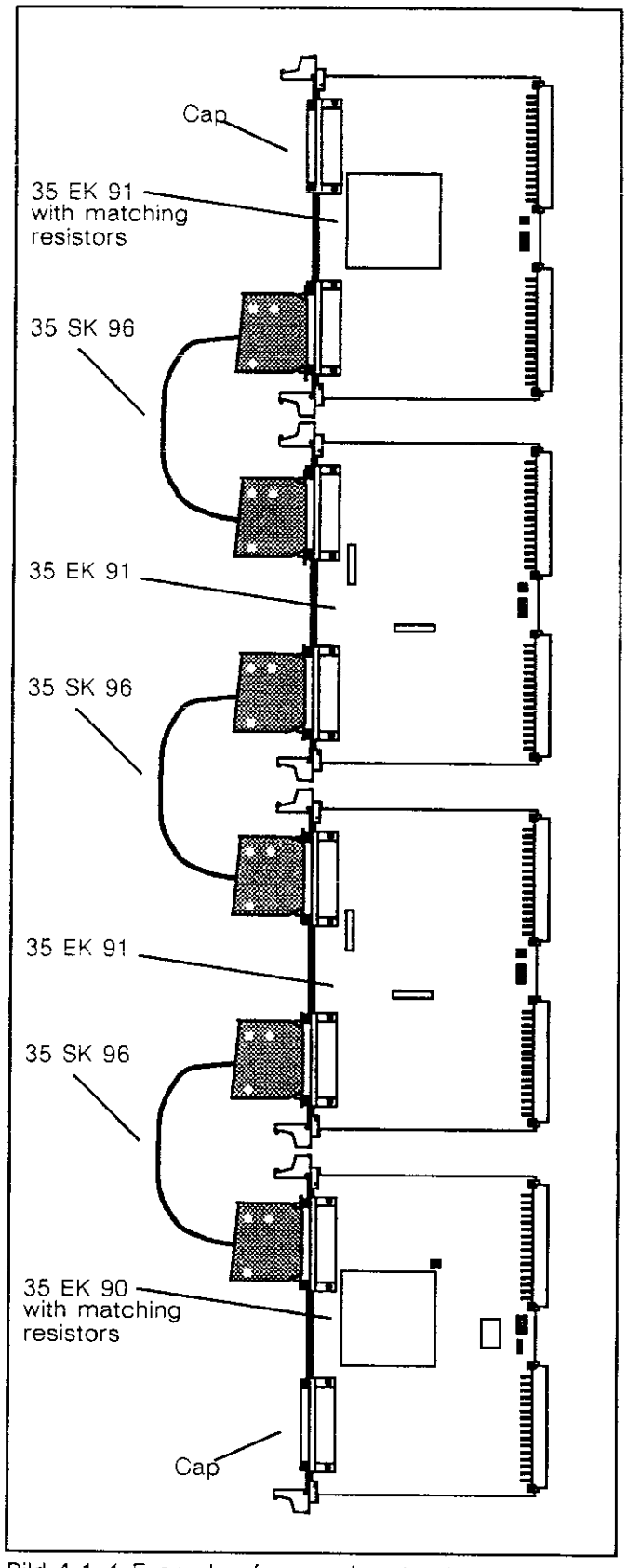

Bild 4.1-1 Example of a coupler structure

Note:
The maximum distance between the lower edges of two subracks amounts to 240 mm caused by the length of the cable 35 SK 96.

5 Processor cards

Processor card 35 PS 93 R11, equipped with 8086.
Processor card 35 PS 93 R21, equipped with 8086 and 8087.
Processor card 35 PS 93 R31, equipped with 8086.
Processor card 35 PS 93 R41, equipped with 8086 and 8087.

5.1	**Processor card 35 ZP 93 R11, R21**	**5.1- 1**
5.1.1	**Technical data**	**5.1- 2**
5.1.2	**Description**	**5.1- 2**
5.1.3	**Mechanical structure**	**5.1- 2**
5.1.4	**Plug assignment**	**5.1- 3**
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5.1.5.2	Wait State Logik	5.1- 6
5.1.5.3	DMA	5.1- 6
5.1.5.4	Memory	5.1- 6
5.1.5.5	Transfer memory	5.1- 6
5.1.5.6	MPST bus transfer	5.1- 7
5.1.5.7	I/O units	5.1- 8
5.1.5.8	Ready Time Out	5.1- 9
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5.1.5.10	Memory overview	5.1-10
5.1.5.11	NMI - non-masked Interrupt	5.1-10
5.1.6	**Timing**	**5.1-10**
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5.1.6.2	MPST bus access times	5.1-11
5.1.6.3	Transfer memory access times	5.1-11
5.1.7	**Settings**	**5.1-11**
5.1.7.1	CCU/AS	5.1-11
5.1.7.2	Transfer memory	5.1-11
5.1.7.3	Subscriber number and transfer memory address	5.1-11
5.1.7.4	RAM/EPROM	5.1-12
5.1.7.5	Wait state	5.1-12
5.1.7.6	MPST bus clock	5.1-12

5.2	**Prozessorkarte 35 ZP 93 R31, R41**	**5.2- 1**
5.2.1	**Technical data**	**5.2- 2**
5.2.2	**Description**	**5.2- 2**
5.2.3	**Mechanical structure**	**5.2- 2**
5.2.4	**Plug assignment**	**5.2- 3**
5.2.4.1	MPST bus interface, plugs X1, X2	5.2- 3
5.2.4.2	Wire wrap zone X3	5.2- 4
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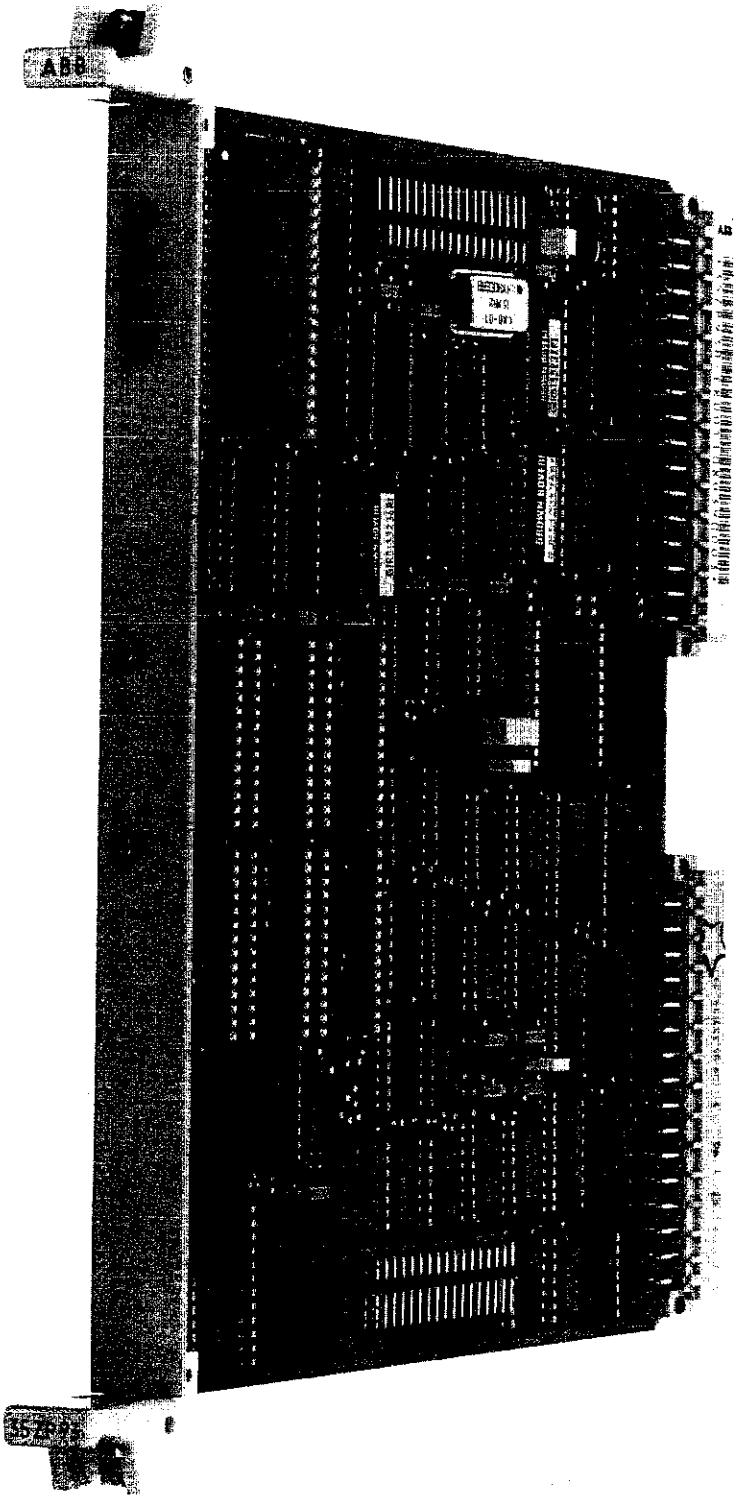
5.2.5	**Function and structure**	**5.2- 6**
5.2.5.1	CPU and NDP	5.2- 6
5.2.5.2	Wait State Logik	5.2- 6
5.2.5.3	DMA	5.2- 6
5.2.5.4	Memory	5.2- 6
5.2.5.5	Transfer memory	5.2- 6
5.2.5.6	MPST bus transfer	5.2- 7
5.2.5.7	I/O units	5.2- 8
5.2.5.8	Ready Time Out	5.2- 9
5.2.5.9	Frequency divider	5.2- 9
5.2.5.10	Memory overview	5.2-10
5.2.6	**Timing**	**5.2-10**
5.2.6.1	Internal access times	5.2-10
5.2.6.2	MPST bus access times	5.2-10
5.2.6.3	Transfer memory access times	5.2-10
5.2.7	**Settings**	**5.2-11**
5.2.7.1	CCU/AS	5.2-11
5.2.7.2	Transfer memory	5.2-11
5.2.7.3	User number and transfer memory address	5.2-11
5.2.7.4	RAM/EPROM	5.2-11
5.2.7.5	Wait state	5.2-12
5.2.7.6	MPST bus clock	5.2-12
5.2.8	**Model differences between 35 ZP 93 R31, R41 and 35 ZP 93 R11, R12**	**5.2-12**

5.1 Processor card 35 ZP 93 R11, R21



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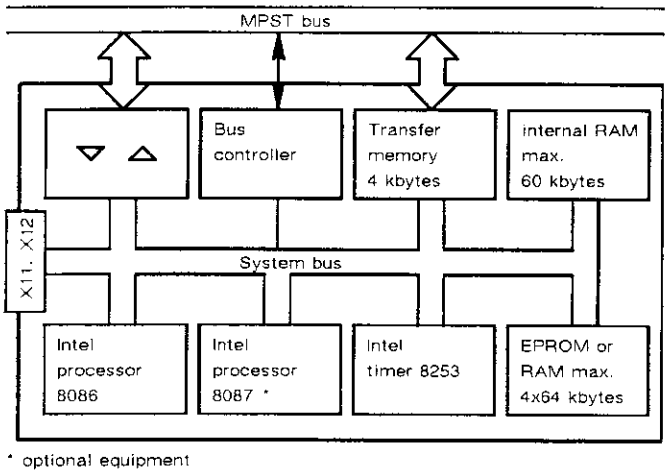
5.1.1 Technical data

Processor	8086
Co-Processor	8087 (only for rubric 21)
Supply voltage	5 V DC ± 5 %
Current input	2.8 A ± 20 %
Power loss	15 W ± 30 %
Frequency cycle	5 MHz
Ambient temperature	0 °C ... +55 °C
Storage temperature	-25 °C ... +75 °C
Humidity rating	F
Mechanical stress when installed	VDE 0160
Dimensions	1 pitch
Weight	0.4 kg
Order number 35 ZP 93 with 8086	GJR5133200R11
Order number 35 ZP 93 with 8086/8087	GJR5133200R21

5.1.2 Description

The central processor card 35 ZP 93 can be used as the central unit (CU) or as an active subscriber (AS) of the multiprocessor control system ABB Procontic T300. A coprocessor 8087 can be used as an option for a fast calculation of geometric data. The exchange of data between the 8086 and the 8087 is carried out via the local bus, between the 35 ZP 93 and the 35 DS 90 via the system bus and to other active or passive subscribers via the MPST bus. The card can process interrupts from the MPST bus and the system bus. 3 timers and several I/O ports are also freely available.



* optional equipment

Fig. 5.1-1 Block diagram

5.1.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

A maximum of two data interfaces 35 DS 90 or 35 DS 91 can be connected to the 35 ZP 93.

The drawn jumpers correspond to the factory setting; see also section 5.1.7, Settings.

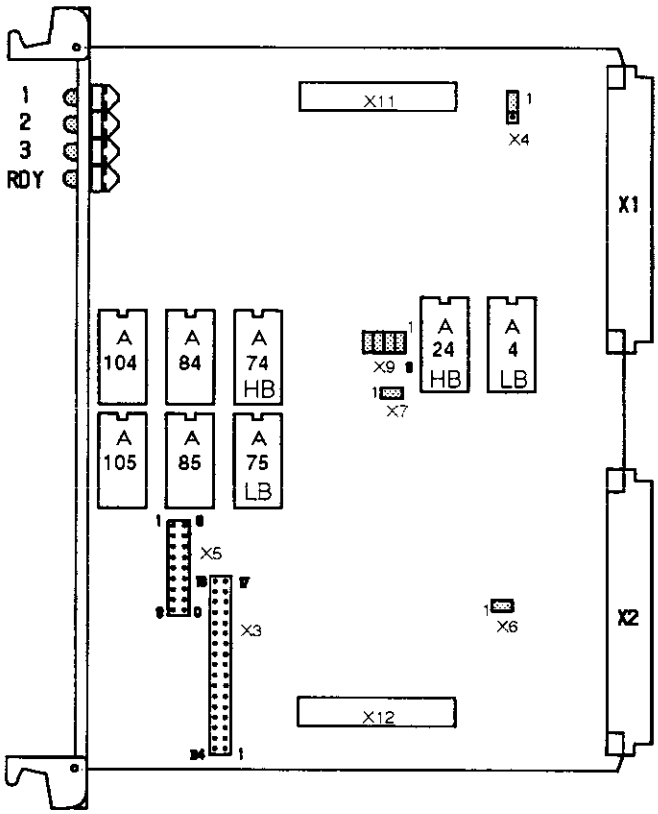


Fig. 5.1-2 Component side (top view)

Code	Interface, plug	Design	Pole
X 1	MPST-Bus	DIN41612, Part 2 constr. form C	32
X 2	MPST-Bus	DIN41612, Part 2 constr. form C	32
X 3	Interrupt, clock, I/O port, T300 signals	Wire-Wrap	34
X 4	Size of the transfer memory	Jumper field	3
X 5	RAM/EPROM equipment	Wire-Wrap	18
X 6	CCU or an active subscriber	Jumper field	2
X 7	Wait states	Jumper field	2
X 9	Subscriber number	Jumper field	8
X11	System bus (to 35 DS 90, 35 DS 91)	Ribbon cable	34
X12	System bus (to 35 DS 90, 35 DS 91)	Ribbon cable	34

5.1.4 Plug assignment

5.1.4.1 MPST bus interface, plugs X1, X2

All inputs of the interfaces X1 and X2 have a fan in of max. IiH = 0.04 mA; IiL = 1.6 mA.

All the outputs of the interfaces X1 and X2 have a fan out of max. IoH = – 0.4 mA; IoL = 16 mA.

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	U B3	– 15 V voltage	X1. 6c	U B2	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{\text{PFD}}$	Power Failure Detect
X1.26a	–	–	X1.26c	–	–
X1.28a	$\overline{\text{BB}}$	Bus Busy	X1.28c	$\overline{\text{RBB}}$	Reset Bus Busy
X1.30a	$\overline{\text{SRQ}}$	Service Request	X1.30c	$\overline{\text{HSRQ}}$	Hold Status SRQ
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	SYNC	Synchronisation signal	X2.20c	CC	Central Clock
X2.22a	–	–	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O–memory area	X2.26c	–	–
X2.28a	$\overline{\text{DMARQ}}$	DMA Request	X2.28c	DMACK	DMA Acknowledge
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

5.1.4.2 Wire wrap zone X3

Various inputs and outputs can be wired up with the I/O units in this wrap zone: timers, interrupt controllers and I/O ports.

Pin	Signal	Meaning	Pin	Signal	Meaning
X3. 1	IR6	IR6 input	X3.18	$\overline{\text{RBB}}$	MPST bus signal
X3. 2	IR7	IR7 input	X3.19	QE	I/O output port
X3. 3	CLK1	Clock timer 1	X3.20	QH/LED1	I/O output port
X3. 4	GT1	Gate timer 1	X3.21	QH/LED2	I/O output port
X3. 5	Out1	Out timer 1	X3.22	QH/LED3	I/O output port
X3. 6	CLK2	Clock timer2	X3.23	DMACK	MPST bus signal
X3. 7	GT2	Gate timer 2	X3.24	IND1	I/O input D1
X3. 8	Out2	Out timer 2	X3.25	IND2	I/O input D2
X3. 9	OSC	15 MHz cycle	X3.26	$\overline{\text{IND3}}$	I/O input D3
X3.10	CK	5 MHz cycle	X3.27	$\overline{\text{SYNC}}$	Central clock
X3.11	PCLK	2.5 MHz cycle	X3.28	0 V	0 V voltage
X3.12	CL1	7.5 MHz cycle	X3.29	DEX	X12. 5 line
X3.13	CL2	1.5 MHz cycle	X3.30	CEX	X12.31 line
X3.14	CL3	0.75 MHz cycle	X3.31	BEX	X12. 3 line
X3.15	$\overline{\text{CL4}}$	0.15 MHz cycle	X3.32	AEX	X12.29 line
X3.16	$\overline{\text{DMARQ}}$	MPST bus signal	X3.33	CC	MPST bus clock
X3.17	$\overline{\text{IR3}}$	IR3 input	X3.34	HIGH	High level

5.1.4.3 System bus

The system bus of the processor card 35 ZP 93 may be loaded with a maximum of two data interfaces 35 DS 90 or 35 DS 91.

The ribbon cable and the mechanical parts required to connect the processor card and data interface are supplied with each data interface.

Plug X11:

Pin	Signal	Meaning	Pin	Signal	Meaning
X11. 1	$\overline{\text{MRDC}}$	Memory read	X11.18	–	–
X11. 2	$\overline{\text{IORC}}$	I/O read	X11.19	–	–
X11. 3	$\overline{\text{MWTC}}$	Memory write	X11.20	U B1	5 V voltage
X11. 4	A01	Address bit 01	X11.21	A01	Address bit 01
X11. 5	A03	Address bit 03	X11.22	A18	Address bit 18
X11. 6	A05	Address bit 05	X11.23	A16	Address bit 16
X11. 7	A07	Address bit 07	X11.24	A14	Address bit 14
X11. 8	A09	Address bit 09	X11.25	A12	Address bit 12
X11. 9	A11	Address bit 11	X11.26	A10	Address bit 10
X11.10	A13	Address bit 13	X11.27	A08	Address bit 08
X11.11	A15	Address bit 15	X11.28	A06	Address bit 06
X11.12	A17	Address bit 17	X11.29	A04	Address bit 04
X11.13	A19	Address bit 19	X11.30	A02	Address bit 02
X11.14	HLDA	Hold Acknowledge	X11.31	A00	Address bit 00
X11.15	U B1	5 V voltage	X11.32	Reserved	Special applications
X11.16	–	–	X11.33	$\overline{\text{AIOWC}}$	I/O write
X11.17	–	–	X11.34	Reserved	Special applications

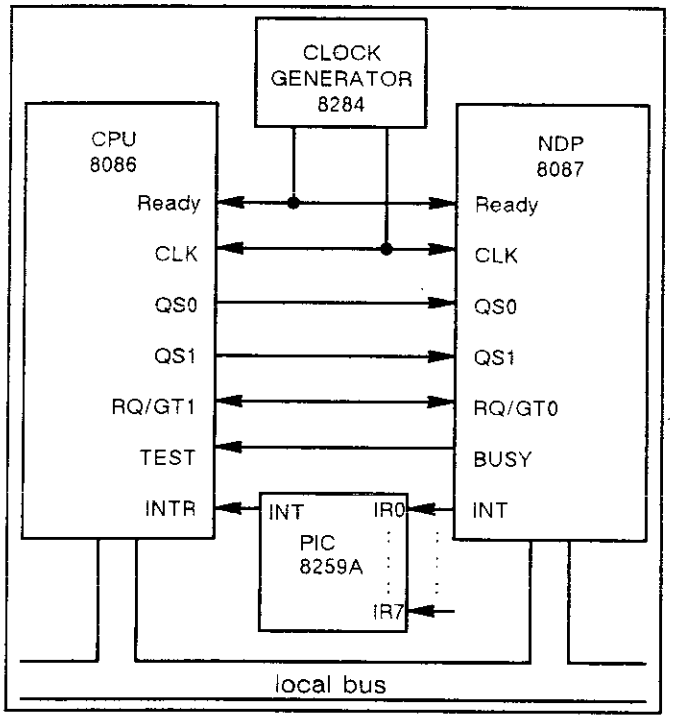
Stecker X12:

Pin	Signal	Meaning	Pin	Signal	Meaning
X12. 1	0 V	0 V voltage	X12.18	–	–
X12. 2	ALE	Address Latch Enable	X12.19	–	–
X12. 3	BEX	B exp. line	X12.20	D14	Data bit 14
X12. 4	$\overline{\text{RES}}$	Reset from 8284A	X12.21	D12	Data bit 12
X12. 5	DEX	D exp. line	X12.22	D10	Data bit 10
X12. 6	CAS0	CAS 0 of the 8259A	X12.23	D08	Data bit 08
X12. 7	CAS1	CAS 1 of the 8259A	X12.24	D06	Data bit 06
X12. 8	D01	Data bit 01	X12.25	D04	Data bit 04
X12. 9	D03	Data bit 03	X12.26	D02	Data bit 02
X12.10	D05	Data bit 05	X12.27	D00	Data bit 00
X12.11	D07	Data bit 07	X12.28	$\overline{\text{INTA}}$	Intr. Acknowledge
X12.12	D09	Data bit 09	X12.29	AEX	A exp. line
X12.13	D11	Data bit 11	X12.30	RDYi	Ready internally
X12.14	D13	Data bit 13	X12.31	CEX	C exp. line
X12.15	D15	Data bit 15	X12.32	$\overline{\text{M/IO}}$	Memory I/O mode
X12.16	–	–	X12.33	HOLD	Hold request
X12.17	–	–	X12.34	0 V	0 V voltage

5.1.5 Function and structure

5.1.5.1 CPU and NDP

The processor 8086 is used as a CPU and the numerical processor 8087 for numerical calculations. The processor 8086 is run in the MAX mode. The processor and coprocessor are connected via the local bus. The arbitration of the local bus is controlled via a RQ/GT line. The busy test line serves as the ready message of the coprocessor to the host processor. The interrupt output of the coprocessor is switched to the IR input of the interrupt controller 8259A.



5.1-3 CPU with a numerical processor

5.1.5.2 Wait State Logic

If slow memories are used, the access times of which are greater than two clock cycles (400 ns for the 5 MHz CPU clock), a wait cycle can be inserted. The jumper X7 must be opened here. Each access is extended in this way by one clock cycle.

5.1.5.3 DMA

The processor card can be brought into the HOLD status via the system bus. The HOLD line and the HLDA line are guided to the plugs X11 and X12. The HOLD request is provided with a LOCK cycle. The CPU is switched to the WAIT state with HLDA. The bus controller 8288 (A62), the address latches 74 LS 373 (A71, A72, A83) and the data drivers 74 LS 245 (A93, A103) are switched to inactive with the signal AEN.

5.1.5.4 Memory

6 assembly positions are available (three 28-polar sockets each for the HIGH and LOW bytes). The assembly positions are already designed for a maximum memory capacity of 64 kbytes (27512). The memory type (RAM, EPROM) and the memory capacity are set by wire-wrap connections to the plug X5.

5.1.5.5 Transfer memory

The transfer memory is designed as a dual port RAM and can be addressed by the MPST and by the system bus. If the transfer memory is addressed by one side and another side also has access to it, the latter goes into the WAIT state, until the former has finished its access. The safe entry of data, which belong together (e.g. a double word), is to be secured by a software semaphore. The guarantee is made active by putting the LOCK prefix before the corresponding command (e.g., LOCK XCHG AX, ES:SPHR). The memory size normally amounts to 4 kbytes but can be extended to 16 kbytes or 64 kbytes. There is a limitation, that only 4 kbytes can be addressed by the MPST bus at any time.

Addressing the transfer memory by the MPST bus is carried out by generating the subscriber no. and the byte no. (see also DIN 66 264, part 1 and part 2). The subscriber no. consists of 5 bits, 4 bits of which are to be set on the unit (X9). The 5th bit selects the upper or lower half of the transfer memory.

The memory capacity belonging to one subscriber number is 2 kbytes (A10...A0).

MPST bus transfer memory : Dual Port RAM

System bus 8086 address area: 10000 ... 1FFFF

Bit sample for addressing the transfer memory by the MPST bus:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
X	X	X	X	Y	0	0	0	0	0	0	0	0	0	0	0
Subscriber's address					Address byte in the subscriber's area										

Subscriber's area:
Y = 0, Even numbered subscriber's area 0, 2, 4 ... 30
Y = 1, Odd numbered subscriber's area 1, 3, 5 ... 31

If the word 0 is written into the transfer memory by the MPST bus, this initiates an interrupt (IR4 for Y = 0, IR5 for Y = 1). The interrupt is reset by reading the corresponding word.

Attention:

A defined output status must be produced by reading the two words (1000:0H, 1000:800H) after switching ON the mains voltage.

5.1.5.6 MPST bus transfer

The multiprocessor-based bus transfer is carried out in 2 levels. The interrupt treatment, for which an interrupt vector of 8 bits is output to the CCU is processed with first priority.

The bus transfer foreseen for the 35 ZP 93 (direct bus mode) allows a multiprocessing, for which the bus arbitration is carried out according to the geometric priority (the slot on the extreme right-hand side has the highest priority). The bus arbitration is carried out by the bus controller as far as the hardware is concerned. The CCU is responsible for supplying the clock for the MPST bus when in the direct bus mode.

The CCU is the same as an active subscriber in the bus transfer. The CCU has the highest priority and must be located on the extreme right in the subrack.

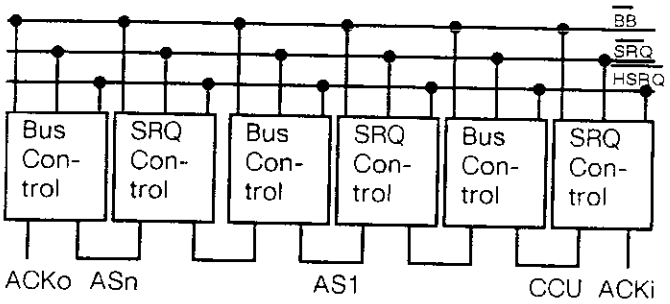


Fig. 5.2-4 Control signals for the bus transfer

The central processor card 35 ZP 93 is also capable of working together with processor units, for which the bus arbitration occurs by the software (indirect bus mode). The use of the 35 ZP 93 in the indirect bus mode is also possible as an active subscriber.

Direct bus mode

The central processor card is installed for the direct bus mode after the hardware reset (I/O port 12H = 0).

Interrupt treatment in the direct bus mode:

An SRQ vector can be output in the direct bus mode. The SRQ exchange of data can only be carried out in the direct or indirect bus modes.

Exchange of data in the direct bus mode:

If the CPU wishes to carry out an exchange of data via the MPST bus, this leads to a bus request (BRQ) by the bus controller, which subsequently interrupts the ACK line. A test takes place in the following clock cycles, whether the bus was returned ($\overline{BB}$ = 1). If the $\overline{BB}$ line is inactive and the ACK line active, the bus is accepted (switching on the data, addresses, producing the $\overline{BOV}$ signal). The processor is in the WAIT state during the time between the bus request until the bus arbitration ($\overline{BB}$ = 0). A subscriber with a low priority must wait for a bus arbitration, until the subscriber with the higher priority has finished its bus cycle. A subscriber with a lower priority can block itself against a bus transfer to a subscriber with a higher priority by setting the LOCK signal.

The MPST bus is obtained by the system bus from the following addresses:

MPST bus active subscribers	30000 ... 3FFFF
MPST bus passive subscribers	20000 ... 2FFFF

Attention:

If the MPST bus is occupied by, for example, a command:

LOCK MOVE mem, reg ; move string via the MPST bus without an interruption, other active subscribers cannot obtain the bus for the length of the command execution. The monitoring for Ready Time Out can be prompted.

Indirect bus mode

Interrupt treatment in the indirect bus mode:

If an active subscriber wishes to output an interrupt vector, it enters this in the SRQ output latch (I/O address 20H) with an OUT command. The SRQ line is activated in this way, and the CCU answers with $\overline{HSRQ}$ and by setting the ACK line. The SRQ vector is read. ACK and $\overline{HSRQ}$. The active subscriber can check that the SRQ vector has been received by testing the bit 7 of the I/O input port (I/O address 10H).

Bit 7 = 0	SRQ vector has not yet been read by the CCU
Bit 7 = 1	SRQ vector has been read by the CCU,
SRQ latch	free for a new vector

Using the 35 ZP 93, it is possible to carry out the SRQ transfer in the indirect bus mode and to operate the data transfer in the direct bus mode at the same time.

Exchange of data in the indirect bus mode:

If an active subscriber wishes to carry out an exchange of data via the MPST bus, it registers this by outputting an SRQ vector to the central unit. The central unit grants its permission for the bus transfer with a software entry. The active subscriber sets its I/O port (12H = 1) and generates the MPST bus address. Several writing or reading cycles can be carried out without returning the bus. The bus is returned by resetting the I/O port (12H = 0). The CCU can interrupt the current bus cycle of an active subscriber by setting $\overline{RBB}$ = 0.

The signal $\overline{RBB}$ can be defined as the interrupt IR3 or as an I/O input in the plug zone X3. A return request of the MPST bus can then be processed by the CCU. If the interrupt is set, this must be activated before the bus access.

5.1.5.7 I/O units

Timer 8253

Various programming types of the timers 1 and 2 are possible with the plug zone X3. The timer 0 is permanently set for the Ready Time Out monitoring. More details concerning the programming of the timer are to be taken from the data sheet of the 8253.

I/O address: 80H Data: D07 ... D00

Address	Function
80	Timer 0
82	Timer 1
84	Timer 2
86	Control word

Interrupt Controller 8259A

The interrupt controller is connected to the system bus as an I/O device. The interrupt requests are read by the 8259A and handed on to the CPU as interrupt requests according to their priority. The CPU reads the vector prepared by the 8259A during the INTA cycle. The vector points to the interrupt vector table, in which the segment and the instruction pointer of the respective interrupt service routine are located.

The codes of the interrupt inputs are as follows:

IR Input	Function	Signal name
IR0	Interrupt by the Co-Processor 8087	IR87
IR1	Ready Time Out	TOUT
IR2	Read interrupt vector	SRQ1
IR3	For free use, primarily for the 2nd 35 DS 90 or 35 DS 91	$\overline{IR3}$ (X3.17)
IR4	Word 0 of the 1st half of the transfer memory	IRW0
IR5	Word 0 of the 2nd half of the transfer memory	IRW1
IR6	For free use	IR6 (X3.1)
IR7	For free use, primarily for the 1st 35 DS 90 or 35 DS 91	$\overline{IR7}$ (X3.2)

I/O address 40H Data: D07 ... D00

Address	Function
40	IRR, ISR, ICW1, OCW2, OCW3
42	IMR, OCW1, ICW2, ICW, ICW4

SRQ sending and reception register

The SRQ function to receive is only active when operating the unit as a CCU (X6.1-2 connected). A unit switched as an active subscriber or as a CCU can use its SRQ sending register. The SRQ vector is output by the SRQ controller with the entry in the SRQ sending register (address 20H). The SRQ controller of the CCU stores this vector. The CCU can read the vector from the SRQ reception register (adress 20H). If the 35 ZP 93 is being used as a CCU, the vector entered in the SRQ sending register is entered in the SRQ reception register by the SRQ controller via the MPST bus. The vector sends itself an SRQ vector, so that the vector can be read again under the address 20H, e.g., the card is a CCU.

SRQ sending register
I/O address: 20H
Data: D07 ... D00

SRQ reception register
I/O address: 20H
Data: D07 ... D00 (only connected for X6.1-2)

I/O output port 74259

The I/O output port serves to control various functions and the LEDs on the front panel of the 35 ZP 93. The port is selected (A01 ... A03) and the status output with the data bit D00.

The outputs are assigned in the following way:

I/O Address	Function with D0 = 1	Signal name
10	Activate Ready Time Out	TOE
12	Indirect bus mode	BM
14	$\overline{SYNC}$ = 0 on the MPST bus	SYNC
16	$\overline{DMARQ}$ = 0 on the MPST bus	DMARQ
18	For free use	QE (X3.19)
1A	LED1 'on' and free use	QE, LED1 (X3.20)
1C	LED2 'on' and free use	QE, LED2 (X3.21)
1E	LED3 'on' and free use	QE, LED3 (X3.22)

I/O input port 74 LS 373

The input port is a transparent latch, the data of which can be constantly read at the output. The status of the inputs are frozen, when the Ready Time Out monitoring addressed, and can then be read by the CPU.

I/O address: 10H Data: D07 ... D00

Data bit	Function	Signal name
D0	MPST bus occupied	DMACK
D1	for free use	IND1 (X3.24)
D2	for free use	IND2 (X3.25)
D3	for free use	IND3 (X3.26)
D4	MPST bus busy	$\overline{BB}$
D5	Dual port RAM request	$\overline{RRAM}$
D6	MPST bus request	$\overline{BRQ}$
D7	SRQ Vector output	$\overline{SRQO}$

5.1.5.8 Ready Time Out

The Ready TIme Out monitoring enables a defined interruption of the system in the case of an error. A time between 0 and 533 ms can be set by programming the timer 0. The timer 0 must be programmed in mode 2 (see data sheet of the 8253). The Ready Time Out monitoring is activated by setting the I/O output port (10H = 1).

If the processor is kept in the WAIT state for longer than the set time, the Ready Time Out monitoring is addressed and produces a ready signal for the processor, which is independent of all status, and an interrupt (IR1). The status are frozen at the same time at the inputs of the I/O input port (address 10H). The I/O input port is first read in the following interrupt routine, the resulting instructions are then carried out, e.g., error message to the CCU. If the Ready Time Out monitoring is then activated again, an "0" and then a "1" must be output via the I/O output port address 10H.

5.1.5.9 Frequency divider

Various frequencies are available for the timers and the MPST bus clock (CC) in the wrap zone X3. The frequency data can be taken from the plug assignment X3.

5.1.5.10 Memory overview

Address	Unit / medium	Position	Process mode	Address	Unit / medium	Position	Process mode
FFFF	Reserved for			4FFFF	EPROM	A84	
	extension units			.	or		
.	like, e.g.,			40000	RAM	A85	
009X	35 DS 90, 35 DS 91			3FFFF	MPST bus		
008X	timer 8253	A87	I/O	.			
004X	interrupt controller	A106		30000	active subscribers		
	8259A			2FFFF	MPST bus		Memory
0020	SRQ vektor	A 8,A18		.			
001X	input/output port	A77,A86		20000	passive subscribers		
FFFFF	EPROM	A74		1FFFF		A 4	
.	or			.	transfer memory		
E0000	RAM	A75	Memory	10000		A24	
DFFFF	memory capacity reser-		0FFFF	EPROM	A104		
.	ved for units, like, e.g.,		.	or			
5000	35 DS 90, 35 DS 91		00000	RAM	A105		

Only for a configuration with a max. of two 35 DS 90

5.1.5.11 NMI - non-masked interrupt

The NMI of the CPU 8086 is guided to the signal line $\overline{PFD}$ (Power Failure Detect).
A suitable interrupt service routine is foreseen for processing the NMI.

5.1.6 Timing

The tolerance of all the times amounts to ±10 %

5.1.6.1 Internal access times

Signal	Time (ns)		Clock number		Meaning
	without Wait	with Wait	without Wait	with Wait	
$\overline{MRDC}$	400	600	2	3	read memory
$\overline{MWTC}$	200	400	1	2	write memory
$\overline{IORC}$	400	600	2	3	read I/O
$\overline{AIOWC}$	400	600	2	3	write I/O

5.1.6.2 MPST bus access times

The times refer to a MPST bus clock of CC = 2.4 MHz and a free bus ($\overline{BB}$ = 1).

Signal	Time (ns)	Meaning
$\overline{R}$	1458	read
$\overline{W}$	1458	write
$\overline{BOV}$ (R)	1040	bus data valid
$\overline{HSRQ}$	800	interrupt treatment

5.1.6.3 Transfer memory access times

The times refer to an MPST bus clock of CC = 2.4 MHz and a free transfer memory.

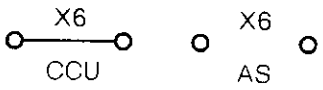
Signal	Time (ns)	Meaning
$\overline{\overline{MRDC}}$	1200	internal read
$\overline{\overline{MWTC}}$	1000	internal write
$\overline{\overline{R}}$	1400	MPST bus reads
$\overline{\overline{W}}$	1400	MPST bus writes

5.1.7 Settings

5.1.7.1 CCU/AS

The setting of the processor unit as a CCU or an active subscriber is carried out with the plug X6. If the processor is being used as a CCU, it produces the MPST bus clock. If the processor is being used as an active subscriber, in which the CCU is not a processor card 35 ZP 93, it must be guaranteed, that an MPST bus clock (CC ≤ 5 MHz) is made available.

Jumper **X6**:



Note:
Only **one** processor card 35 ZP 93 with the jumper X6 may be operated per ABB Procontic T300.

5.1.7.2 Transfer memory

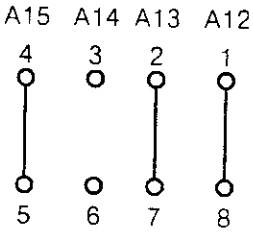
The size of the transfer memory dependent on the assembly can be set with the plug X4. If a larger transfer memory than 4 kbytes is equipped, attention is to be paid but only 4 kbytes can be obtained by the MPST bus. The transfer memory is obtained internally independent of the MPST subscriber number starting from 1000:H. The memory address is repeated depending on the memory size, e.g., the same memory cell is always addressed when using HM6116P-2 with the addresses 1000:0H, 1000:1000H, 1000:2000H etc..

Jumper zone **X4**:

5.1.7.3 Subscriber number and transfer memory address

The subscriber number is set with the plug X9. The subscriber number consists of the upper 5 address bits, the upper 4 bits of which can be set on the 35 ZP 93. Byte 5 in the transfer memory of the example mentioned below is obtained by another active subscriber (AS) with the following address: 3000:4005H.

Jumper zone **X9**:



X9 set address: 4XXXH

The transfer memory is always obtained by the internal CPU under the addresses

1000:0000H ... 1000:0FFFH := 10000H ... 10FFFH.

5.1.7.4 RAM/EPROM

The type and size of the memory ICs can be wired up to the plug X5 for 2 assembly positions each. A 20-polar socket is available for each of the memory positions A74, A75, A84, A85, A104, A105. If an IC is used with only a 24-polar casing, pins 1 - 2 and 27 - 28 in the socket remain free!

The numbers given in the above table describe the pins of the socket X5. If, for example, position A104, A105 should be equipped with an EPROM 2716, X5.2 must be connected to X5.13 and X5.3 to X5.13.

Position			EPROM					RAM		
A104 A105	A84 A84	A74 A75	2716	2732	2764	27128	27256	6116	6264	43256
1	5	9	–	–	13	13	13	–	–	18
2	6	10	13	16	16	16	16	14	16	16
3	7	11	13	13	–	17	17	13	13	17
4	8	12	–	–	13	13	18	–	14	14

The assignment is as follows:

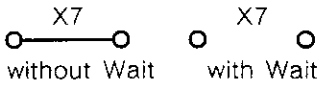
Position		Address area
High byte	Low byte	
A104 A 84 A 74	A106 A 85 A 75	0000:0 ... 0000:FFFF 4000:0 ... 4000:FFFF E000:0 ... E000:FFFF

5.1.7.5 Wait State

An additional clock cycle can be set for slow memory media. The setting is carried out with X7.

Attention: A wait cycle is inserted for all the bus accesses!

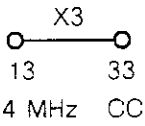
Jumper **X7**:



5.1.7.6 MPST bus clock

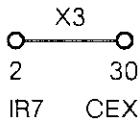
For a CPU clock of 5 MHz:

Jumper zone **X3**:



Interrupt of the data interface

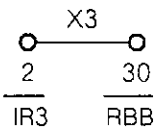
Jumper zone **X3**:



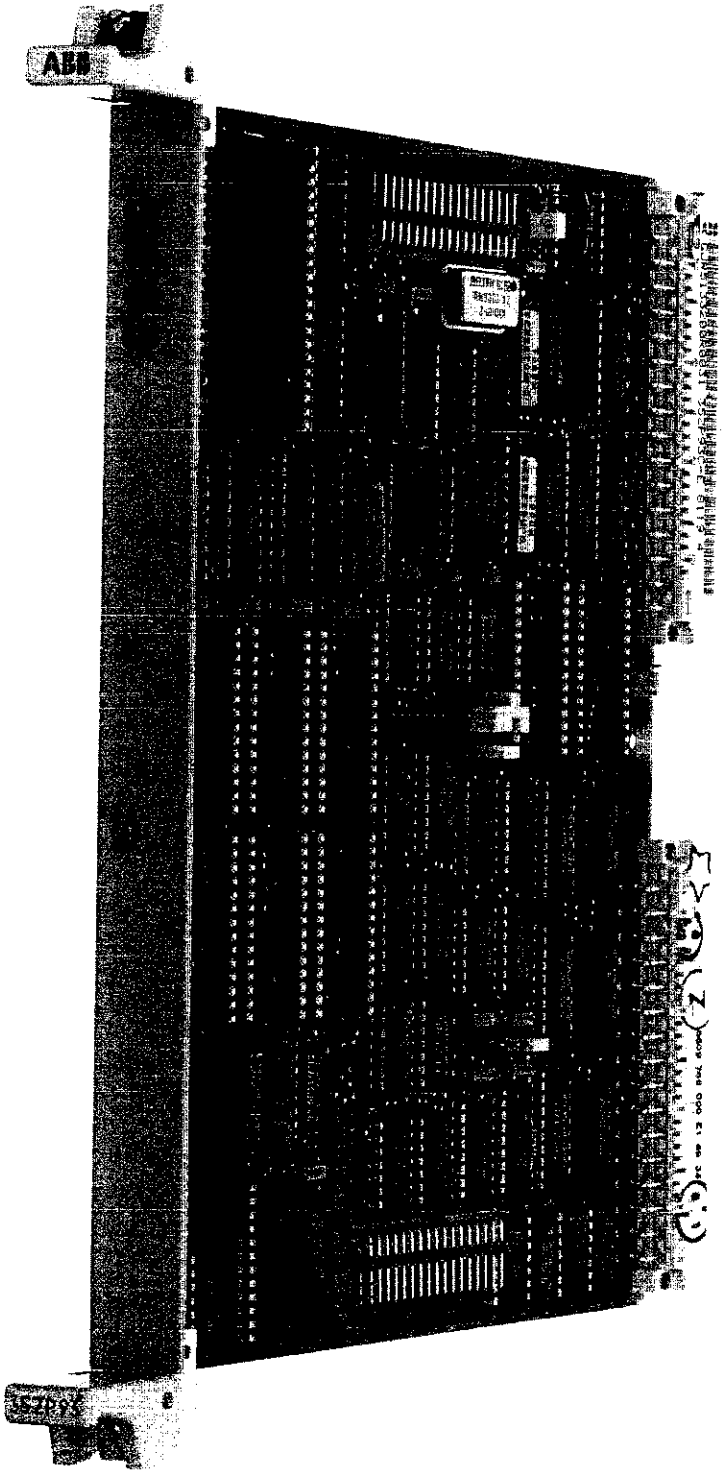
Interrupt by $\overline{\text{RBB}}$

The CCU must have the possibility of moving the active subscriber currently on the bus by sending $\overline{\text{RBB}}$ = 0 for the return of the bus. This takes place in the indirect bus mode. This requires the subscriber, who receives the bus to demask IR3 and the IR3 pin to connect with $\overline{\text{RBB}}$.

Jumper zone **X3**:



5.2 Processor card 35 ZP 93 R31, R41



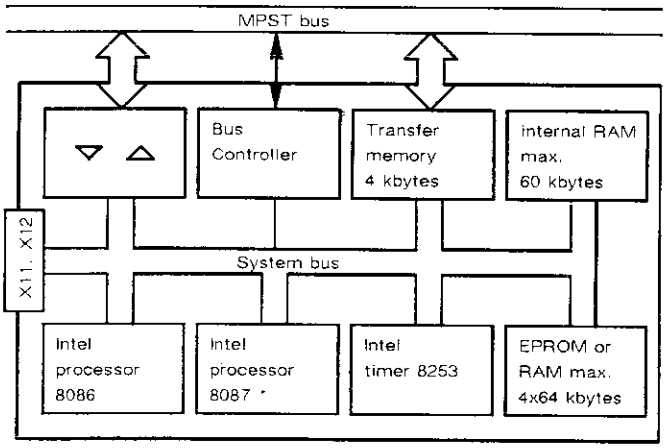
90 01 67

5.2.1 Technical data

Processor	8086
Co-processor	8087 (only for rubric 41)
Supply voltage	5 V DC ± 5 %
Current input	2.8 A ± 20 %
Power loss	15 W ± 30 %
Clock frequency	8 MHz
Ambient temperature	0 °C ... +55 °C
Storage temperature	-25 °C ... +75 °C
Humidity rating	F
Mechanical stress when installed	VDE 0160
Dimensions	1 pitch
Weight	0.4 kg
Order nummer 35 ZP 93 with 8086	GJR5133200 R31
Order nummer 35 ZP 93 with 8086/8087	GJR5133200 R41

5.2.2 Description

The central processor card 35 ZP 93 can be used as the central unit (CU) or as an active subscriber (AS) of the multiprocessor control system ABB Procontic T300. A coprocessor 8087 can be used as an option for a fast calculation of geometric data. The exchange of data between the 8086 and the 8087 is carried out via the local bus, between the 35 ZP 93 and the 35 DS 90 via the system bus and to other active or passive subscribers via the MPST bus. The card can process interrupts from the MPST bus and the system bus. 3 timers and several I/O ports are also freely available.



* optional equipment

Fig. 5.2-1 Block diagram

5.2.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

A maximum of two data interfaces 35 DS 90 or 35 DS 91 can be connected to the 35 ZP 93.

The drawn jumpers correspond to the factory settings; see also section 5.2.7, Settings.

Attention:
The slots may not be equipped with the segment address 4000H on the 35 DS 90!

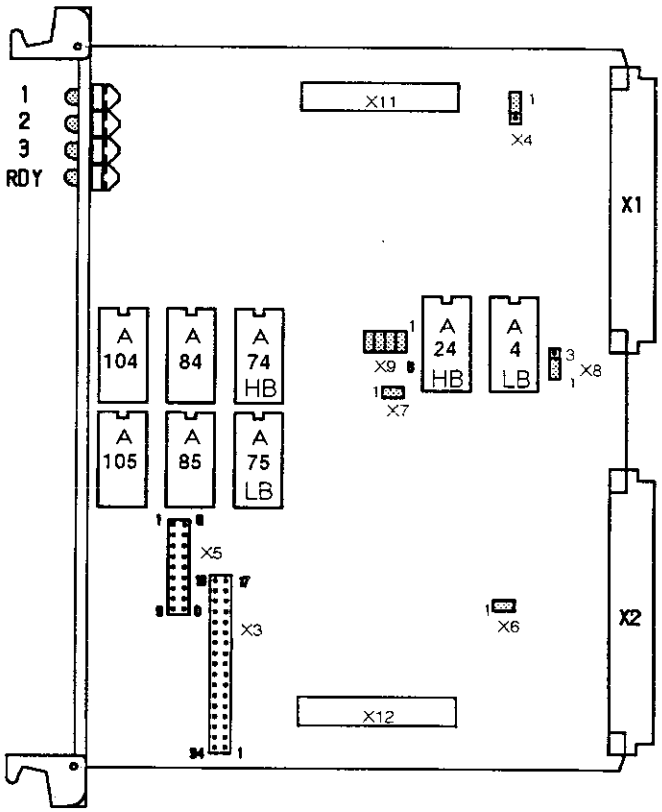


Fig. 5.2-2 Component side (top view)

Code	Interface, plug	Design	Pole
X 1	MPST bus	DIN41612, Part 2 constr. form C	32
X 2	MPST bus	DIN41612, Part 2 constr. form C	32
X 3	Interrupt, clock, I/O-port, T300 bus signals	Wire-Wrap	34
X 4	Size of the transfer memory (RAM)	Jumper field	3
X 5	RAM/EPROM equipment	Wire-Wrap	18
X 6	CCU or an active subscriber	Jumper field	2
X 7	Wait states	Jumper field	2
X 8	Size of the transfer memory (RAM)	Jumper field	3
X 9	Subscriber's number	Jumper field	8
X11	System bus (to 35 DS 90, 35 DS 91)	Ribbon cable	34
X12	System bus (to 35 DS 90, 35 DS 91)	Ribbon cable	34

5.2.4 Plug assignment

5.2.4.1 MPST bus interface, plugs X1, X2

All inputs of the interfaces X1 and X2 have a fan in of max. IiH = 0.04 mA; IiL = 1.6 mA.

All the outputs of the interfaces X1 and X2 have a fan out of max. IoH = - 0.4 mA; IoL = 16 mA.

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	U B3	- 15 V voltage	X1. 6c	U B2	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{PFD}$	Power Failure Detect
X1.26a	-	-	X1.26c	-	-
X1.28a	$\overline{BB}$	Bus Busy	X1.28c	$\overline{RBB}$	Reset Bus Busy
X1.30a	$\overline{SRQ}$	Service Request	X1.30c	$\overline{HSRQ}$	Hold status SRQ
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{BOV}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	SYNC	Synchronisation signal	X2.20c	CC	Central Clock
X2.22a	-	-	X2.22c	$\overline{RS}$	Reset
X2.24a	$\overline{W}$	Write	X2.24c	$\overline{R}$	Read
X2.26a	$\overline{I/O}$	I/O memory area	X2.26c	-	-
X2.28a	$\overline{DMARQ}$	DMA Request	X2.28c	DMACK	DMA Acknowledge
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

5.2.4.2 Wire wrap zone X3

Various inputs and outputs can be wired up with the I/O units in this wrap zone: timers, interrupt controllers and I/O ports.

Pin	Signal	Meaning	Pin	Signal	Meaning
X3. 1	IR6	IR6 input	X3.18	$\overline{\text{RBB}}$	MPST bus signal
X3. 2	IR7	IR7 input	X3.19	QE	I/O output port
X3. 3	CLK1	Clock timer 1	X3.20	QH/LED1	I/O output port
X3. 4	GT1	Gate timer 1	X3.21	QH/LED2	I/O output port
X3. 5	Out1	Out timer 1	X3.22	QH/LED3	I/O outport port
X3. 6	CLK2	Clock timer 2	X3.23	DMACK	MPST bus signal
X3. 7	GT2	Gate timer 2	X3.24	IND1	I/O input D1
X3. 8	Out2	Out timer 2	X3.25	IND2	I/O input D2
X3. 9	OSC	15 MHz cycle	X3.26	$\overline{\text{IND3}}$	I/O input D3
X3.10	CK	5 MHz cycle	X3.27	$\overline{\text{SYNC}}$	Central clock
X3.11	PCLK	2.5 MHz cycle	X3.28	0 V	0 V voltage
X3.12	CL1	7.5 MHz cycle	X3.29	DEX	X12. 5 line
X3.13	CL2	1.5 MHz cycle	X3.30	CEX	X12.31 line
X3.14	CL3	0.75 MHz cycle	X3.31	BEX	X12. 3 line
X3.15	$\overline{\text{CL4}}$	0.15 MHz cycle	X3.32	AEX	X12.29 line
X3.16	$\overline{\text{DMARQ}}$	MPST bus signal	X3.33	CC	MPST bus clock
X3.17	$\overline{\text{IR3}}$	IR3 input	X3.34	HIGH	High level

5.2.4.3 System bus

The system bus of the processor card 35 ZP 93 may be loaded with a maximum of two data interfaces 35 DS 90 or 35 DS 91.

The ribbon cable and the mechanical parts required to connect the processor card and data interface are supplied with each data interface.

Plug X11:

Pin	Signal	Meaning	Pin	Signal	Meaning
X11. 1	$\overline{\text{MRDC}}$	Memory read	X11.18	–	–
X11. 2	$\overline{\text{IORC}}$	I/O read	X11.19	–	–
X11. 3	$\overline{\text{MWTC}}$	Memory write	X11.20	UB1	5 V voltage
X11. 4	A01	Address bit 01	X11.21	A01	Address bit 01
X11. 5	A03	Address bit 03	X11.22	A18	Address bit 18
X11. 6	A05	Address bit 05	X11.23	A16	Address bit 16
X11. 7	A07	Address bit 07	X11.24	A14	Address bit 14
X11. 8	A09	Address bit 09	X11.25	A12	Address bit 12
X11. 9	A11	Address bit 11	X11.26	A10	Address bit 10
X11.10	A13	Address bit 13	X11.27	A08	Address bit 08
X11.11	A15	Address bit 15	X11.28	A06	Address bit 06
X11.12	A17	Address bit 17	X11.29	A04	Address bit 04
X11.13	A19	Address bit 19	X11.30	A02	Address bit 02
X11.14	HLDA	Hold Acknowledge	X11.31	A00	Address bit 00
X11.15	UB1	5 V voltage	X11.32	$\overline{\text{AEN}}$	Adress Enable
X11.16	–	–	X11.33	$\overline{\text{AIOWC}}$	I/O write
X11.17	–	–	X11.34	$\overline{\text{DEN}}$	Data Enable

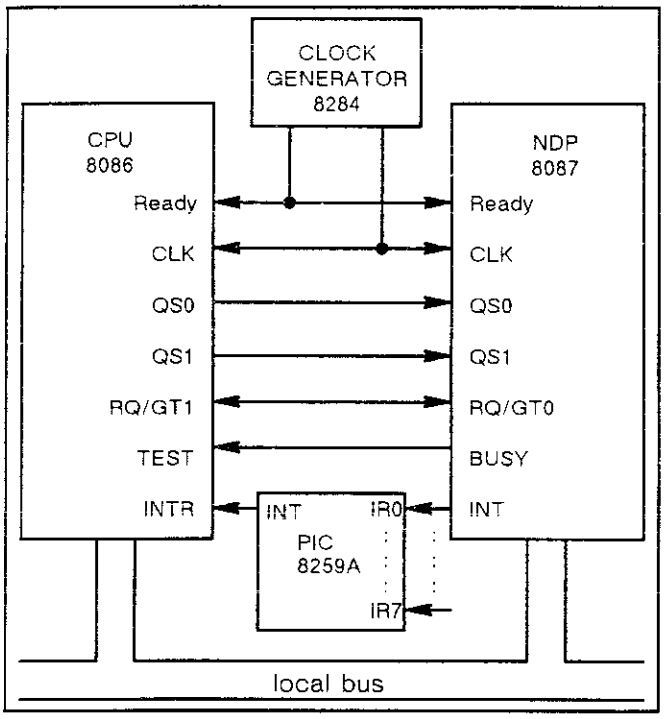
Stecker X12:

Pin	Signal	Meaning	Pin	Signal	Meaning
X12. 1	0 V	0 V voltage	X12.18	–	–
X12. 2	ALE	Address Latch Enable	X12.19	–	–
X12. 3	BEX	B exp. line	X12.20	D14	Data bit 14
X12. 4	$\overline{\text{RES}}$	Reset from 8284A	X12.21	D12	Data bit 12
X12. 5	DEX	D exp. line	X12.22	D10	Data bit 10
X12. 6	CAS0	CAS 0 of the 8259A	X12.23	D08	Data bit 08
X12. 7	CAS1	CAS 1 of the 8259A	X12.24	D06	Data bit 06
X12. 8	D01	Data bit 01	X12.25	D04	Data bit 04
X12. 9	D03	Data bit 03	X12.26	D02	Data bit 02
X12.10	D05	Data bit 05	X12.27	D00	Data bit 00
X12.11	D07	Data bit 07	X12.28	$\overline{\text{INTA}}$	Intr. acknowledge
X12.12	D09	Data bit 09	X12.29	AEX	A exp. line
X12.13	D11	Data bit 11	X12.30	RDYi	Ready internally
X12.14	D13	Data bit 13	X12.31	CEX	C exp. line
X12.15	D15	Data bit 15	X12.32	M/$\overline{\text{IO}}$	Memory I/O mode
X12.16	–	–	X12.33	$\overline{\text{HOLD}}$	Hold request
X12.17	–	–	X12.34	0 V	0 V voltage

5.2.5 Function and structure

5.2.5.1 CPU und NDP

The processor 8086 is used as a CPU and the numerical processor 8087 for numerical calculations. The processor 8086 is run in the MAX mode. The processor and coprocessor are connected via the local bus. The arbitration of the local bus is controlled via an RQ/GT line. The busy test line serves as the ready message of the coprocessor to the host processor. The interrupt output of the coprocessor is switched to the IR input of the interrupt controller 8259A.



5.2-3 CPU with a numerical processor

5.2.5.2 Wait State Logik

If slow memories are used, the access times of which are greater than two clock cycles (250 ns for the 8 MHz CPU clock), a wait cycle can be inserted. The jumper X7 must be opened here. Each access is extended in this way by one clock cycle.

5.2.5.3 DMA

The processor card can be brought into the HOLD status via the system bus. The HOLD line and the HLDA line are guided to the plugs X11 and X12. The HOLD request is provided with a LOCK cycle. The CPU is switched to the WAIT state with HLDA. The bus controller 8288 (A62), the address latches 74 LS 373 (A71, A72, A83) and the data drivers 74 LS 245 (A93, A103) are switched to inactive with the signal AEN.

5.2.5.4 Memory

6 assembly positions are available (three 28-polar sockets each for the HIGH and LOW bytes). The assembly positions are already designed for a maximum memory capacity of 64 KBytes (27512). The memory type (RAM, EPROM) and the memory capacity are set by wire-wrap connections to the plug X5.

Attention:
If the module is used together with 35 DS 90, the memory area 40000H ... 4FFFFH on the 35 DS 90 may not be equipped.

5.2.5.5 Transfer memory (RAM)

The transfer memory is designed as a dual port RAM and can be addressed by the MPST and by the system bus. If the transfer memory is addressed by one side and another side also has access to it, the latter goes into the WAIT state, until the former has finished its access. The safe entry of data, which belong together (e.g. a double word), is to be secured by a software semaphore. The guarantee is made active by putting the LOCK prefix before the corresponding command (e.g., LOCK XCHG AX, ES:SPHR). The memory size normally amounts to 4 KBytes but can be extended to 16 KBytes or 64 KBytes. There is a limitation, that only 4 KBytes can be addressed by the MPST bus at any time.

Addressing the transfer memory by the MPST bus is carried out by generating the subscriber no. and the byte no. (see also DIN 66 264, part 1 and part 2). The subscriber no. consists of 5 bits, 4 bits of which are to be set on the unit (X9). The 5th bit selects the upper or lower half of the transfer memory.

The memory capacity belonging to one subscriber number is 2 Kbytes (A10...A0).

MPST bus transfer memory : Dual Port RAM

System bus 8086 address area: 10000 ... 1FFFF

Bit sample for addressing the transfer memory by the MPST bus:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
X	X	X	X	Y	0	0	0	0	0	0	0	0	0	0	0
Subscriber's address					Address byte in the subscriber's area										

Subscriber's area:
Y = 0, Even numbered subscriber's area 0, 2, 4 ... 30
Y = 1, Odd numbered subscriber's area 1, 3, 5 ... 31

If the word 0 is written into the transfer memory by the MPST bus, this initiates an interrupt (IR4 for Y = 0, IR5 for Y = 1). The interrupt is reset by reading the corresponding word.

Attention:

A defined output status must be produced by reading the two words (1000:0H, 1000:800H) after switching ON the mains voltage.

5.2.5.6 MPST bus transfer

The multiprocessor-based bus transfer is carried out in 2 levels. The interrupt treatment, for which an interrupt vector of 8 bits is output to the CCU is processed with first priority.

The bus transfer foreseen for the 35 ZP 93 (direct bus mode) allows a multiprocessing, for which the bus arbitration is carried out according to the geometric priority (the slot on the extreme right-hand side has the highest priority). The bus arbitration is carried out by the bus controller as far as the hardware is concerned. The CCU is responsible for supplying the clock for the MPST bus when in the direct bus mode.

The CCU is the same as an active subscriber in the bus transfer. The CCU has the highest priority and must be located on the extreme right in the subrack.

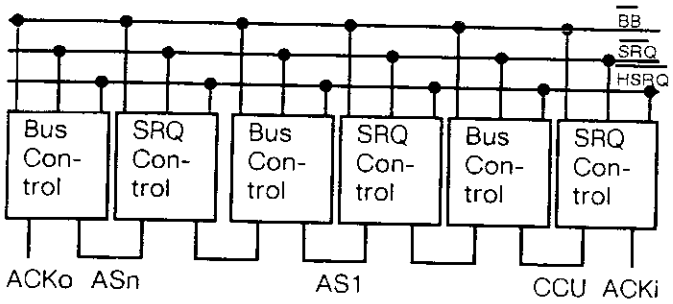


Fig. 5.2-4 Control signals for the bus transfer

The central processor card 35 ZP 93 is also capable of working together with processor units (e.g., 35 ZE 93 and 35 ZE 94), for which the bus arbitration occurs by the software (indirect bus mode). The use of the 35 ZP 93 in the indirect bus mode is also possible as an active subscriber.

Direct bus mode

The central processor card is installed for the direct bus mode after the hardware rest (I/O port 12H = 0).

Interrupt treatment in the direct bus mode:

An SRQ vector can be output in the direct bus mode. The SRQ exchange of data can only be carried out in the direct or indirect bus modes.

Exchange of data in the direct bus mode:

If the CPU wishes to carry out an exchange of data via the MPST bus, this leads to a bus request (BRQ) by the bus controller, which subsequently interrupts the ACK line. A test takes place in the following clock cycles, whether the bus was returned ($\overline{BB}$ = 1). If the $\overline{BB}$ line is inactive and the ACK line active, the bus is accepted (switching on the data, addresses, producing the $\overline{BOV}$ signal). The processor is in the WAIT state during the time between the bus request until the bus arbitration ($\overline{BB}$ = 0). A subscriber with a low priority must wait for a bus arbitration, until the subscriber with the higher priority has finished its bus cycle. A subscriber with a lower priority can block itself against a bus transfer to a subscriber with a higher priority by setting the LOCK signal.

The MPST bus is obtained by the system bus from the following addresses:

MPST bus active subscribers	30000 ... 3FFFF
MPST bus passive subscribers	20000 ... 2FFFF

Attention:

If the MPST bus is occupied by, for example, a command:

LOCK MOVE mem, reg ; move string via the MPST bus without an interruption, other active subscribers cannot obtain the bus for the length of the command execution. The monitoring for Ready Time Out can be prompted.

Indirect bus mode

Interrupt treatment in the indirect bus mode:

If an active subscriber wishes to output an interrupt vector, it enters this in the SRQ output latch (I/O address 20H) with an OUT command. The SRQ line is activated in this way, and the CCU answers with $\overline{HSRQ}$ and by setting the ACK line. The SRQ vector is read. ACK and $\overline{HSRQ}$. The active subscriber can check that the SRQ vector has been received by testing the bit 7 of the I/O input port (I/O address 10H).

Bit 7 = 0	SRQ vector has not yet been read by the CCU
Bit 7 = 1	SRQ vector has been read by the CCU,
SRQ latch	free for a new vector

Using the 35 ZP 93, it is possible to carry out the SRQ transfer in the indirect bus mode and to operate the data transfer in the direct bus mode at the same time.

Exchange of data in the indirect bus mode:

If an active subscriber wishes to carry out an exchange of data via the MPST bus, it registers this by outputting an SRQ vector to the central unit. The central unit grants its permission for the bus transfer with a software entry. The active subscriber sets its I/O port (12H = 1) and generates the MPST bus address. Several writing or reading cycles can be carried out without returning the bus. The bus is returned by resetting the I/O port (12H = 0). The CCU can interrupt the current bus cycle of an active subscriber by setting $\overline{RBB}$ = 0.

The signal $\overline{RBB}$ can be defined as the interrupt IR3 or as an I/O input in the plug zone X3. A return request of the MPST bus can then be processed by the CCU. If the interrupt is set, this must be activated before the bus access.

5.2.5.7 I/O units

Timer 8253

Various programming types of the timers 1 and 2 are possible with the plug zone X3. The timer 0 is permanently set for the Ready Time Out monitoring. More details concerning the programming of the timer are to be taken from the data sheet of the 8253.

I/O address: 80H Data: D07 ... D00

Address	Function
80	Timer 0
82	Timer 1
84	Timer 2
86	Control word

Interrupt Controller 8259A

The interrupt controller is connected to the system bus as an I/O device. The interrupt requests are read by the 8259A and handed on to the CPU as interrupt requests according to their priority. The CPU reads the vector prepared by the 8259A during the INTA cycle. The vector points to the interrupt vector table, in which the segment and the instruction pointer of the respective interrupt service routine are located.

The codes of the interrupt inputs are as follows:

T

IR Input	Function	Signal name
IR0	Interrupt by the Co-Processor 8087	IR87
IR1	Ready Time Out	TOUT
IR2	Read interrupt vector	SRQ1
IR3	For free use, primarily for the 2nd 35 DS 90 or 35 DS 91	$\overline{IR3}$ (X3.17)
IR4	Word 0 of the 1st half of the transfer memory	IRW0
IR5	Word 0 of the 2nd half of the transfer memory	IRW1
IR6	For free use	IR6 (X3.1)
IR7	For free use, primarily for the 1st 35 DS 90 or 35 DS 91	$\overline{IR7}$ (X3.2)

I/O address 40H Data: D07 ... D00

Address	Function
40	IRR, ISR, ICW1, OCW2, OCW3
42	IMR, OCW1, ICW2, ICW, ICW4

SRQ sending and reception register

The SRQ function to receive is only active when operating the unit as a CCU (X6.1-2 connected). A unit switched as an active subscriber or as a CCU can use its SRQ sending register. The SRQ vector is output by the SRQ controller with the entry in the SRQ sending register (address 20H). The SRQ controller of the CCU stores this vector. The CCU can read the vector from the SRQ reception register (adress 20H). If the 35 ZP 93 is being used as a CCU, the vector entered in the SRQ sending register is entered in the SRQ reception register by the SRQ controller via the MPST bus. The vector sends itself an SRQ vector, so that the vector can be read again under the address 20H, e.g., the card is a CCU.

SRQ sending register
I/O address: 20H
Data: D07 ... D00

SRQ reception register
I/O address: 20H
Data: D07 ... D00 (only connected for X6.1-2)

I/O output port 74259

The I/O output port serves to control various functions and the LEDs on the front panel of the 35 ZP 93. The port is selected (A01 ... A03) and the status output with the data bit D00.

The outputs are assigned in the following way:

I/O Address	Function with D0 = 1	Signal name
10	Activate Ready Time Out	TOE
12	Indirect bus mode	BM
14	SYNC = 0 on the MPST bus	$\overline{\text{SYNC}}$
16	DMARQ = 0 on the MPST bus	$\overline{\text{DMARQ}}$
18	For free use	QE (X3.19)
1A	LED1 'on' and free use	QE, LED1 (X3.20)
1C	LED2 'on' and free use	QE, LED2 (X3.21)
1E	LED3 'on' and free use	QE, LED3 (X3.22)

I/O input port 74 LS 373

The input port is a transparent latch, the data of which can be constantly read at the output. The status of the inputs are frozen, when the Ready Time Out monitoring is addressed, and can then be read by the CPU.

I/O address: 10H Data: D07 ... D00

Data bit	Function	Signal name
D0	MPST bus occupied	DMACK
D1	for free use	IND1 (X3.24)
D2	for free use	IND2 (X3.25)
D3	for free use	IND3 (X3.26)
D4	MPST bus occupied	$\overline{\text{BB}}$
D5	Dual port RAM request	$\overline{\text{RRAM}}$
D6	MPST bus request	$\overline{\text{BRQ}}$
D7	SRQ Vector output	$\overline{\text{SRQO}}$

5.2.5.8 Ready Time Out

The supervision of the ready time out enables a defined interruption of the system in the case of an error. A time between 0 and 533 ms can be set by programming the timer 0. The timer 0 must be programmed in mode 2 (see data sheet of the 8253). The Ready Time Out monitoring is activated by setting the I/O output port (10H = 1).

If the processor is kept in the WAIT state for longer than the set time, the Ready Time Out monitoring is addressed and produces a ready signal for the processor, which is independent of all status, and an interrupt (IR1). The status are frozen at the same time at the inputs of the I/O input port (address 10H). The I/O input port is first read in the following interrupt routine, the resulting instructions are then carried out, e.g., error message to the CCU. If the Ready Time Out monitoring is then activated again, an "0" and then a "1" must then be output via the I/O output port address 10H.

5.2.5.9 Frequency divider

Various frequencies are available for the timers and the MPST bus clock (CC) in the wrap zone X3. The frequency data can be taken from the pin assignment X3.

5.2.5.10 Memory overview

Address	Unit / medium	Position	Process mode	Address	Unit / medium	Position	Process mode
FFFF	reserved for			4FFFF	EPROM	A84	
	extension units			.	or		
.	like, e.g.,			40000	RAM	A85	
009X	35 DS 90, 35 DS 91			3FFFF	MPST bus		
008X	timer 8253	A87	I/O	.			
004X	interrupt controller	A106		30000	active subscribers		
	8259A			2FFFF	MPST bus		Memory
0020	SRQ vektor	A 8,A18		.			
001X	input/output port	A77,A86		20000	passive subscribers		
FFFFF	EPROM	A74		1FFFF		A 4	
.	or			.	transfer memory		
E0000	RAM	A75	Memory	10000		A24	
DFFFF	memory capacity reserv-		0FFFF	EPROM	A104		
.	ed for units, like, e.g.,			.	or		
5000	35 DS 90, 35 DS 91			00000	RAM	A105	

Only for a configuration with a maximum of two interface units.

5.2.6 Timing

The tolerance of all the times amounts to ±10 %

5.2.6.1 Internal access times

signal	time (ns)		clock number		meaning
	without Wait	with Wait	without Wait	with Wait	
$\overline{MRDC}$	400	600	2	3	read memory
$\overline{MWTC}$	200	400	1	2	write memory
$\overline{IORC}$	400	600	2	3	read I/O
$\overline{AIOWC}$	400	600	2	3	write I/O

5.2.6.2 MPST bus access times

The times refer to a MPST bus clock of CC = 2.4 MHz and a free bus ($\overline{BB}$ = 1).

signal time (ns) meaning

Signal	Time (ns)	Meaning
$\overline{R}$	1167	read
$\overline{W}$	1167	write
$\overline{BOV}$ ($\overline{W}$)	720	bus data valid
$\overline{BOV}$ ($\overline{R}$)	527	bus data valid
$\overline{HSRQ}$	800	interrupt treatment

5.2.6.3 Transfer memory access times

The times refer to a MPST bus clock of CC = 2.4 MHz and a free transfer memory.

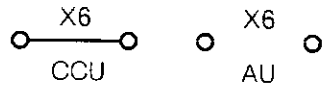
Signal	Time (ns)	Meaning
$\overline{MRDC}$	1200	internal reading
$\overline{MWTC}$	1000	internal writing
$\overline{R}$	1400	MPST bus reading
$\overline{W}$	1400	MPST bus writing

5.2.7 Settings

5.2.7.1 CCU/AS

The setting of the processor unit as a CCU or an active subscriber is carried out with the plug X6. If the processor is being used as a CCU, it produces the MPST bus clock. If the processor is being used as an active subscriber, in which the CCU is not a processor card 35 ZP 93, it must be guaranteed, that an MPST bus clock (CC <= 5MHz) is made available.

Jumper **X6**:



Note:
Only **one** processor card 35 ZP 93 with the jumper X6 may be operated per ABB Procontic T300.

5.2.7.2 Transfer memory

The size of the transfer memory dependent on the assembly can be set with the plug X4. If a larger transfer memory than 4 Kbytes is equipped, attention is to be paid but only 4 Kbytes can be obtained by the MPST bus. The transfer memory is obtained internally independent of the MPST subscriber number starting from 1000:H. The memory address is repeated depending on the memory size, e.g., the same memory cell is always addressed when using HM6116P-2 with the addresses 1000:0H, 1000:1000H.

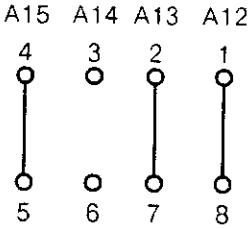
RAM	z.B. Type	X4	X8
2K x 8	6116	1 2 3	1 2 3
8K x 8	6264	1 2 3	1 2 3
32K x 8	62256	1 2 3	1 2 3

Setting the size of the transfer memory (RAM)

5.2.7.3 Subscriber number and transfer memory address

The subscriber number is set with the plug X9. The subscriber number consists of the upper 5 address bits, the upper 4 bits of which can be set on the 35 ZP 93. The byte 5 in the transfer memory of the example mentioned below is obtained by another active subscriber (AS) with the following address: 3000:4005H.

Jumper zone **X9**:



X9 set address: 4XXXH

The transfer memory is always obtained by the internal CPU under the addresses

1000:0000H ... 1000:0FFFH := 10000H ... 10FFFH.

5.2.7.4 RAM/EPROM

The type and size of the memory ICs can be wired up to plug X5 for 2 assembly positions each. A 20-polar socket is available for each of the memory positions A74, A75, A84, A85, A104, A105. If an IC is used with only a 24-polar casing, pins 1 - 2 and 27 - 28 in the socket remain free!

The numbers given in the above table describe the pins of the plug X5. If, for example, positions A104, A105 should be equipped with an EPROM 2716, X5.2 must be connected to X5.13 and X5.3 to X5.13.

position			EPROM					RAM		
A104 A105	A84 A84	A74 A75	2716	2732	2764	27128	27256	6116	6264	43256
1	5	9	-	-	13	13	13	-	-	18
2	6	10	13	16	16	16	16	14	16	16
3	7	11	13	13	-	17	17	13	13	17
4	8	12	-	-	13	13	18	-	14	14

* Only significant for positions A74 and A75! See also the assignment of the memory position address area under 5.2.5.10.

The assignment is as follows:

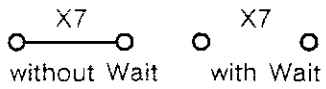
position		address area
high byte	low byte	
A104 A 84 A 74	A106 A 85 A 75	0000:0 ... 0000:FFFF 4000:0 ... 4000:FFFF E000:0 ... E000:FFFF

5.2.7.5 Wait state

An additional clock cycle can be set for slow memory media. The setting is carried out with X7.

Attention: A wait cycle is inserted for all the bus accesses!

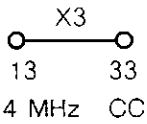
Jumper **X7**:



5.2.7.6 MPST bus clock

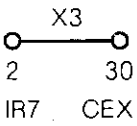
For a CPU clock of 8 MHz:

Jumper zone **X3**:



Interrupt of the data interface

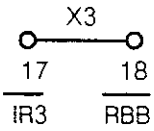
Jumper zone **X3**



Interrupt by $\overline{RBB}$

The CCU must have the possibility in the indirect bus mode of moving the active subscriber currently on the bus by sending $\overline{RBB}$ = 0 for the return of the bus. This requires the subscriber, who receives the bus, to demask IR3 and the IR3 pin is connected with $\overline{RBB}$.

Jumper zone **X3**



5.2.8 Model differences between 35 ZP 93 R31, R41 and R11, R12

The differences between the previous 5 MHz version (R11, R21) and the 8 MHz version (R31, R41) are listed in the following.

The printed board description can be the differing feature. The printed board code is GJR5133311 Px, whereby it is the 5 MHz version for x = 1 ... 5 and the 8 MHz version for x = 6.

Further differences include the following:
- The limitations for the interrupt treatment in the direct and indirect bus modes are no longer valid
- Extension for plug X8; RAM in the segment 1000
- Alteration of the clocks to wire wrap zone X3 (X3.9 to X3.15)
- Extension of the system bus; X11.32, X11.34
- Altering the timing (internal access times)
- Setting the transfer memory
- Setting the RAM/EPROM equipment
- Address decoding for the slots A74, A75, A84, A85
- Value for the MPST bus clock.

6 Data interfaces

35 DS 90 R20: Data interface for RS422 (RS423), RS232C and 20 mA current loop, 2-fold.
35 DS 91 R1: Data interface for RS423 and RS232C, without memory blocks, 2-fold.
35 DS 91 R2: Data interface for RS423 and RS232C, without memory blocks, 2-fold.
35 DS 91 R3: Data interface for RS423 and RS232C, with memory blocks, 2-fold.

6.1 Data interface 35 DS 90 R20 ..... 6.1- 1

6.1.1 Technical data 6.1- 2
6.1.2 Description 6.1- 2
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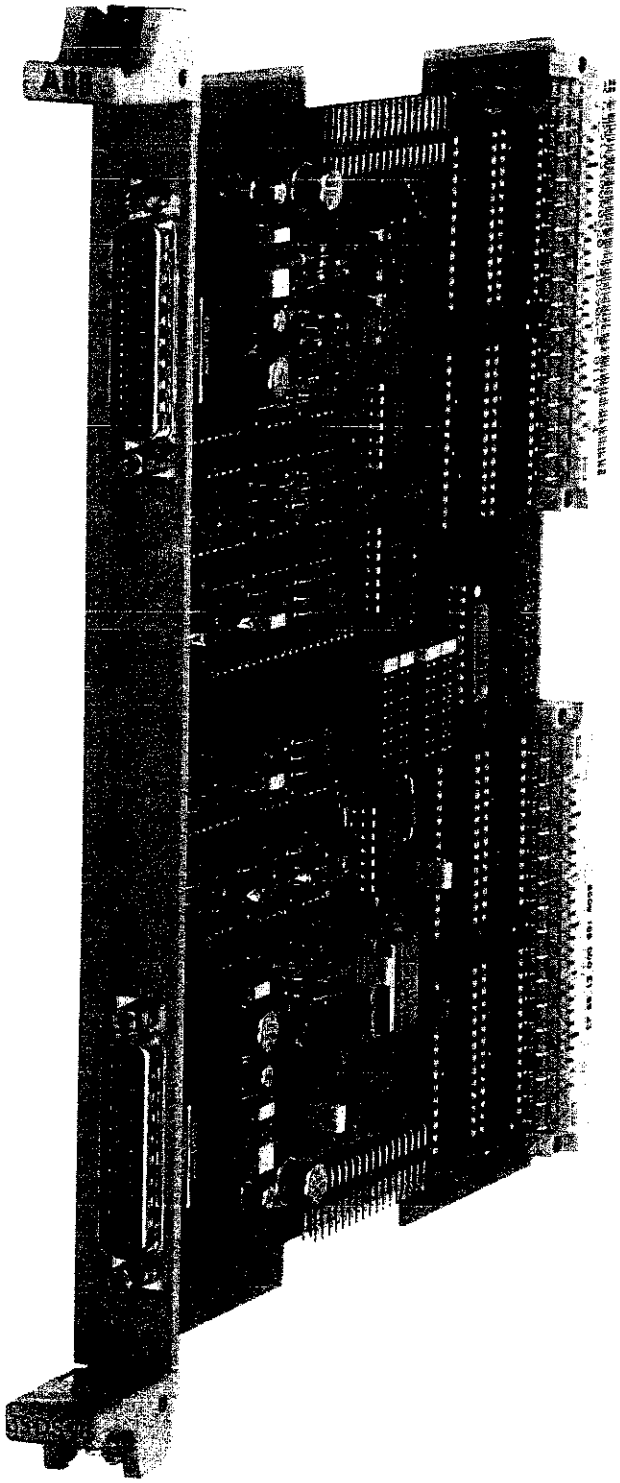
6.1 Data interface 35 DS 90 R20



90 07 08

6.1.1 Technical data

Number of interfaces	2
Interface 1	RS 232 RS 422 20 mA
Interface 2	RS 232 RS 422 20 mA
Memory extension	max. 256 KBytes
U_{B1} pos. supply voltage	+ 5 V ± 5 %
U_{B2} pos. supply voltage	+15 V ± 5 %
U_{B3} negative supply voltage	-15 V ± 5 %
Power loss	2.5 W ± 20 %
I_{B1} for U_{B1}	typically 0.4 A, max. 0.65 A
I_{B2} for U_{B2}	typically 0.08 A, max. 0.15 A
I_{B3} for U_{B3}	typically 0.08 A, max. 0.15 A
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	1 pitch
Weight	1.0 kg
Order number	GJR5133300R20

6.1.2 Description

The unit 35 DS 90 operates with the system bus of the processor card 35 ZP 93. The current supply of the data interface comes via the plug for the MPST bus.

6.1.2.1 Serial interfaces

The 35 DS 90 has two serial interfaces for a full duplex operation. Every interface is equipped with an interface switch for RS422 (RS423), RS232 and 20 mA current loop (active, passive). The transfer rates can be set separately for the sender and receiver of each interface (110, 300, 600, 1200, 2400, 4800, 9600, 19200 and 38400 Baud). A 25-polar standard plug is available for each interface. There is an operation display with LEDs on the front panel. The MPSC 8274 from Messrs Intel was used as the interface block. The MPSC can be programmed for an asynchronic and a bit-synchronic transfer protocol.

6.1.2.2 Memory extension

The 35 DS 90 also has a memory extension of maximal 256 Kbytes. A total of eight 28-polar slots are available for higher and lower bytes. The slots can be equipped with EPROM as well as RAM.

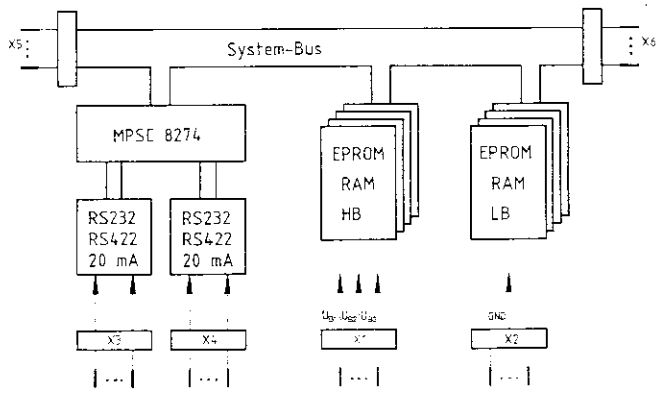


Fig. 6.1-1

6.1.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

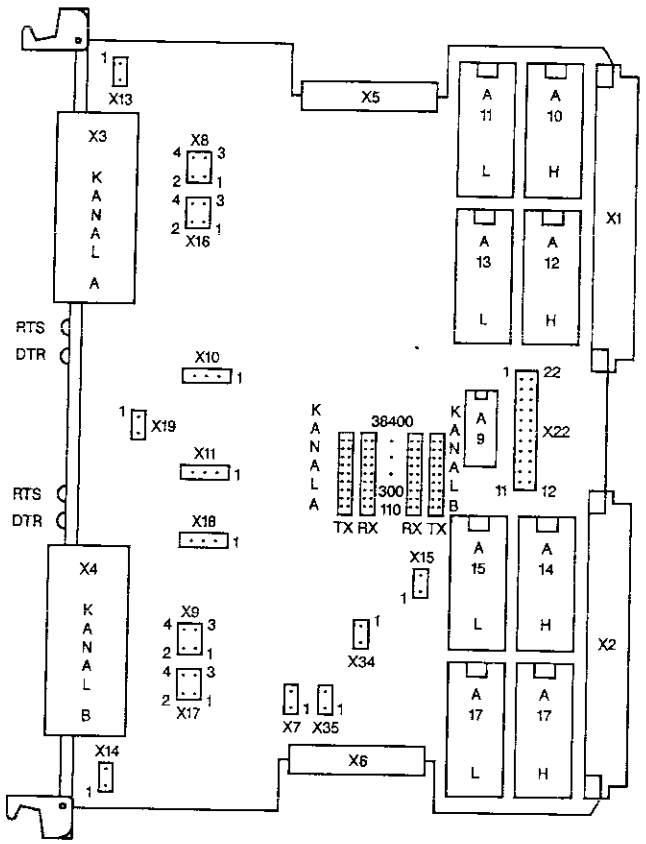


Fig. 6.1-2 Component side (top view)

A maximum of two data interfaces 35 DS 90 can be connected to a 35 ZP 93.

Summary of the interfaces and plugs

Code	Interface, plug	Model	Pole
X1	MPST bus (only current supply)	DIN41612, part2 constr. form C	32
X2	MPST bus (only current supply)	DIN41612, part2 constr. form C	32
X3	Serial interface channel A	Cannonconnector	25
X4	Serial interface channel B	Cannonconnector	25
X5	System bus to the 35 ZP 93	Flat cable	34
X6	System bus to the 35 ZP 93	Flat cable	34
X7	MPSC 8274 interrupt, high-active	Wire-wrap	2
X8	20 mA current loop, channel A	Wire-wrap	4
X9	20 mA current loop, channel B	Wire-wrap	4
X10	Operating load, channel A	Wire-wrap	3
X11	Operating load, channel B	Wire-wrap	3
X12	RAM/EPROM equipment	Wire-wrap	22
X13	Connection: screen - 0 Volt, A	Wire-wrap	2
X14	Connection: screen - 0 Volt, B	Wire-wrap	2
X15	Addresses of the assembly positions	Wire-wrap	2
X16	20 mA current loop, channel A	Wire-wrap	4
X17	20 mA current loop, channel B	Wire-wrap	4
X18	Addresses of the MPSC 8274	Wire-wrap	3
X19	SYNDET for 8274, channel B	Wire-wrap	2
X21	Baudratechannel A, Transmit Data	Wire-wrap	18
X22	Baudratechannel A, Receive Data	Wire-wrap	18
X31	Baudratechannel B, Transmit Data	Wire-wrap	18
X32	Baudratechannel B, Receive Data	Wire-wrap	18
X34	Baud rate clock oscillator	Wire-wrap	2
X35	MPSC 8274 interrupt, low-active	Wire-wrap	2

6.1.4 Interface values

6.1.4.1 MPST interface, plugs X1, X2

No connections to X1, X2 except for the current supply. The ACK line is a through connection.

Plug X1:

Pin	Signal name	Meaning
X1. 2a	UB1	5 V voltage
X1. 4a	UB1	5 V voltage
X1. 6a	UB3	–15 V voltage
X1.30a	–	–
X1.32a	ACKo	Acknowledge out
X1. 2c	UB1	5 V voltage
X1. 4c	UB1	5 V voltage
X1. 6c	UB2	15 V voltage
X1.30c	–	–
X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal name	Meaning
X2. 2a	–	–
X2. 4a	–	–
X2.28a	–	–
X2.30a	0 V	0 V voltage
X2.32a	0 V	0 V voltage
X2. 2c	–	–
X2. 4c	–	–
X2.28c	–	–
X2.30c	0 V	0 V voltage
X2.32c	0 V	0 V voltage

6.1.4.2 Serial interfaces X3, X4

Plug X3: 8274 channel A

Pin	Signal name	Meaning	Operating mode		I/O
X3.1	Screen	Protective ground			
X3.2	$\overline{\text{TxD}}$	Transmit data	RS422	RS232	O
X3.3	$\overline{\text{RxD}}$	Receive data	RS422/423	RS232	I
X3.4	RTS	Request to send		RS232	O
X3.5	CTS	Clear to send	RS423	RS232	I
X3.6					
X3.7	GND	Signal 0 V			
X3.8	CD	Carrier detect	RS423	RS232	I
X3.9	TxI–	Transmit data		20 mA	
X3.10	TxI+	passive			
X3.11					
X3.12	SYNDET	Syncr. detection	RS423	RS232	I
X3.13					
X3.14					
X3.15					
X3.16					
X3.17					
X3.18	TxD	Transmit data	RS422		O
X3.19					
X3.20	DTR	Data terminate ready		RS232	O
X3.21	RxD	Receive data	RS422		I
X3.22					
X3.23					
X3.24	RxI+	Receive data		20 mA	
X3.25	RxI–	passive			

Plug X4: 8274 channel B

Pin	Signal name	Meaning	Operating mode	I/O
X4.1	Screen	Protective ground		
X4.2	$\overline{TxD}$	Transmit data	RS422 RS232	O
X4.3	$\overline{RxD}$	Receive data	RS422/423 RS232	I
X4.4	RTS	Request to send	RS232	O
X4.5	CTS	Clear to send	RS423 RS232	I
X4.6				
X4.7	GND	Signal ground		
X4.8	CD	Carrier detect	RS423 RS232	I
X4.9	TxI–	Transmit data passive	20 mA	
X4.10	TxI+			
X4.11				
X4.12	SYNDET	Syncr. detection	RS423 RS232	I
X4.13				
X4.14				
X4.15				
X4.16				
X4.17				
X4.18	TxD	Transmit data	RS422	O
X4.19				
X4.20	DTR	Data terminate ready	RS232	O
X4.21	RxD	Receive data	RS422	I
X4.22				
X4.23				
X4.24	RxI+	Receive data passive	20 mA	
X4.25	RxI–			

Operating mode	max. cable length*	Max. baud rate
RS422	500 m	38,400
RS232	50 m	19,00
20 mA	200 m	9,600

* Type LiYCY 5 x 0.14 mm^2 with a common screen.

The given lengths are recommended values. Please note the data of the units to be connected for the actual lengths.

6.1.4.3 System bus

The system bus of the processor card 35 ZP 93 may be loaded with a maximum of two data interfaces 35 DS 90. The ribbon cable and the mechanical connecting elements required for the connection of the processor card with the data interface are included with every data interface.

Plug X5:

Pin	Signal name	Meaning
X5.1	$\overline{MRDC}$	Memory read
X5.2	$\overline{IORC}$	I/O Read
X5.3	$\overline{MWTC}$	Memory write
X5.4	A01	Address bit 01
X5.5	A03	Address bit 03
X5.6	A05	Address bit 05
X5.7	A07	Address bit 07
X5.8	A09	Address bit 09
X5.9	A11	Address bit 11
X5.10	A13	Address bit 13
X5.11	A15	Address bit 15
X5.12	A17	Address bit 17
X5.13	A19	Address bit 19
X5.14	HLDA	Hold Acknowl.
X5.15	+ 5 V	Supply voltage
X5.16		
X5.17		
X5.18		
X5.19		
X5.20	+ 5 V	Supply voltage
X5.21	$\overline{BHE}$	
X5.22	A18	Address bit 18
X5.23	A16	Address bit 16
X5.24	A14	Address bit 14
X5.25	A12	Address bit 12
X5.26	A10	Address bit 10
X5.27	A08	Address bit 08
X5.28	A06	Address bit 06
X5.29	A04	Address bit 04
X5.30	A02	Address bit 02
X5.31	A00	Address bit 00
X5.32	Reserved	Special uses
X5.33	$\overline{AIOWC}$	Adv. I/O write
X5.34	Reserved	Special uses

Plug X6:

Pin	Signal name	Meaning
X6.1	GND	Ground
X6.2	ALE	Addr. latch enab.
X6.3	BEX	Line B exp.
X6.4	$\overline{RES}$	Reset from 8284A
X6.5	DEX	Line D exp.
X6.6	CAS0	CAS 0 of the 8259A
X6.7	CAS1	CAS 1 of the 8259A
X6.8	D01	Data bit 01
X6.9	D03	Data bit 03
X6.1	D05	Data bit 05
X6.11	D07	Data bit 07
X6.12	D09	Data bit 09
X6.13	D11	Data bit 11
X6.14	D13	Data bit 13
X6.15	D15	Data bit 15
X6.16		
X6.17		
X6.18		
X6.19		
X6.20	D14	Data bit 14
X6.21	D12	Data bit 12
X6.22	D10	Data bit 10
X6.23	D08	Data bit 08
X6.24	D06	Data bit 06
X6.25	D04	Data bit 04
X6.26	D02	Data bit 02
X6.27	D00	Data bit 00
X6.28	$\overline{INTA}$	Intr. Acknowl.
X6.29	AEX	Line A exp.
X6.30	RDYi	Ready internally
X6.31	CEX	Line C exp.
X6.32	$\overline{M/IO}$	Memery I/0 mode
X6.33	$\overline{HOLD}$	Hold request
X6.34	GND	Ground

The lines AEX, BEX, CEX and DEX must be wired up in wrap zone X3 on the processor card 35 ZP 93 according to their use.

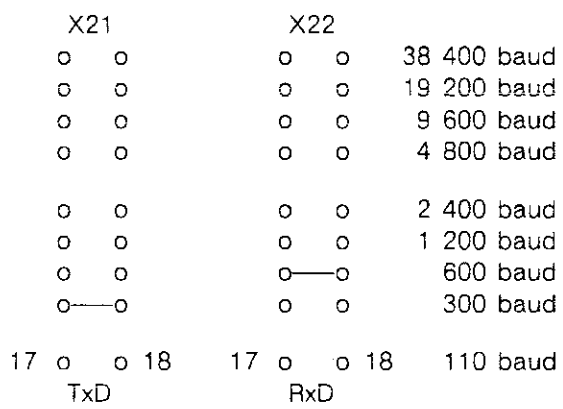
6.1.5 Settings

6.15.1 Serial interfaces

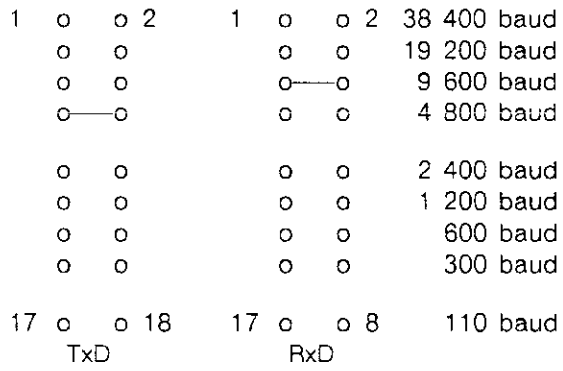
Baud rates

The setting of the baud rate is carried out using the plug panel X21-X32. The plug X34 serves to disconnect the clock oscillator but should normally always be connected.

Channel A



Channel B

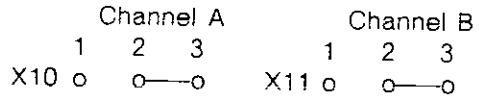


The following is set as an example:

Channel A	Sender	300 baud
	Receiver	600 baud
Channel B	Sender	4 800 baud
	Receiver	9 600 baud

Operating modes

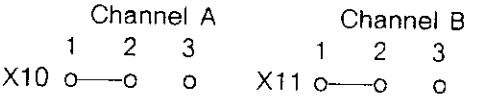
RS232



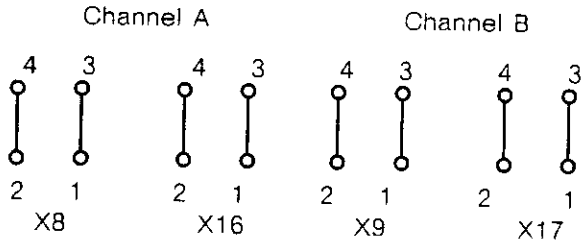
The inputs for the control signals SYNDET, CD and CTS are set permanently to RS423/RS232 and the outputs for RTS, DTR permanently to RS232.

If the input signal SYNDET B should be used for the channel B of the 8274, the jumper X19 must be connected. The signal RTS for channel B is then no longer available.

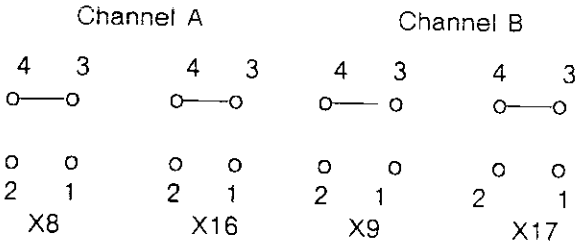
RS422



20 mA current loop, active



20 mA current loop, passive



The loop current is limited to typically 20 mA in the sender and receiver in the active and passive modes. The maximum voltage $U_{ext.}$ is $\leq$ 24 V, when the loop resistance Rs = 0.

Attention:
The 20 mA interface may not be active, if the interface RS 232 is active. This can lead to the destruction of the interface.

6.1.5.2 Address overview

Addresses in the I/O area

Basis address of the MPSC 8274

X18 3 2 1	I/O Basic address	Channel A Data	Channel A Com-mand	Channel B Data	Channel B Com-mand
o o—o o—o o	100H 200H	100H 200H	104H 204H	102H 202H	106H 206H

Address assignment from 35 DS 90 to 35 ZP 93

Positions	Address X15 1 2 o—o	Address X15 1 2 o o
A10, A11	40000 ... 4FFFFH	80000 ... 8FFFFH
A12, A13	50000 ... 5FFFFH	90000 ... 9FFFFH
A14, A15	60000 ... 6FFFFH	A0000 ... AFFFFH
A16, A17	70000 ... 7FFFFH	B0000 ... BFFFFH
		D0000 ... DFFFFH

If the memory IC used is smaller than 64 kbytes it leads to the repetition of the memory area for different memory addresses within the decoded 64 kbytes. I.e., the byte 0 can be obtained under the following addresses when using an 8 k x 8 memory IC on the positioned A10, A11:
80000H, 84000H, 88000H, 8C000H.

If a link capacity of 32 kbytes is to be obtained and only memory ICs of 8 k x 8 are available on the positions A10, A11, A12, A13, the segment must be put on 8C000H.

6.1.6 RAM/EPROM equipment

The type and size of the memory ICs can be wired up to the plug X12 for two assembly positions each. A 28-polar socket is available for each position A10 to A17. If an IC is used with a 24-polar casing only, pins 1-2 and 27-28 in the socket remain free.

The numbers given in the table code the pins of plug X12. If, for example, positions A10, A11 are to be equipped with an EPROM 2716, X12.21 must be connected with X12.6 and X12.20 with X 12.6.

The low bytes are A11, A13, A15, A17 and the high bytes are A10, A12, A14, A16.

Position				EPROM					RAM		
A10 A11	A12 A13	A14 A15	A16 A17	2716	2732	2764	27128	27256	6116	6264	43256
22	18	14	10	–	–	6	6	6	–	–	2
21	17	13	9	6	4	4	4	4	1	4	4
20	16	12	8	6	6	–	3	3	6	6	3
19	15	11	7	–	–	6	6	2	–	1	1

6.1.7 Interrupt wiring

The interrupt output of the 8274 can be connected with the plugs X7/X35 with the lines BEX and CEX of the system bus. The plug X7 switches an active high interrupt to the line CEX and the plug X35 an active low interrupt to the line BEX.

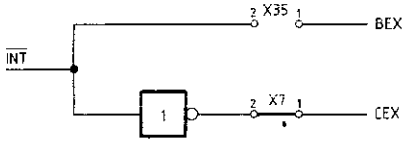


Fig. 6.1-3

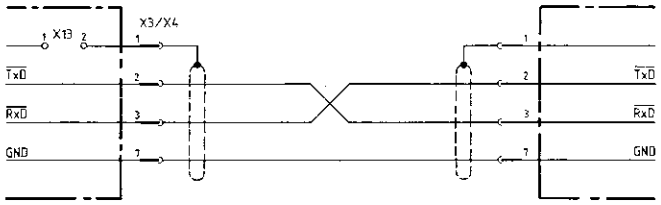
6.1.8 Application instructions

When connecting the serial interfaces, attention is to be paid that the connections are carried out completely as described in the following drawings. Special attention is to be paid to the fact, that the pin 7 (GND) is connected for RS 232 as well in order to guarantee the functioning of the interference suppression coil.

If 2 units, which are supplied from different mains, are to be connected with the RS 232 interface, considerable voltage differences can arise, and these destroy the interface blocks. If this is the case, the 0 V area of the two units is to be connected with a conductor, which has a sufficient cross section.

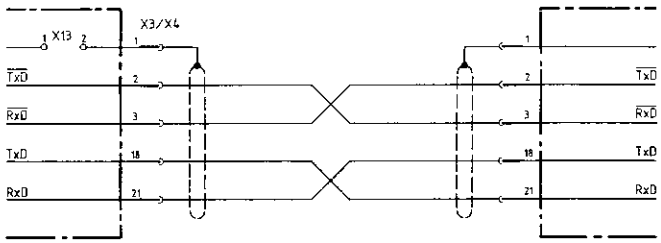
Attention is also to be paid to the fact, that the screen is always put on one side only. This should be carried out on the side turned away from the 35 DS 90, if possible. If this is not possible, the screen is connected with the casing via the plug X3/X4. There are no interference pression coils installed in the lines X3.1/X4.1.

RS232



35 DS 90 35 DS 90 or other units

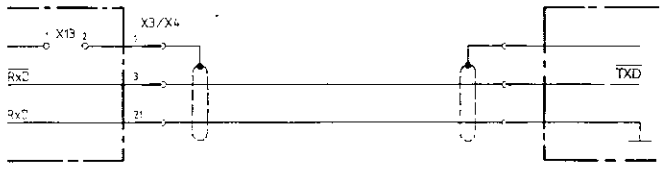
RS422



35 DS 90

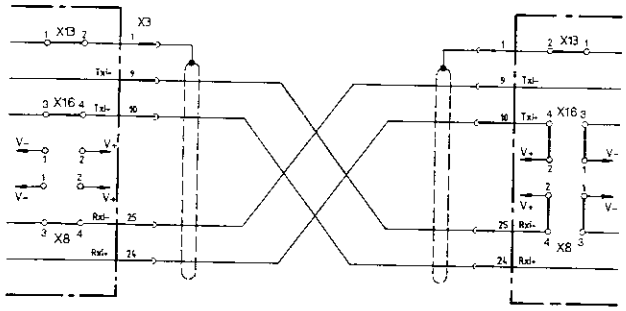
Attention:
A chassy earth connection may not be created with the interface cable for RS422. An equipotential bonding between the two systems must be carried out using a conductor with a sufficient cross section ($\geq$ 4 mm^2) in order to prevent a voltage difference being created between the 35 DS 90 and the other unit.

RS423 (only receivers)



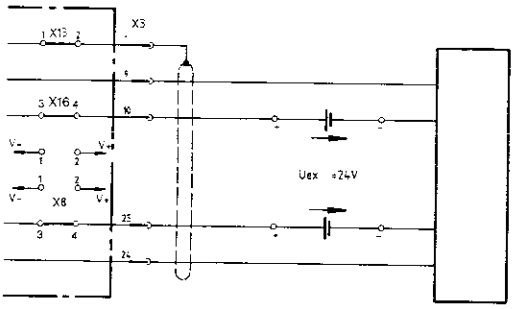
35 DS 90

Current loop 20 mA



35 DS 90
passive

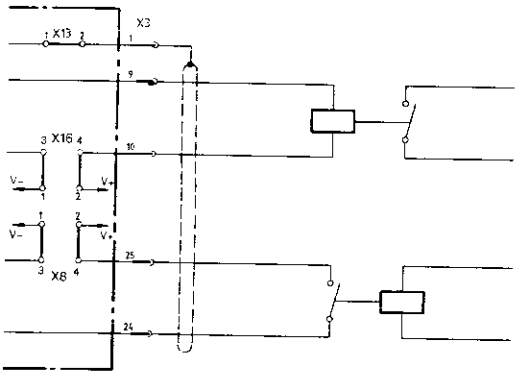
35 DS 90
active



35 DS 90
passive

other unit
passive

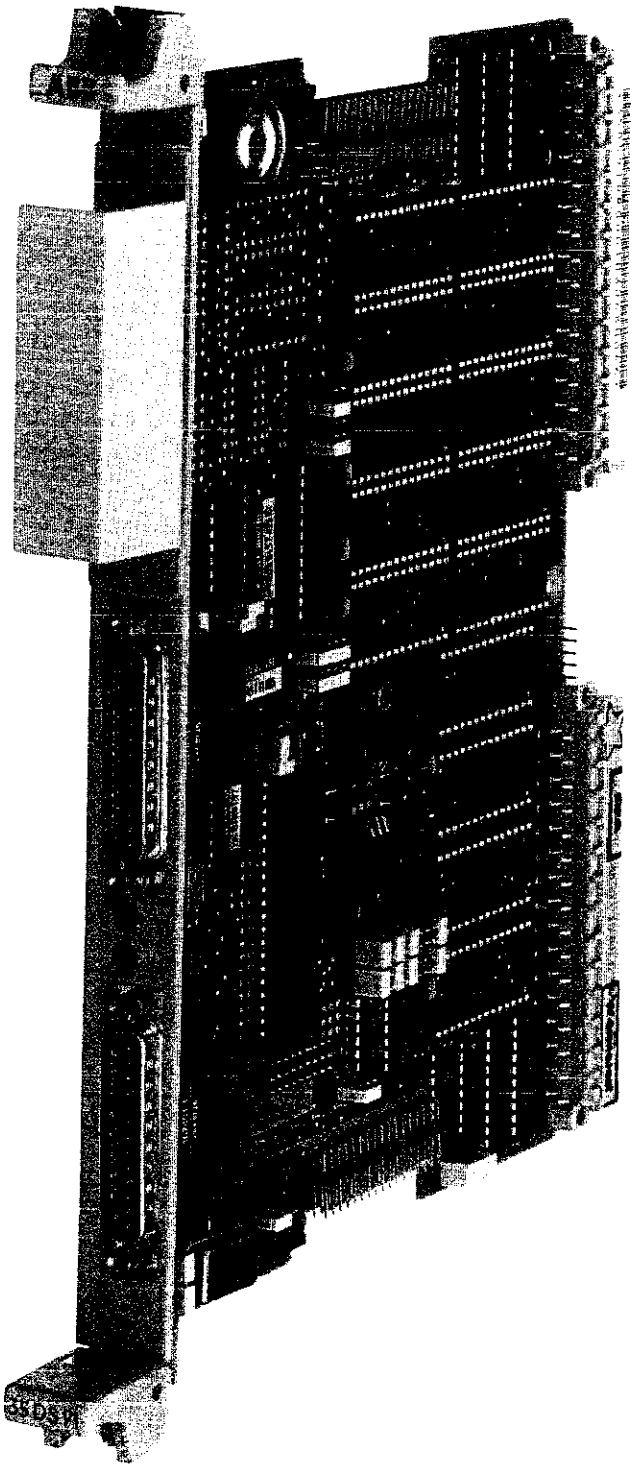
Fig. 6.1-4: Interface connections



35 DS 90
active

other unit
passive

6.2 Data interface 35 DS 91 R1



90 07 03

6.2.1 Technical data

Interface specification	RS 423 and RS 232 C
	Note: No display of the operating status of the serial interface using LED
Transfer rates	110, 300, 600, 1200, 2400, 4800, 9600, 19200 and 38400 baud
	Note: The transfer rate can only be set in common for the sender and receiver of one channel.
Channels	2
Handshakes	Hardware handshakes via 'request to send' and 'clear to send'; software handshake via XON and XOFF.
Protocols	Asynchronic protocol with 1 start bit, 8 data bits, 1 stop bit and no parity bit.
	Note: Further asynchronic protocols can be programmed. Asynchronic, byte-synchronic, bit-synchronic transfer protocols can be programmed.
Supply voltages:	
U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+ 15 V ± 5 %
U_{B3} negative supply voltage	− 15 V ± 5 %
U_{SR} Buffer voltage (lithium battery)	+ 2.9 V ... + 3.7 V
Supply currents with the full equipment:	
I_{B1} from U_{B1}	0.5 A ± 30 %
I_{B2} from U_{B2}	0.1 A ± 30 %
I_{B3} from U_{B3}	0.1 A ± 30 %
Power dissipation	max. 7W
Ambient temperature	0 °C ... + 55 °C
Storage temperature	− 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Electromagnetic compatibility (EMC)	IEC 801
Dimensions	1 pitch
Weight	1.0 kg
Order number	GJR5137410 R1

Accessories:

Lithium battery 07 LB 20 R1	GJR5223500R1
Lithium battery module 35 LE 90 R1	GJR5146300R1

6.2.2 Description

The data interface 35 DS 91 operates with the system-bus of the processor card 35 ZP 93 R31, R41 (8 MHz version). Two 35 DS 91 or a combination of 35 DS 91 and 35 DS 90 can be connected to the processor card 35 ZP 93 using the system bus. The current supply of the data interface comes via the MPST bus.

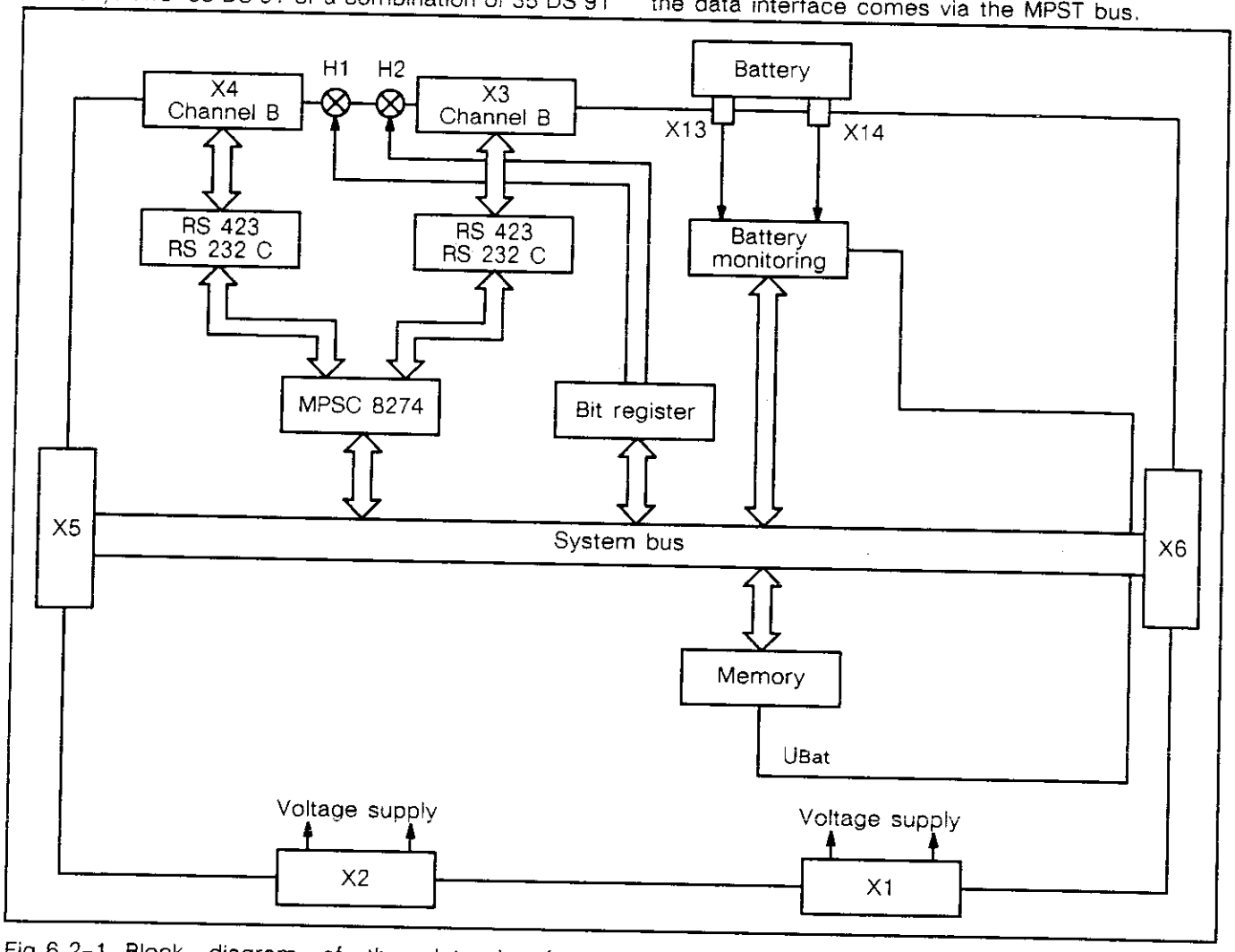


Fig.6.2-1 Block diagram of the data interface 35 DS 91

6.2.2.1 Memory

The data interface 35 DS 91 has a memory extension of max. 576 Kbytes. A total of 14 28-polar slots are available. Ten of these slots are foreseen for RAM and four slots selectively for RAM or EPROM. The entire memory positions can be buffered with a battery.

6.2.2.2 Battery

The battery for buffering the RAM slots are attached on the front panel of the unit. Changing the lithium battery or the lithium battery module is therefore possible without disconnecting the module.

6.2.2.3 Bit register

The bit register consists of an input multiplexer and an output register. Hardware signals are read via the input multiplexer. Four bits can be set using the plug-in jumpers on X19.

Important signals for the hardware are output with the output register. The bit register outputs are set to 0 by an MPST reset or by switching on the voltage.

6.2.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

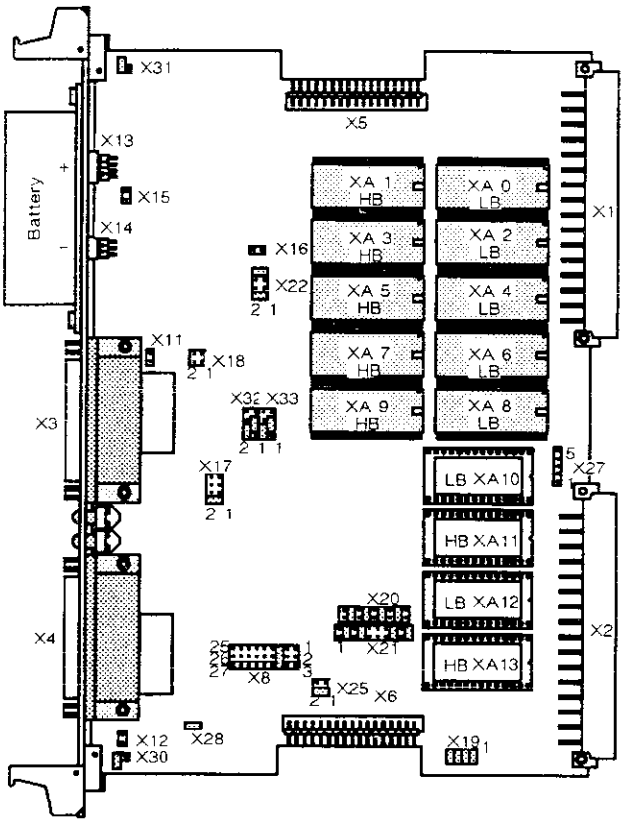


Fig. 6.2-2 Component side (top view)

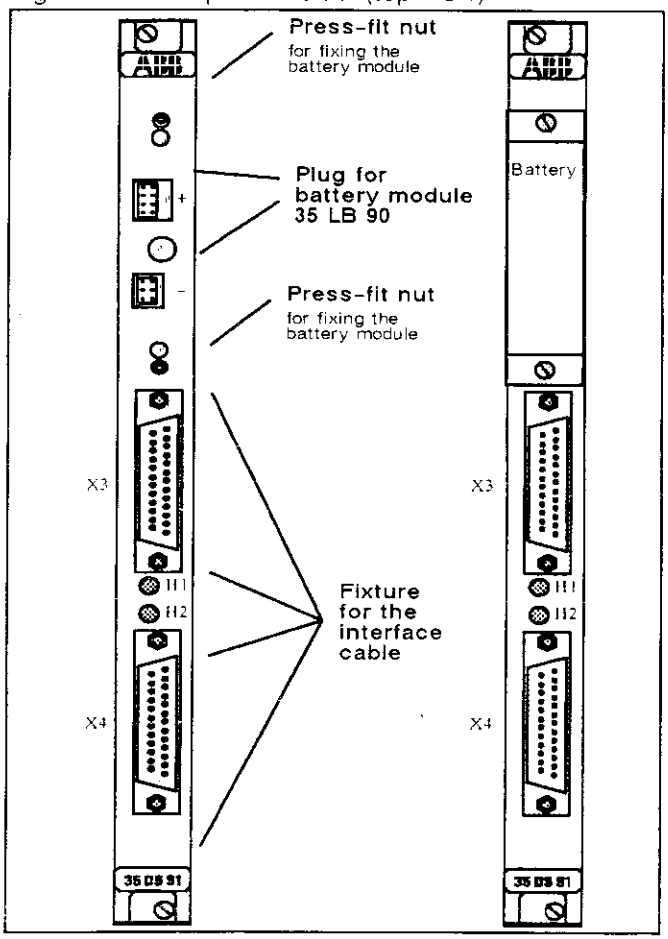


Fig. 6.2-3: Front panel with/without a lithium battery module 35 LE 90

Interface, plug and wrap zone overview

Code	Interface, plug	Model	Pole
X1	MPST bus (only current supply)	DIN41612, part 2 constr. form C	32
X2	MPST bus (only current supply)	DIN41612, part 2 constr. form C	32
X3	Serial interface channel A	Male connector	25
X4	Serial interface channel B	Male connector	25
X5	System bus to the 35 ZP 93	Flat cable	34
X6	System bus to the 35 ZP 93	Flat cable	34
X8	Baud rate channels A and B	Plug connector	27
X11	Connection: screen - 0 V	Plug connector	2
X12	Connection: screen - 0 V	Plug connector	2
X13	Battery contact: positive	Plug connector	8
X14	Battery contact: negative	Plug connector	6
X15	Basic load for the battery	Plug connector	2
X16	Only for test purposes of the producer	Plug connector	2
X17	Unit address (3 various)	Plug connector	6
X18	Memory addresses	Plug connector	4
X19	Binary input for the bit register	Plug connector	8
X20	Battery buffer, memory type for XA 10, XA 11	Plug connector	18
X21	Battery buffer, memory type for XA 12, XA 13	Plug connector	20
X22	Battery buffer for XA 0 - XA 9	Plug connector	8
X25	interrupt 35 DS 91 with 35 ZP 93	Plug connector	4
X27	Battery voltage MPST bus	Plug connector	5
X28	Oscillator frequency serial interface	Plug connector	2
X30	Connection: front panel - 0 V	Plug connector	2
X31	Connection: front panel - 0 V	Plug connector	2
X32	Memory address high byte	Plug connector	8
X33	Memory address low byte	Plug connector	8

6.2.4 Plug assignment

6.2.4.1 MPST interface, plugs X1, X2

The ACK line is connected continuously.

Plug X1:

Pin	Signal name	Meaning
X1. 2a	UB1	5 V voltage
X1. 4a	UB1	5 V voltage
X1. 6a	UB3	−15 V voltage
X1.26a	–	–
X1.32a	ACKo	Acknowledge out
X1. 2c	UB1	5 V voltage
X1. 4c	UB1	5 V voltage
X1. 6c	UB2	15 V voltage
X1.26c	–	–
X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal name	Meaning
X2.22a	–	–
X2.30a	0 V	0 V voltage
X2.32a	0 V	0 V voltage
X2.22c	$\overline{RS}$	Reset
X2.26c	–	–
X2.30c	0 V	0 V voltage
X2.32c	0 V	0 V voltage

6.2.4.2 Serial interfaces

Plug X3: Channel A

Pin	Signal name	Meaning	Operating mode	I/O
X3.1	Screen	Protective ground		
X3.2	$\overline{TxD}$	Transmit data	RS423, RS 232	O
X3.3	$\overline{RxD}$	Receive data	RS423, RS 232	I
X3.4	RTS	Request to send	RS423, RS 232	O
X3.5	CTS	Clear to send	RS423, RS 232	I
X3.7	GND	Signal ground		
X3.20	DTR *	Data terminal Ready	RS423, RS 232	O

* DTR is logically 1 (on line), after the voltage has been switched on

Plug X4: Channel B

Pin	Signal name	Meaning	Operating mode	I/O
X4.1	Screen	Protective ground		
X4.2	$\overline{TxD}$	Transmit data	RS423, RS 232	O
X4.3	$\overline{RxD}$	Receive data	RS423, RS 232	I
X4.4	RTS	Request to send	RS423, RS 232	O
X4.5	CTS	Clear to send	RS423, RS 232	I
X4.7	GND	Signal ground		
X4.20	DTR *	Data terminal Ready	RS423, RS 232	O

* DTR is logically 1 (online), after the voltage has been switched on

Note:

Non-listed pins are not assigned.

6.2.4.3 System bus

According to the assertion mentioned in 6.2.2 concerning the double effect between the data interfaces and the processor unit, attention is to be paid to the fact that the memory area of 50000H ... DFFFFH is not assigned twice. This means that either the 35 DS 91 memory is blocked with the SA signal or the 35 DS 90 is operated without memory blocks.The remaining functions of the units can still be used. The ribbon cable required to connect the processor card and the data interface are enclosed with every data interface. The enclosed connecting set also includes the parts required for the mechanical connection of the data interface and processor card.

Plug X5:

Pin	Signal	Meaning		Pin	Signal	Meaning
X5. 1	$\overline{\text{MRDC}}$	Memory read		X5.18	–	–
X5. 2	$\overline{\text{IORC}}$	I/O read		X5.19	–	–
X5. 3	$\overline{\text{MWTC}}$	Memory write		X5.20	UB1	5 V voltage
X5. 4	A01	Address bit 01		X5.21	$\overline{\text{BHE}}$	Bus high byte
X5. 5	A03	Address bit 03		X5.22	A18	Address bit 18
X5. 6	A05	Address bit 05		X5.23	A16	Address bit 16
X5. 7	A07	Address bit 07		X5.24	A14	Address bit 14
X5. 8	A09	Address bit 09		X5.25	A12	Address bit 12
X5. 9	A11	Address bit 11		X5.26	A10	Address bit 10
X5.10	A13	Address bit 13		X5.27	A08	Address bit 08
X5.11	A15	Address bit 15		X5.28	A06	Address bit 06
X5.12	A17	Address bit 17		X5.29	A04	Address bit 04
X5.13	A19	Address bit 19		X5.30	A02	Address bit 02
X5.14	HLDA	Hold Acknowledge		X5.31	A00	Address bit 00
X5.15	UB1	5 V voltage		X5.32	Reserved	Special applications
X5.16	–	–		X5.33	$\overline{\text{AIOWC}}$	Adv. I/O write
X5.17	–	–		X5.34	Reserved	Special applications

Plug X6:

Pin	Signal	Meaning		Pin	Signal	Meaning
X6. 1	0 V	0 V voltage		X6.18	–	–
X6. 2	ALE	Address latch enabable		X6.19	–	–
X6. 3	BEX	Line B exp.		X6.20	D14	Data bit 14
X6. 4	RES	Reset of the 8284A		X6.21	D12	Data bit 12
X6. 5	DEX	Line D exp.		X6.22	D10	Data bit 10
X6. 6	CAS0	CAS 0 of the 8259A		X6.23	D08	Data bit 08
X6. 7	CAS1	CAS 1 of the 8259A		X6.24	D06	Data bit 06
X6. 8	D01	Data bit 01		X6.25	D04	Data bit 04
X6. 9	D03	Data bit 03		X6.26	D02	Data bit 02
X6.10	D05	Data bit 05		X6.27	D00	Data bit 00
X6.11	D07	Data bit 07		X6.28	$\overline{\text{INTA}}$	Intr. acknowledge
X6.12	D09	Data bit 09		X6.29	AEX	Line A exp.
X6.13	D11	Data bit 11		X6.30	RDYi	Ready internally
X6.14	D13	Data bit 13		X6.31	CEX	Line C exp.
X6.15	D15	Data bit 15		X6.32	$\overline{\text{M/IO}}$	Memory I/O mode
X6.16	–	–		X6.33	$\overline{\text{HOLD}}$	Hold request
X6.17	–	–		X6.34	0 V	0 V voltage

The lines AEX, BEX, CEX and DEX must be wired up to the wrap zone X3 on the processor card 35 ZP 93 depending on their use.

6.2.5 Settings in the I/O area

6.2.5.1 Setting the I/O addresses:

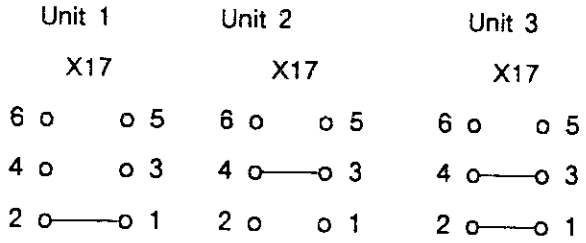
The interface 35 DS 91 can be operated together with the processor card 35 ZP 93 as unit 1, 2 or 3. The only differences are in the assignment of the I/O addresses to the function units.

A certain 35 DS 91, which is operated using the system bus of the processor card, is understood with the word 'unit'. The words 'unit address' are the I/O addresses of the function units available on the data interface.

Note:
Only 2 data interfaces can be operated physically on the system bus.

The assignment of the respective unit number is carried out with the settings in the jumper zone X17:

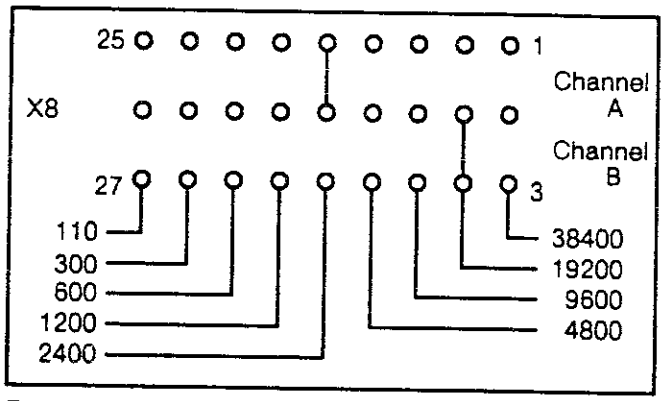
Jumper field **X17**:



6.2.5.2 Serial interface

Baud rates;
Setting the baud rate is carried out using the plug panel X8. The baud rates can be set independently of each other for channels A and B. The transmit and receive baud rates of one channel can only be set together. The plug X28 serves to connect the clock oscillator and the serial interface and must always be plugged in.

Jumper field X8:



The given baud rates are only valid, if the MPSC block was programmed with an internal pitch factor of 16.

Set baud rate:
Channel A: Sender and receiver 2400 Baud
Channel B: Sender and receiver 19200 Baud

Basis address of the interface controller

Unit	I/O Basis address	Channel A Data	Channel A Com-mand	Channel B Data	Channel B Com-mand
1	0100 H	0100 H	0104 H	0102 H	0106 H
2	0400 H	0400 H	0404 H	0402 H	0406 H
3	1400 H	1400 H	1404 H	1402 H	1406 H

Note:
The subscriber address is set in the plug zone X17.

0 V plug connection for RS232/RS422
X11, X12: The jumper connects the screen of the serial interface with 0 V of the data interface (electronics 0 V)
X30, X31: The jumper connects the front panel with 0 V of the data interface

6.2.6 Address overview

Address assignment for the 35 ZP 93 by the 35 DS 91

Address	Unit/Medium	Position
DFFFF to 50000	Maximum memory capacity of the 35 DS 91	XA00 to XA13

Addresses in the I/O area of the 35 ZP 93

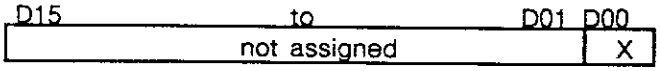
Function	X17 5 o o 6 3 o o 4 1 o—o 2	X17 5 o o 6 3 o—o 4 1 o o 2	X17 5 o o 6 3 o—o 4 1 o—o 2
Serial interface	0100...010F	0400...040F	1400...140F
Status bit register	2400...240F	3400...340F	4400...440F
Reserved for clock	5400...540F 6400...640F		
Reserved for the interrupt controller	7400...740F	8400...840F	9400...940F
Reserved for the iSBX interface	A400...A40F B400...B40F	C400...C40F D400...D40F	E400...E40F F400...F40F

6.2.7 Settings

6.2.7.1 Status bit register

This is an 8 bit status register, which can be read and written. The basic address can be set in the I/O area on 240X, 340X and 440X.

Data format of the bit register
The in- and outputs of the bit register are only connected with the data line D0.



X = 0 or 1

Address in the bit register:	X 4 0 8	X 4 0 A	X 4 0 C	X 4 0 E

All these status bit registers (outputs) are deleted after a reset.

Function and addresses of the status bit register

Address	Signal access	Function of data bit D00
X400	not assigned	
X402	not assigned	
X404	SA Read SA Write	1 = entire memory area faded out 1 = switch off the entire memory area
X406	not assigned	
X408	I4 Read Write	Binary input: 0 = Jumper X19/7-8 not used
X40A	I3 Read Write	Binary input: 0 = Jumper X19/5-6 not used
X40C	I2 Read H2 Write	Binary input: 0 = Jumper X19/3-4 1 = LED (H2) ON
X40E	I2 Read H1 Write	Binary input: 0 = Jumper X19/1-2 1 = LED (H1) ON

X = one of 3 unit addresses, which can be set in the plug zone X19.

Address X40E: 0 = 'Siebert telegram'
1 = 'ASCII telegram'

Signal SA:
This can be set as a single signal using the bit register and prompted.

SA = 1: The memory area on the 35 DS 91 cannot be addressed.
SA = 0: The memory area can be addressed.

Binary input (X19):
A four-figure binary value can be set in the jumper zone X19 and prompted using the bit register.

See the function and addresses of the status bit register.

6.2.7.2 Battery monitoring

Signals of the battery monitoring

$\overline{\text{BATOK}}$:
This signal is produced by the battery monitoring switch and can be prompted using the bit register or can initiate an interrupt using the interrupt controller.

- $\overline{\text{BATOK}}$ = 0 The battery is OK, battery voltage > 2.9 V
- $\overline{\text{BATOK}}$ = 1
  - o The battery is not present
  - o Battery voltage < 2.9 V
  - o A new battery is present but the battery change was not yet acknowledged with BATQ.

BATQ: Battery acknowledgement
BATQ is an input signal for the monitoring switch of the battery and is produced by the bit register. The correct use of this signal completes a battery change.

- BATQ = 0 is the status, which is always to be assumed after an acknowledgement.
- BATQ = 1 means that a battery change is to be acknowledged with BATQ = 1 (Output via the bit register, address: X406 =1). BATQ is then to be reset to 0.

6.2.8 Settings in the memory area

6.2.8.1 Setting the memory addresses

The assignment of the memory addresses to the corresponding assembly positions for the memories is carried out in the wrap zones X18, X32 and X33.

The settings for the memory type used and a battery buffer can also be carried out in the wrap zones X20, X21 and X22 (see also the following tables).

The even position numbers (XA00, XA02, etc.) are the low bytes.

The odd position numbers (XA01, XA03 etc.) are the high bytes.

The assembly positions XA00 ... XA09 are foreseen for memory ICs 32 K x 8 bits.

A variable assignment of the addresses to the memory positions as well as the use of RAM and EPROM memory types is only possible for the assembly positions XA10 ... XA13.

6.2.8.2 Setting the slots for the permitted memory blocks

Socket	Address area	Memory type RAM	Memory type Battery buffered RAM
XA00/XA01	50000 ... 5FFFF	X22	X22
XA02/XA03	60000 ... 6FFFF	8 o—o 7	8 o o 7
XA04/XA05	70000 ... 7FFFF	6 o o 5	6 o—o 5
		X22	X22
XA06/XA07	80000 ... 8FFFF		
XA02/XA03	90000 ... 9FFFF	4 o—o 3	4 o o 3
		2 o o 1	2 o—o 1

The jumper X24/1-2 is to be removed on principle in the battery-buffered mode. It may only be connected for test purposes.

Position	Addresses	Type	X18	X32, X33	X20, X21, X22
XA10, XA11 XA12, XA13	A0000 ... AFFFF	RAM 32K*8	1-2	7-8	see table
		or	3-4	3-4	in 6.2-10
	B0000 ... BFFFF	EPROM 32K*8			
	A0000 ... BFFFF	EPROM 64K*8	1-2	any	see table
	C0000 ... DFFFF	EPROM 64K*8			in 6.2-10
	B0000 ... BFFFF	RAM 32K*8	3-4	5-6	see table
		or			in 6.2-10
	C0000 ... CFFFF	EPROM 32K*8		1-2	
	A0000 ... AFFFF	RAM 32K*8		7-8	see table
		or			in 6.2-10
		EPROM 32K*8			and X21/19-20
	B0000 ... CFFFF	EPROM 64K*8			without X21/13-14

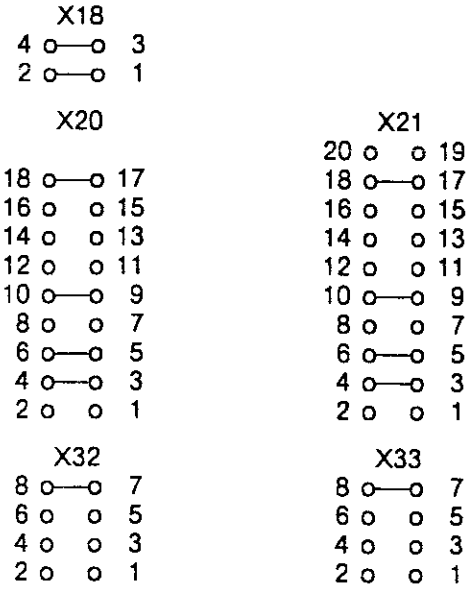
6.2.8.2 Setting the slots for the permitted memory blocks

Position	Memory blocks used			Battery buffer
	EPROM 32K*8	EPROM 64K*8	RAM 32K*8	RAM 32K*8
XA10	X20/15–16	X20/15–16		X20/17–18
			X20/17–18	X20/9–10
XA11	X20/7–8	X20/7–8	X20/9–10	X20/5–6
			X20/5–6	X20/1–2
	X20/11–12	X20/13–14	X20/3–4	
	X20/3–4	X20/3–4		
XA12	X21/15–16	X21/15–16		X21/17–18
			X21/17–18	X21/9–10
XA13	X21/7–8	X21/7–8	X21/9–10	X21/5–6
			X21/5–6	X21/1–2
	X21/11–12	X21/13–14	X21/3–4	
	X21/3–4	X21/3–4		

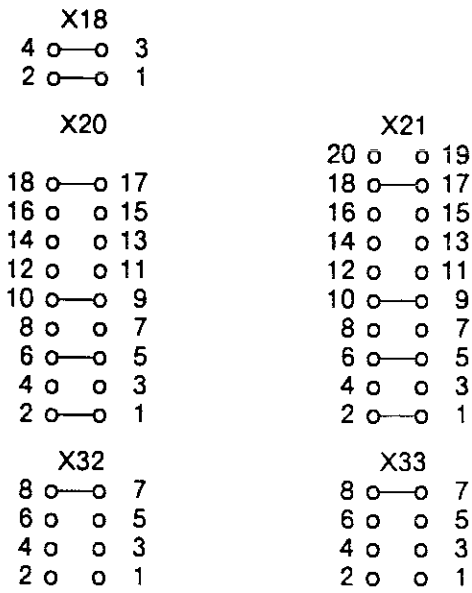
The jumper X24/1–2 is to be removed on principle in the battery-buffered mode. It may only be connected for test purposes.

Example:

Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	RAM 32kx8
XA12, XA13	B0000 ... BFFFF	RAM 32kx8

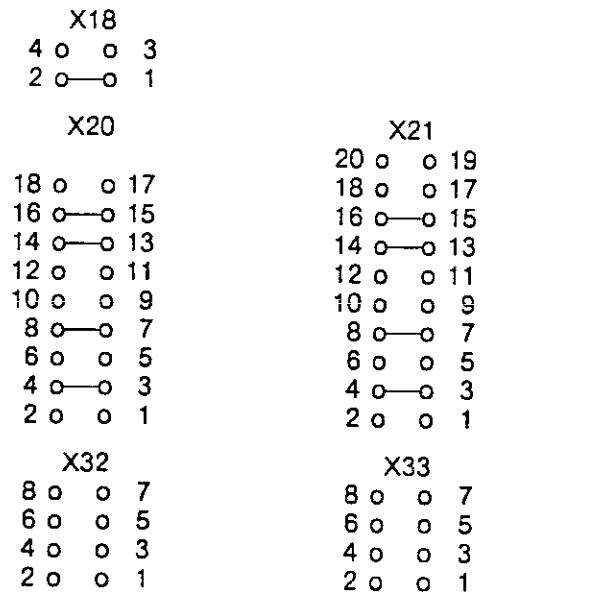


Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	RAM 32kx8 #
XA12, XA13	B0000 ... BFFFF	RAM 32kx8 #

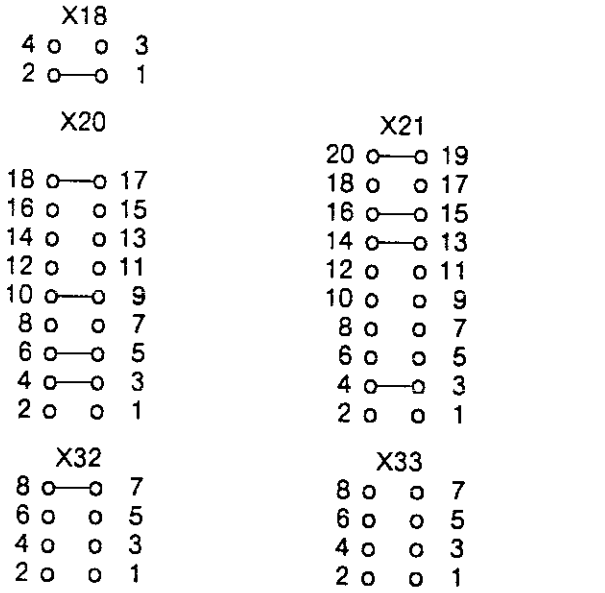


with a battery buffer

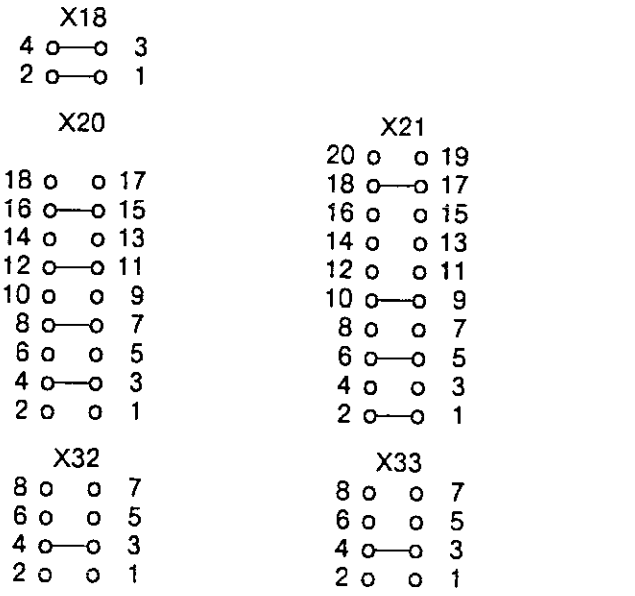
Socket	Address area	Memory type
XA10, XA11 XA12, XA13	A0000 ... BFFFF C0000 ... DFFFF	EPROM 64k*8 EPROM 64k*8



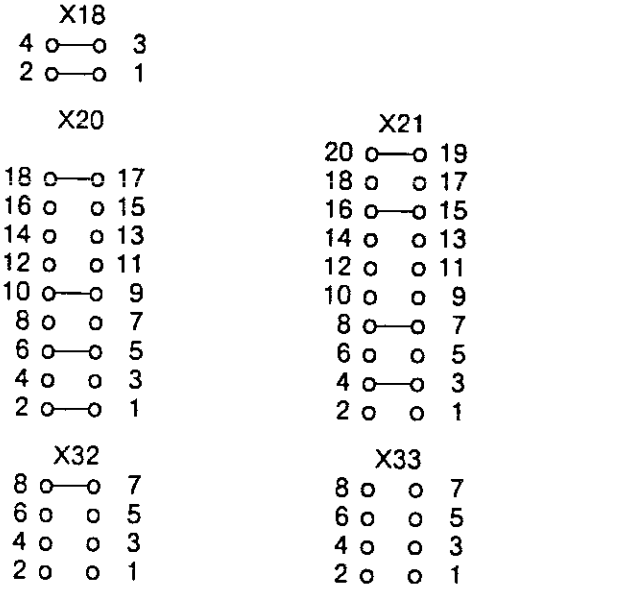
Socket	Address area	Memory type
XA10, XA11 XA12, XA13	A0000 ... AFFFF B0000 ... CFFFF	RAM 32k*8 EPROM 64k*8



Socket	Address area	Memory type
XA10, XA11 XA12, XA13	A0000 ... AFFFF B0000 ... BFFFF	EPROM 32k*8 RAM 32k*8 #



Socket	Address area	Memory type
XA10, XA11 XA12, XA13	A0000 ... AFFFF B0000 ... CFFFF	RAM 32k*8 # RAM 64k*8 #



with a battery buffer

6.2.8.3 Fading out the memory area

If the signal SA = 1 is output via the bit register, no access to the memory area is possible.

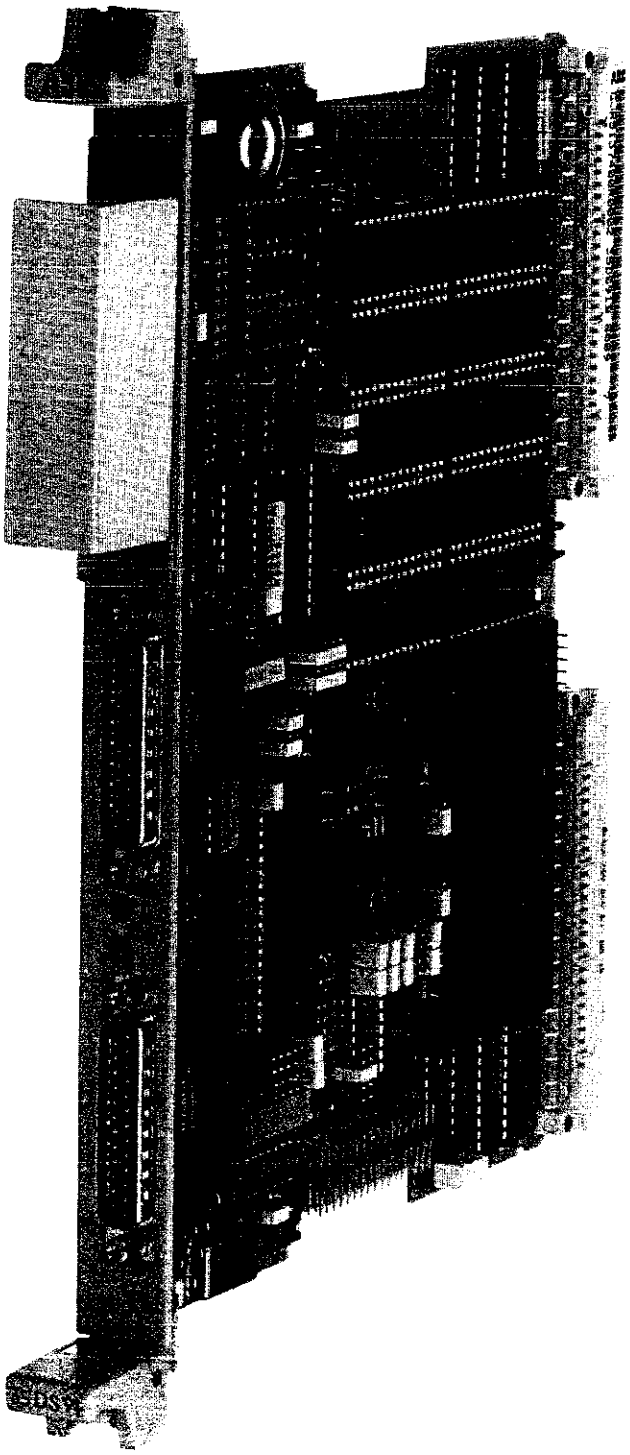
6.2.9 Application instructions

6.2.9.1 Cables, serial interface

When connecting the serial interface, attention is to be paid to the fact that the total current, which flows through the interface equals the total current, which flows out of the interface. If this is not observed, the integrated interference suppression coils do not function.

Attention is also to be paid to the fact that the screen is always put on one side only. This should be the side turned away from the 35 DS 91, if possible. If this is not possible, the screen is connected to the casing via the plugs X13 or X14. The maximum cable length for the RS423/RS4232C interface is 15 m. (See section 20.3.)

6.3 Data interface 35 DS 91 R2, R3



90 07 04

6.3.1 Technical data

Interface specification	RS 423 and RS 232 C **Note:** No display of the operating status of the serial interface using LED
Transfer rates	110, 300, 600, 1200, 2400, 4800, 9600, 19200 and 38400 baud **Note:** The transfer rate can only be set in common for the sender and receiver of one channel.
Channels	2
Handshakes	Hardware handshakes via 'request to send' and 'clear to send'; software handshake via XON and XOFF
Protocols	Asynchronic protocol with 1 start bit, 8 data bit, 1 stop bit, no parity bit. **Note:** Further asynchronic protocols can be programmed. Asynchronic, byte-synchronic, bit-synchronic transfer protocols can be programmed.

Functional scope of the unit rubrics:

Rubric 2	without memory blocks, without a real-time clock, without an interrupt controller, without a parity monitoring, without an interrupt controller, without iSBX plugs, without a lithium battery and without powerless sockets
Rubric 3	Includes the full functional scope of 35 DS 91, with memory blocks, with a real-time clock, with an interrupt controller, with a parity monitoring, with an interrupt controller, with iSBX plugs, with a lithium battery and with powerless sockets **Note:** The powerless sockets are IC sockets, with which the ICs are fixed via a screw attached to the socket. The iSBX plugs are required to connect multi-module boards.

Supply voltages:

U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+ 15 V ± 5 %
U_{B3} negative supply voltage	− 15 V ± 5 %
U_{SR} buffer voltage (lithium battery)	+ 2.9 V ... + 3.7 V

Supply currents with the full equipment:	Rubric R3 without an iSBX module	Rubric R2
I_{B1} for U_{B1}	0.8 A ± 30 %	0.5 A ± 30 %
I_{B2} for U_{B2}	0.1 A ± 30 %	0.1 A ± 30 %
I_{B3} for U_{B3}	0.1 A ± 30 %	0.1 A ± 30 %
Power dissipation	max. 10W	max. 7W
Ambient temperature	0 °C ... + 55 °C	
Storage temperature	− 25 °C ... + 75 °C	
Humidity rating	F	
Mechanical stress when installed	VDE 160	
Electromagnetic compatibility (EMC)	IEC 801	

Dimensions	1 pitch
Weight	1.0 kg
Order number	
Rubric R2	GJR5137410 R2
Rubric R3	GJR5137410 R3

Accessories:

Lithium battery 07 LB 20 R1	GJR5223500R1
Lithium battery module 35 LE 90 R1	GJR5146300R1

The figure on page 6.3-1 shows the unit 35 DS 91 rubric 2

6.3.2 Description

The data interface 35 DS 91 operates with the system bus of the processor card 35 ZP 93 R31, R41 (MHz version). Two 35 DS 91 or a combination of 35 DS 91 and 35 DS 90 can be connected to the processor card 35 ZP 93 via the system bus. The current supply of the data interface is received via the MPST bus

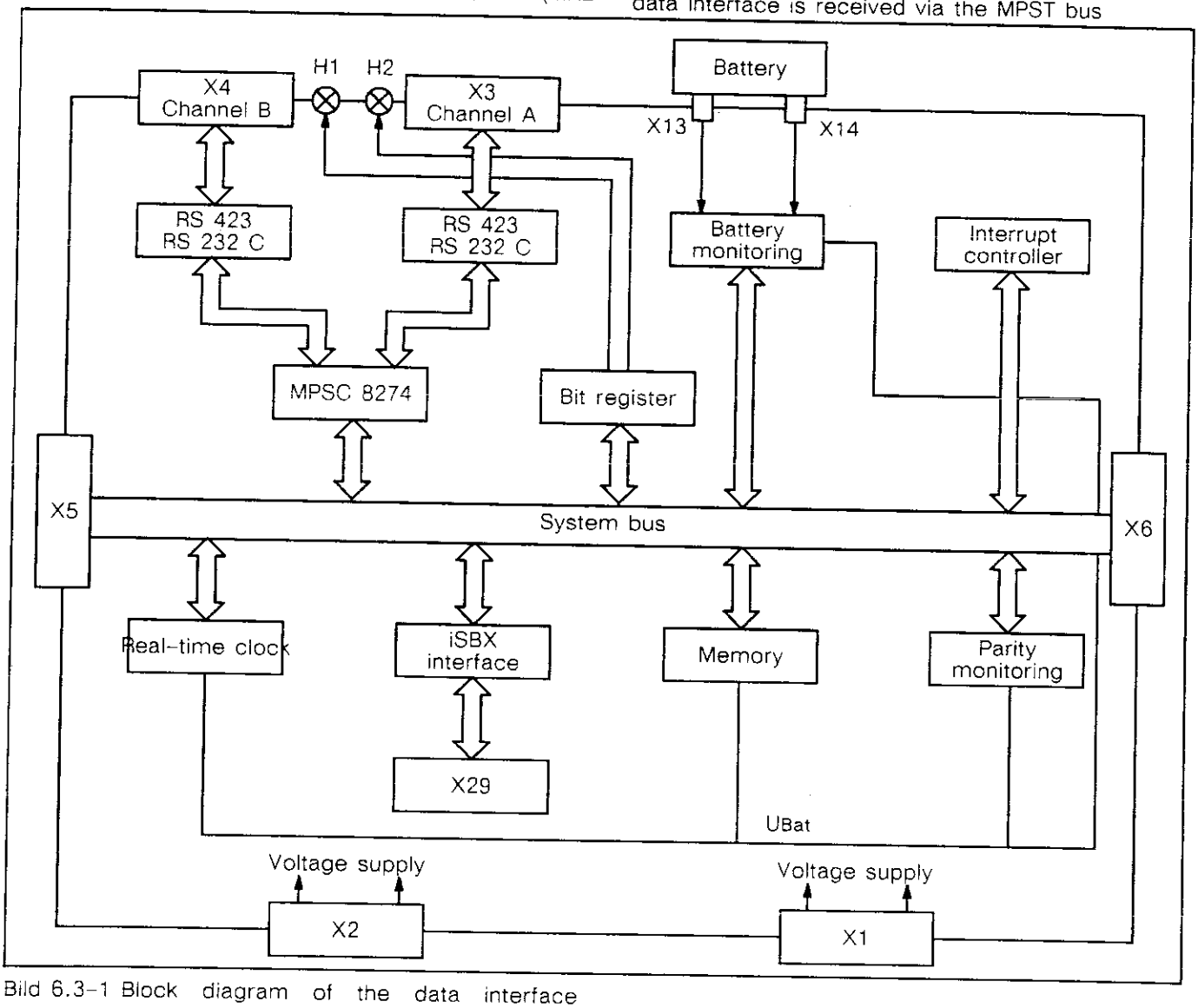


Bild 6.3-1 Block diagram of the data interface 35 DS 91

6.3.2.1 Memory

The data interface 35 DS 91 has a memory extension of max. 576 Kbytes. A total of 14 28-polar slots are available. Ten of these slots are foreseen for RAM and 4 slots selectively for RAM or EPROM. A parity monitoring is available for a memory area of 128 Kbytes (subscriber program and flags for PLC). The total memory positions can be buffered using a battery.

6.3.2.2 iSBX interface

A plug for multi-module boards from Messrs. Intel is attached to the processor card 35 ZP 93. Multi-module boards are functional units fixed on a printed board and can be plugged into the iSBX plug. The 35 DS 91 occupies two pitches in the subrack, when the multi-module board is plugged in.

6.3.2.3 Real-time clock

There is a battery-buffered real-time clock with a calendar on the 35 DS 91 for the protocol. The programmable time range stretches from 0.1 seconds to theoretically to 100 years. A separate pulse or a periodical clock can also be generated.

6.3.2.4 Battery and battery monitoring

The battery for buffering the clock, the RAM slots and the parity bit memory is attached to the front of the unit. Changing the lithium battery or the lithium unit is therefore possible without disconnecting the subassembly.

The battery monitoring is carried out via the software (see the software description).

6.3.2.5 Bit register

The bit register consists of an input multiplexer and an output register. Hardware signals and a 4 bit wide vector,which can be set with X19, are read using the input multiplexer.

Important signals are output for the hardware with the output register. A reset sets the bit register outputs to the status 0.

6.3.2.6 Interrupt controller

The interrupt controller 8259 on the data interface 35 DS 91 is driven as a slave block and is subordinate to the interrupt controller on the processor card 35 ZP 93.

6.3.2.7 Parity monitoring

The RAM memory address area 80000 ... 9FFFFH (socket XA6-XA9) is provided to secure the data stored here with a parity bit. Byte and word accesses can be executed. A parity error is displayed by initiating an interrupt as well as in the bit register (interrupt IR5 on the 8259 and address X400 in the bit register).

6.3.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

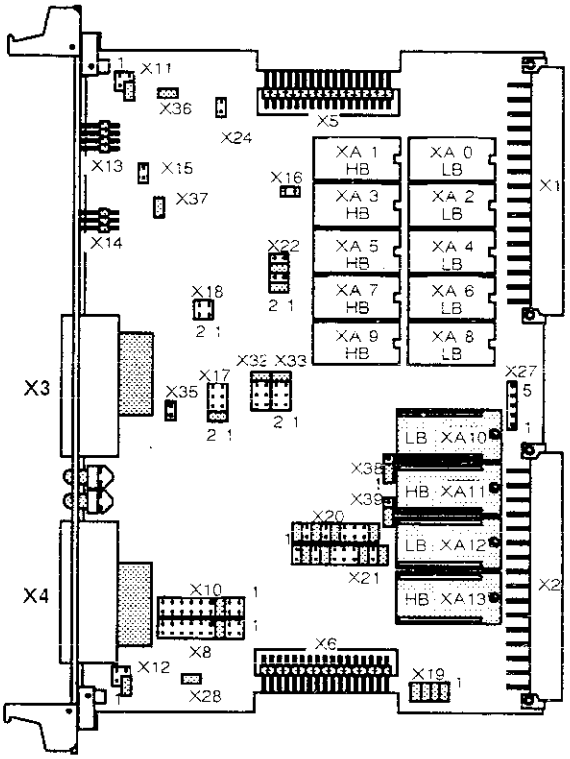


Fig. 6.3-2: Component side of the 35 DS 91 R2

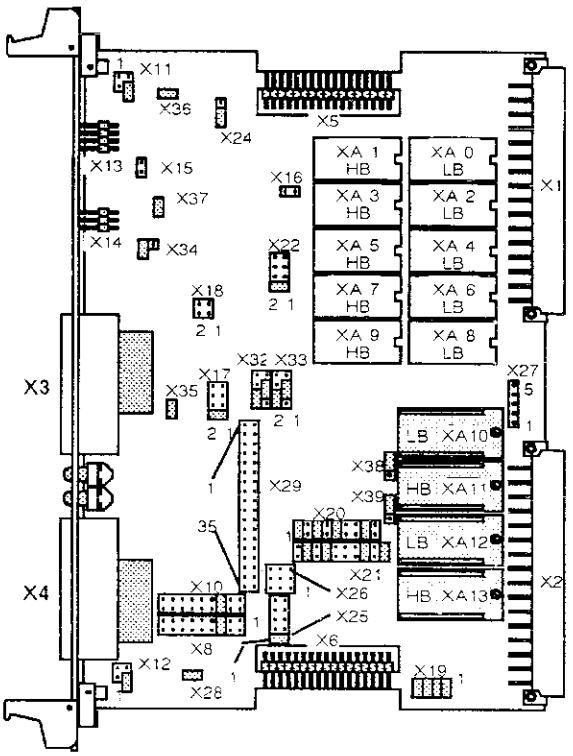


Fig. 6.3-3: Component side of the 35 DS 91 R3

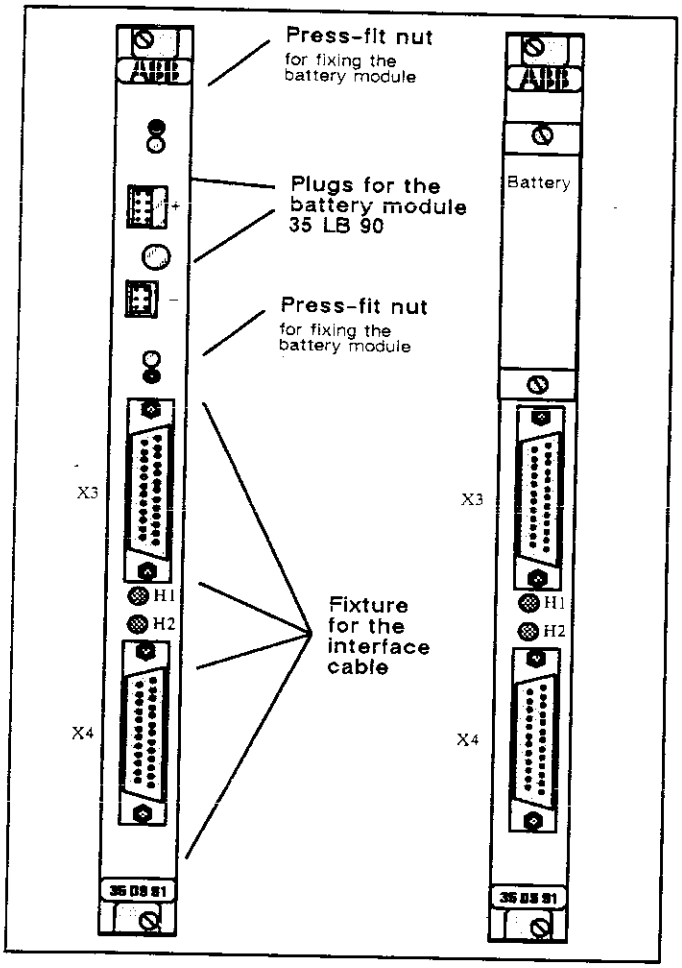


Fig. 6.3-4: Front panel with/without the battery module 35 LE 90

Overview of the interfaces, plugs and wrap

Code	Interface, plug	Design	Pole
X1	MPST bus (only current supply)	DIN41612, part 2C	32
X2	MPST bus (only current supply)	DIN41612, part 2C	32
X3	Serial interface channel A	Male connector	25
X4	Serial interface channel B	Male connector	25
X5	System bus to the 35 ZP 93	Flat cable	34
X6	System bus to the 35 ZP 93	Flat cable	34
X8	Baud rate channels A and B	Plug connector	27
X11	Connection: screen - 0 V	Plug connector	4
X12	Connection: screen - 0 V	Plug connector	4
X13	Battery contact: positive	Plug connector	8
X14	Battery contact: negative	Plug connector	6
X15	Basic load for the battery	Plug connector	2
X16	interrupt intern. clock	Plug connector *	2
X17	Unit address (3 various)	Plug connector	6
X18	Memory addresses	Plug connector	4
X19	Binary input for the bit register	Plug connector	8
X20	Battery buffering, memory type for XA 10, XA 11	Plug connector	18
X21	Battery buffering, memory type for XA 12, XA 13	Plug connector	20
X22	Battery buffering for XA 0 - XA 9	Plug connector	8
X24	Connection.: ground - /CS-RAM	Plug connector	2
X25	Interrupt 35 DS 91 - 35 ZP 93	Plug connector *	4
X26	Interrupt iSBX	Plug connector *	9
X27	Battery voltage MPST bus	Plug connector	5
X28	Oscillator frequency serial interface	Plug connector	2
X29	iSBX interface	Special plug *	36
X32	Memory address high byte	Plug connector	8
X33	Memory address low byte	Plug connector	8
X34	Parity error interrupt 35 ZP 93	Plug connector *	2
X35	Interrupt for serial interfaces	Plug connector *	2
X36	Interruption buffer capacitor	Plug connector	2
X37	Parity error test	Plug connector	2
X38	Select XA10, XA11	Plug connector	3
X39	Select XA12, XA13	Plug connector	3

* = only 35 DS 91 R3

6.3.4 Plug assignment

6.3.4.1 MPST interface, plugs X1, X2

The ACK line is a through connection.

Plug X1:

Pin	Signal name	Meaning
X1. 2a	UB1	5 V voltage
X1. 4a	UB1	5 V voltage
X1. 6a	UB3	-15 V voltage
X1.26a	-	-
X1.32a	ACKo	Acknowledge out
X1. 2c	UB1	5 V voltage
X1. 4c	UB1	5 V voltage
X1. 6c	UB2	15 V voltage
X1.26c	-	-
X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal name	Meaning
X2.22a	-	-
X2.30a	0 V	0 V voltage
X2.32a	0 V	0 V voltage
X2.22c	RS	Reset
X2.26c	-	-
X2.30c	0 V	0 V voltage
X2.32c	0 V	0 V voltage

6.3.4.2 Serial interfaces

Plug X3: Channel A

Pin	Signal name	Meaning	Operating mode	I/O
X3.1	screen	Protective ground		
X3.2	TxD	Transmit data	RS423, RS 232	O
X3.3	RxD	Receive data	RS423, RS 232	I
X3.4	RTS	Request to send	RS423, RS 232	O
X3.5	CTS	Clear to send	RS423, RS 232	I
X3.7	GND	Signal ground		
X3.20	DTR *	Data terminal Ready	RS423, RS 232	O

* DTR is logically 1 (online), after the voltage has been switched on

Plug X4: Channel B

Pin	Signal name	Meaning	operating mode	I/O
X4.1	screen	Protective ground		
X4.2	TxD	Transmit data	RS423, RS 232	O
X4.3	RxD	Receive data	RS423, RS 232	I
X4.4	RTS	Request to send	RS423, RS 232	O
X4.5	CTS	Clear to send	RS423, RS 232	I
X4.7	GND	Signal ground		
X4.20	DTR *	Data terminal Ready	RS423, RS 232	O

* DTR is logically 1 (on line), after the voltage has been switched on.

6.3.4.3 System bus

According to the assertion mentioned in 6.3.2 concerning the double effect between the data interfaces and the processor unit, attention is to be paid to the fact, that the memory area of 50000H ... DFFFFH is not assigned twice. This means that either the 35 DS 91 memory is blocked with the SA signal or the 35 DS 90 is operated without memory blocks.The remaining functions of the units can still be used. The ribbon cable required to connect the processor card and the data interface are enclosed with every data interface. The enclosed connecting set also includes the parts required for the mechanical connection of the data interface and processor card.

Plug X5:

Pin	Signal	Meaning	Pin	Signal	Meaning
X5. 1	$\overline{\text{MRDC}}$	Memory read	X5.18	–	–
X5. 2	$\overline{\text{IORC}}$	I/O read	X5.19	–	–
X5. 3	$\overline{\text{MWTC}}$	Memory write	X5.20	UB1	5 V voltage
X5. 4	A01	Address bit 01	X5.21	$\overline{\text{BHE}}$	Bus high byte
X5. 5	A03	Address bit 03	X5.22	A18	Address bit 18
X5. 6	A05	Address bit 05	X5.23	A16	Address bit 16
X5. 7	A07	Address bit 07	X5.24	A14	Address bit 14
X5. 8	A09	Address bit 09	X5.25	A12	Address bit 12
X5. 9	A11	Address bit 11	X5.26	A10	Address bit 10
X5.10	A13	Address bit 13	X5.27	A08	Address bit 08
X5.11	A15	Address bit 15	X5.28	A06	Address bit 06
X5.12	A17	Address bit 17	X5.29	A04	Address bit 04
X5.13	A19	Address bit 19	X5.30	A02	Address bit 02
X5.14	HLDA	Hold Acknowledge	X5.31	A00	Address bit 00
X5.15	UB1	5 V voltage	X5.32	Reserved	Special applications
X5.16	–	–	X5.33	$\overline{\text{AIOWC}}$	Adv. I/O write
X5.17	–	–	X5.34	Reserved	Special applications

Plug X6:

Pin	Signal	Meaning	Pin	Signal	Meaning
X6. 1	0 V	0 V voltage	X6.18	–	–
X6. 2	ALE	Address latch enable	X6.19	–	–
X6. 3	BEX	Line B exp.	X6.20	D14	Data bit 14
X6. 4	RES	Reset of the 8284A	X6.21	D12	Data bit 12
X6. 5	DEX	Line D exp.	X6.22	D10	Data bit 10
X6. 6	CAS0	CAS 0 of the 8259A	X6.23	D08	Data bit 08
X6. 7	CAS1	CAS 1 of the 8259A	X6.24	D06	Data bit 06
X6. 8	D01	Data bit 01	X6.25	D04	Data bit 04
X6. 9	D03	Data bit 03	X6.26	D02	Data bit 02
X6.10	D05	Data bit 05	X6.27	D00	Data bit 00
X6.11	D07	Data bit 07	X6.28	$\overline{\text{INTA}}$	Intr. acknowledge
X6.12	D09	Data bit 09	X6.29	AEX	Line A exp.
X6.13	D11	Data bit 11	X6.30	RDYi	Ready internally
X6.14	D13	Data bit 13	X6.31	CEX	Line C exp.
X6.15	D15	Data bit 15	X6.32	$\overline{\text{M/IO}}$	Memory/IO mode
X6.16	–	–	X6.33	$\overline{\text{HOLD}}$	Hold request
X6.17	–	–	X6.34	0 V	0 V voltage

The lines AEX, BEX, CEX and DEX must be wired up to the wrap zone X3 on the processor card 35 ZP 93 depending on their use.

Pin	Signalname	Meaning
1	+ 12 V	12 V voltage
2	– 12 V	– 12 V voltage
3	0 V	0 V voltage
4	UB1	5 V voltage
5	RESET	Reset
6	MCLK	10 MHz clock
7	A 2	Address signal 2
8	$\overline{\text{MPST}}$	Multi-module board installed
9	A 1	Address signal 1
10	–	Reserved
11	A 0	Address signal 0
12	INTR 1	Interrupt 1
13	$\overline{\text{AIOWC}}$	Advanced I/O write command
14	$\overline{\text{INTR 0}}$	Interrupt 0
15	$\overline{\text{IORD}}$	I/O read command
16	RDYi	Ready internally
17	GND	Signal GND
18	+ 5 V	+ 5 Volt
19	D 7	Data signal 7
20	$\overline{\text{MCS 1}}$	Chip select signal 1
21	D 6	Data signal 6
22	$\overline{\text{MCS 0}}$	Chip select signal 0
24	–	Reserved
25	D 4	Data signal 4
26	TDMA	Terminate DMA
27	D 3	Data signal 3
28	OPT 1	Option 1
29	D 2	Data signal 2
30	OPT 0	Option 0
31	D 1	Data signal 1
32	$\overline{\text{MDACK}}$	DMA acknowledge
33	D 0	Data signal 0
34	MDRQT	DMA request
35	GND	Signal GND
36	UB1	5 V voltage
37	D E	Data signal E
38	D F	Data signal F
39	D C	Data signal C
40	D D	Data signal D
41	D A	Data signal A
42	D B	Datasignal B
43	D 8	Datasignal 8
44	D 9	Datasignal 9

6.3.5 Settings in the I/O area

6.3.5.1 Setting the I/O addresses:

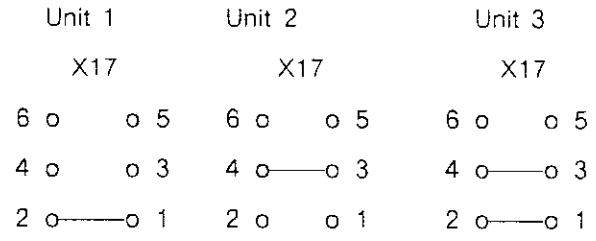
The interface 35 DS 91 can be operated together with the processor card 35 ZP 93 as unit 1, 2 or 3. The only differences are in the assignment of the I/O addresses to the function units.

A certain 35 DS 91, which is operated using the system bus of the processor card, is understood with the word "unit". The words "unit address" are the I/O addresses of the function units available on the data interface.

Note:
Only 2 data interfaces can be operated physically on the system bus.

The assignment of the respective unit number is carried out with the settings in the jumper zone X17:

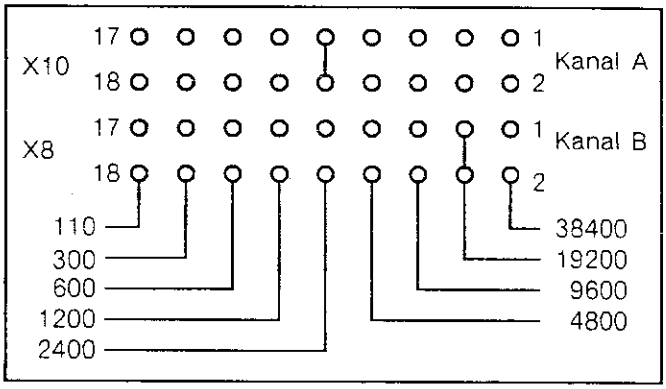
Jumper zone **X17**:



6.3.5.2 Serial interface

Baud rates;
Setting the baud rate is carried out using the jumper zone X8 and X10. The baud rates can be set independently of each other for channels A and B. The transmit and recieve baud rates of one channel can only be set together. The plug X28 serves to connect the clock oscillator and the serial interface and must always be plugged in.

Jumper zone **X8** and **X10**:



The given baud rates are only valid, if the MPSC block was programmed with an internal pitch factor of 16.

Set baud rate:
Channel A: Sender and receiver 2400 Baud
Channel B: Sender and receiver 19200 Baud

Basis address of the interface controller

Unit	I/O Basis address	Channel A Data	Channel A Command	Channel B Data	Channel B Command
1	0100 H	0100 H	0104 H	0102 H	0106 H
2	0400 H	0400 H	0404 H	0402 H	0406 H
3	1400 H	1400 H	1404 H	1402 H	1406 H

Note:
The subscriber address is set in the jumper zone **X17**.

0 V plug connection for RS232/RS422

Jumper zone **X11**:

1 - 2: The jumper connects the front panel with 0 V of the data interface.
1 - 3: The jumper connects the screen (X3/1) with the front panel.
3 - 4: The jumper connects the screen (X3/1) of the serial interface with 0 V of the data interface (electronics 0 V).

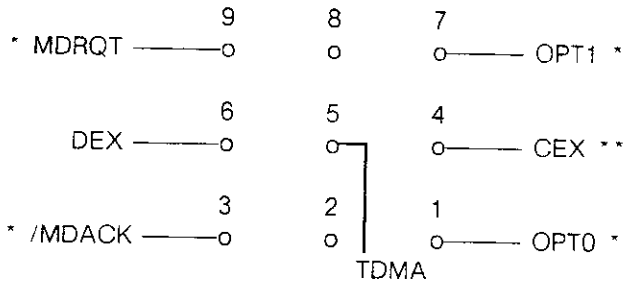
Jumper zone **X12**:

1 - 2: The jumper connects the front panel with 0 V of the data interface.
1 - 3: The jumper connects the screen (X4/1) with the front panel.
3 - 4: The jumper connects the screen (X4/1) of the serial interface with 0 V of the data interface (electronics 0 V).

6.3.5.3 iSBX interface

The iSBX interface does not require any special settings. Optional signals and DMA signals can be connected to the lines AEX and BEX in the jumper zone X26 in a special case of application.

Jumper zone **X26**:



* Signals for the iSBX interface
** to the 35 ZP 93 IR6 or IR7

6.3.6 Address overview

Address assignment for the 35 ZP 93 by the 35 DS 91

Address	Unit/medium	Position
DFFFF to 50000	Maximum memory capacity of the 35 DS 91	XA00 to XA13

Addresses in the I/O area of the 35 ZP 93

Function	X17 (5 o o 6 / 3 o o 4 / 1 o—o 2)	X17 (5 o o 6 / 3 o—o 4 / 1 o o 2)	X17 (5 o o 6 / 3 o—o 4 / 1 o—o 2)
Serial interface	0100...010F	0400...040F	1400...140F
Status bit register	2400...240F	3400...340F	4400...440F
Reserved for the clock	5400...540F 6400...640F		
Reserved for the interrupt controller	7400...740F	8400...840F	9400...940F
Reserved for the iSBX interface	A400...A40F B400...B40F	C400...C40F D400...D40F	E400...E40F F400...F40F

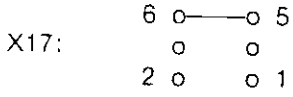
6.3.7 Settings

6.3.7.1 Real-time clock

The clock is supplied by the battery in the case of a voltage failure. All the functions are maintained. The clock is programmed or read out using 16 internal registers. The address area of the clock can be switched off with the jumper X17.

Switching on the real-time clock

Jumper zone **X17**:



Switching on the real-time clock: jumper X17/5-6

Switching off the real-time clock: no jumper

Data format of the real-time clock

D15 to D04	D03	D02	D01	D00
not occupied	X	X	X	X

X = 0 or 1

Register addresses of the clock

Register	Address A13	A03	A02	A01	Hex. Addr	Access
0 Control register	0	0	0	0	5400	R/W
1 tenth of a second	0	0	0	1	5402	Read
2 seconds	0	0	1	0	5404	R/W
3 ten seconds	0	0	1	1	5406	R/W
4 minutes	0	1	0	0	5408	R/W
5 ten minutes	0	1	0	1	540A	R/W
6 hours	0	1	1	0	540C	R/W
7 ten hours	0	1	1	1	540E	R/W
8 days	1	0	0	0	6400	R/W
9 ten days	1	0	0	1	6402	R/W
10 months	1	0	1	0	6404	R/W
11 ten months	1	0	1	1	6406	R/W
12 years	1	1	0	0	6408	R/W
13 ten years	1	1	0	1	640A	R/W
14 week day	1	1	1	0	640C	R/W
15 Clock setting interrupt reg.	1	1	1	1	640E	R/W

Attention:
The clock setting register and the interrupt register use the same address. In order to address one of the two registers, the data bit D01 must first be addressed in the control register.

Control register
(Address: 5400)

See also the following table.

Reading the control register:
The status of the data changed flag and the interrupt flag can be prompted. A reading access sets the flags to 0.

Data changed flag (D03):
D03 = 1 the data in the register for the tenths of a second has changed
D03 = 0 no data change in the register for the seconds

Interrupt flag (D00):
D00 = 1 interrupt has taken place

D00 = 0 interrupt has not taken place

Writing the control register:

Test bit (D03):
Various time registers are directly connected to the clock cycle of 32.768 kHz in the test mode. The clock can be tested with a higher speed.

Clock Start/Stop (D02):
starting or stopping the real-time clock.

Interrupt select (D01):
Only one common address is available for the clock setting register and the interrupt register. The interrupt register can only be addressed, if D01 of the control register has the value 1

Interrupt Start/Stop (D00):
starting or stopping the interrupt mode

Access	D03	D02	D01	D00
Read	Data changed Flag	0	0	Interrupt Flag
Write	Test 0 = Normal 1 = Test mode	Clock start/stop 0 = Clock run 1 = Clock stop	Interrupt select 0 = Clock set reg. 1 = Interruptregister	Interrupt start/stop 0 = Interrupt start 1 = Interrupt stop

Clock setting register
(Address: 640EH and control register D01 = 0)

Function	Data D03	D02	D01	D00	Comment	Access
Leap year counter	X	X			0=Leap year	R/W
AM/PM Indicator			X		0=AM 1=PM	R/W
(12 hourly)					0 in 24 hours	
12/24 hours				X	0=12 hours 1=24 hours	R/W

Note:
Hour select bit and AM/PM select bit cannot be set in the same writing operation.

Leap year counter:
The leap year counter (D03, D02) is a binary counter with two levels.

The counter must be initialised with the number of years passed since the last leap year.

Example: Initialisation 1987 → Value 3 must be written into the counter, since 1984 was the last leap year.

Interrupt setting register
(Address: 640EH and control register D01 = 0)

Function	Control word D03	D02	D01	D00	Comment
No interrupt	X	0	0	0	interrupt output deleted, Start/stop byte=1
0.1 seconds	0/1	0	0	1	
0.5 seconds	0/1	0	1	0	
1 second	0/1	1	1	1	
5 seconds	0/1	1	0	0	
10 seconds	0/1	1	0	1	
30 seconds	0/1	1	1	0	
60 seconds	0/1	1	1	1	

X = 0 Single Interrupt
X = 1 Repeated Interrupt

The clock interrupt is guided to input I2 of the interrupt controller. A signal change of the clock interrupt from 0 to 1 displays the end of the interrupt time.

Single interrupt:
The clock interrupt is executed only once after the start (D00 = 0). Attention is to be paid that the interrupt flag is set to 0 before the start or before the end of the interrupt time (by reading the control register). If this is not observed, no interrupt can be initiated.

Repeated interrupt:
The repeated interrupt is executed after the start, if the data bit D03 is set to 1 in the interrupt setting register. The corresponding flag must be set to 0 before the end of the interrupt time and after the start of the repeated interrupt. This must also occur after every interrupt.

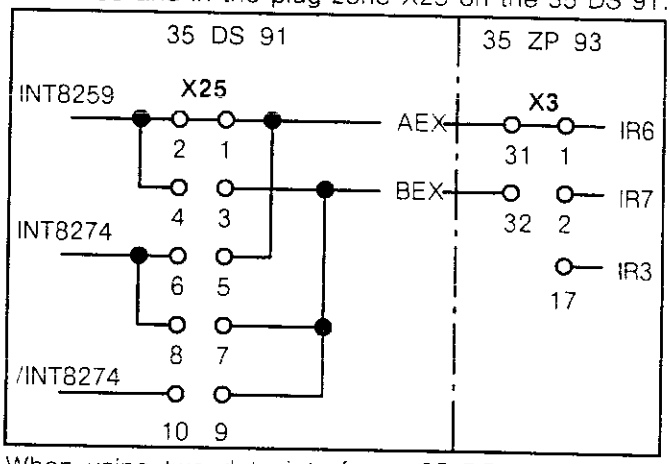
No interrupt:
D00 = 0
D01 = 0
D02 = 0
D03 without effect

6.3.7.2 Interrupt controller

Interrupt inputs

Internal input	Code	Meaning
IR 0	INTR 0	Interrupt 0 of the iSBX plug
IR 1	INTR 1	Interrupt 1 of the iSBX plug
IR 2	IR-CLOCK	Interrupt of the clock block
IR 3	INT-8274	Interrupt of the serial interface
IR 4	BATOK	Battery is OK
IR 5	PF	Parity error signal
IR 6	GND	Non-used input
IR7	GND	Non-used input

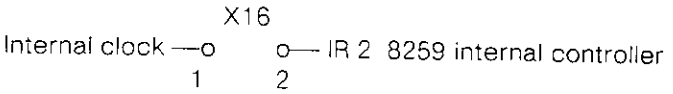
Interrupt wiring to the processor unit 35 ZP 93
The interrupt controller on the data interface operates as a slave controller. An interrupt message of the slave controller is guided to the master interrupt controller of the processor card 35 ZP 93 via the lines AEX or BEX. The connection is produced in the wrap zone X3 on the 35 ZP 93 and in the plug zone X25 on the 35 DS 91.



When using two data interfaces 35 DS 91, one unit uses the interrupt IR 7, for example, and the other one the interrupt IR 6.

Interrupt wiring of the parity equipment
If the interrupt controller is not assembled on the data interface, the interrupt of the parity equipment (PF) can be connected directly to the interrupt controller on the processor card 35 ZP 93.

Interrupt wiring of the real-time clock
The clock interrupt can be interrupted by the jumper zone **X16**.



6.3.7.3 Status bit register

This is an 8 bit reading and writing status register. The basic address can be set in the I/O area on 240X, 340X and 440X.

Data format of the bit register

The in- and outputs of the bit register are only connected with the data line D0.

D15 to D01	D00
Not occupied	X

X = 0 or 1

All these status bit registers (outputs) are deleted after a reset.

Function and addresses of the status bit register

Address	Signal	access	Function of data bit 0
X400	PF	read	0 = Parity error
	PFEN	write	1 = Switching on the parity output
X402	MPST	read	0 = iSBX module installed Not used
X404	SA	read	0 = total memory area faded out
	SA	write	0 = Switching off the total memory area
X406	$\overline{\text{BATOK}}$	read	1 = Battery voltage < 2.9 V
	BATQ	write	1 = "Battery change" acknowledgement
		write	0 = Operating status
X408	I4	read	Binary input: 0 = Jumper X19/7-8
		write	Not used
X40A	I3	read	Binary input: 0 = Jumper X19/5-6
		write	Not used
X40C	I2	read	Binary input: 0 = Jumper X19/3-4
	H2	write	1 = LED (H2) ON
X40E	I2	read	Binary input: 0 = Jumper X19/1-2
	H1	write	1 = LED (H1) ON

* For the ABB Procontic T300 PLC, the following means:

Address X40E: 0 = "Siebert telegram"
1 = 'ASCII telegram'

X = One of 3 unit addresses, which can be set in the jumper zone X19.

Signal SA:

This can be set and prompted as a single signal using the bit register.

SA = 1: The memory area on the 35 DS 91 cannot be addressed.
SA = 0: The memory area can be addressed.

Binary input (X19):

A four-digit binary value can be set in the jumper zone X19 and prompted using the bit register.

See the function and addresses of the status bit register.

6.3.7.4 Parity monitoring

The address area 80000 ... 9FFFFH is foreseen to store data in the battery-buffered RAM (these are the subscriber program UP and the flags for the PLC). A parity monitoring with a battery-buffered parity bit RAM is also available for this address area. The output register of the parity equipment is activated by setting the signal PFEN using the bit register.

Functional table

Parity after the reading cycle	PFEN	PF
Error	1	0
OK	1	1
No evaluation	0	1

PFEN = Switching on/off the parity error output

Using the parity monitoring

Reading data:

The parity bit is automatically formed and saved when writing onto the parity-secured memory area. No settings are to be made at all.

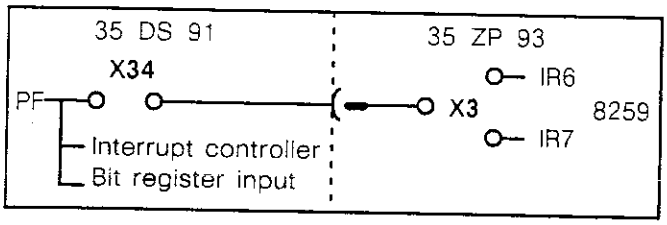
(For the assembly of the slots foreseen here, see 6.3.8.2)

Reading out data:

If data are read out of the secured memory area, PFEN = 1 is to be output first using the bit register (D0 = 1). The parity result can now be prompted after every reading procedure using the bit register and initiate an interrupt. A parity error must be reset by outputting PFEN = 0 (address : X400 = 0).

Registering a parity error

The output of the parity error register is guided to an interrupt controller input, a bit register input and the jumper zone X34. If there is no interrupt controller on the 35 DS 91, an interrupt can be initiated on the processor card 35 ZP 93 using the line BEX.



6.3.7.5 Battery monitoring

Battery monitoring signals

$\overline{\text{BATOK}}$:

This signal is produced by the battery monitoring switch and can be prompted using the bit register or initiate an interrupt via the interrupt controller.

- $\overline{\text{BATOK}}$ = 0 The battery is OK, battery voltage > 2.9 V
- $\overline{\text{BATOK}}$ = 1

o Battery is not present
o Battery voltage < 2.9 V
o The new battery is present but the battery change was not yet acknowledged with BATQ.

BATQ: Battery acknowledgement

BATQ is an input signal for the monitoring switch of the battery and is produced by the bit register. The correct use of this signal completes a battery change.

- BATQ = 0 is the status, which is always to be assumed after an acknowledgement.
- BATQ = 1 means that a battery change must be acknowledged with BATQ = 1 (output via the bit register, address : X406 = 1). BATQ is to be set to 0 again afterwards.

6.3.8 Settings in the memory area

6.3.8.1 Setting the memory addresses

The assignment of the memory addresses to the corresponding assembly positions for the memories is carried out in the wrap zones X18, X32 and X33.

The settings for the memory type used and a battery buffer can also be carried out in the wrap zones X20, X21 and X22 (see also the following tables).

The even position numbers (XA00, XA02, etc.) are the low bytes.

The odd position numbers (XA01, XA03, etc.) are the high bytes.

The assembly positions XA00 ... XA09 are foreseen for memory ICs 32 K x 8 bits.

A variable assignment of the addresses to the memory positions as well as the use of RAM and EPROM memory types is only possible for the assembly positions XA10 ... XA13.

6.3.8.2 Setting the slots for the permitted memory blocks

Socket	Address area	Memory type RAM	Battery buffered RAM
XA00/XA01	50000 ... 5FFFF	X22	X22
XA02/XA03	60000 ... 6FFFF	8 o——o 7	8 o o 7
XA04/XA05	70000 ... 7FFFF	6 o o 5	6 o——o 5
		X22	X22
XA06/XA07	80000 ... 8FFFF	4 o——o 3	4 o o 3
XA08/XA09	90000 ... 9FFFF	2 o o 1	2 o——o 1

The jumper X24/1-2 is to be removed on principle in the battery-buffered mode. It may only be plugged in for test purposes.

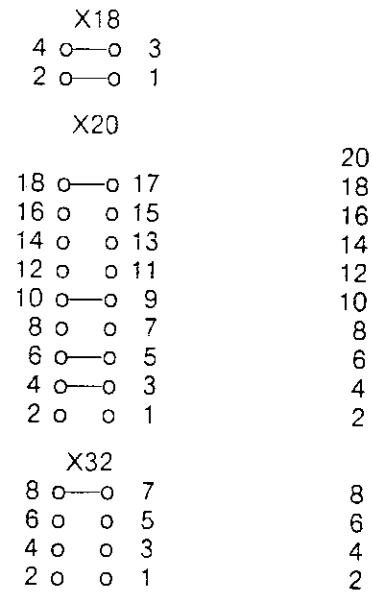
Positions	Addresses	Type	X18	X32, X33	X20, X21, X22
XA10, XA11 XA12, XA13	A0000 ... AFFFF	RAM 32K*8	1-2	7-8	see tables
		or	3-4	3-4	in 6.3.8.2
	B0000 ... BFFFF	EPROM 32K*8			
	A0000 ... BFFFF	EPROM 64K*8	1-2	any	see tables
	C0000 ... DFFFF	EPROM 64K*8			in 6.3.8.2
	B0000 ... BFFFF	RAM 32K*8	3-4	5-6	see tables
		or			in 6.3.8.2
	C0000 ... CFFFF	EPROM 32K*8		1-2	
	A0000 ... AFFFF	RAM 32K*8		7-8	see tables
		or			in 6.3.8.2 32K*8
		EPROM 32K*8			and X21/19-20
	B0000 ... CFFFF	EPROM 64K*8			without X21/13-14

Position	Memory blocks used		Battery buffer	
	EPROM 32K*8	EPROM 64K*8	RAM 32K*8	
XA10	X20/15-16	X20/15-16		X20/1-2
			X20/17-18	
XA11	X20/7-8	X20/7-8	X20/9-10	Jumper X20/3-4
			X20/5-6	is to be removed
	X20/11-12	X20/13-14	X20/3-4	
	X20/3-4	X20/3-4		
XA12	X21/15-16	X21/15-16		X21/1-2
			X21/17-18	
XA13	X21/7-8	X21/7-8	X21/9-10	Jumper X21/3-4
			X21/5-6	is to be removed
	X21/11-12	X21/13-14	X21/3-4	
	X21/3-4	X21/3-4		

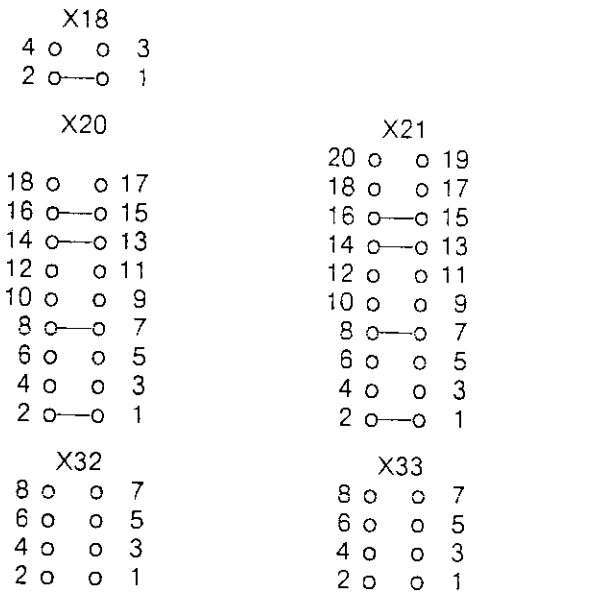
The jumper X24/1-2 is to be removed on principle in the battery-buffered mode. It may only be connected for test purposes.

Examples:

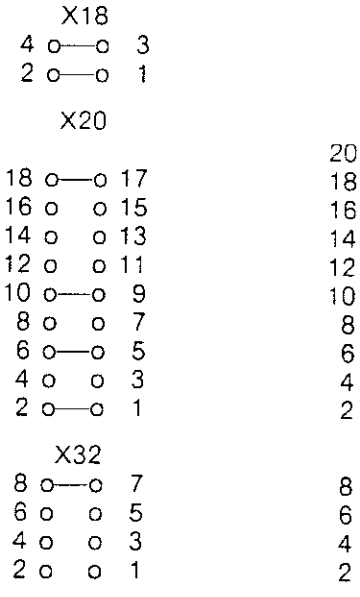
Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	RAM 32k*8
XA12, XA13	B0000 ... BFFFF	RAM 32k*8



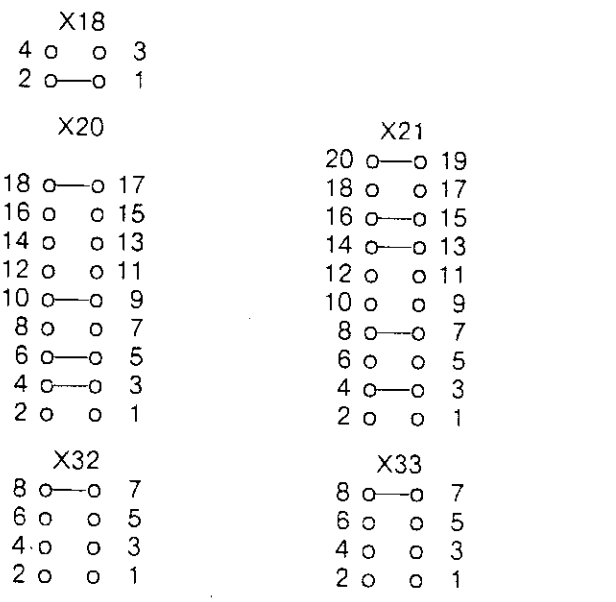
Socket	Address area	Memory type
XA10, XA11	A0000 ... BFFFF	EPROM 64k*8
XA12, XA13	C0000 ... DFFFF	EPROM 64k*8



Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	RAM 32k*8 #
XA12, XA13	B0000 ... BFFFF	RAM 32k*8 #



Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	RAM 32k*8
XA12, XA13	B0000 ... CFFFF	EPROM 64k*8



with a battery buffer

Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	EPROM 32k*8
XA12, XA13	B0000 ... BFFFF	RAM 32k*8 #

X18

4 o—o 3
2 o—o 1

X20

18 o o 17
16 o—o 15
14 o o 13
12 o—o 11
10 o o 9
8 o—o 7
6 o o 5
4 o—o 3
2 o o 1

X21

20 o o 19
18 o—o 17
16 o o 15
14 o o 13
12 o o 11
10 o—o 9
8 o o 7
6 o—o 5
4 o o 3
2 o—o 1

X32

8 o o 7
6 o o 5
4 o—o 3
2 o o 1

X33

8 o o 7
6 o o 5
4 o—o 3
2 o o 1

Socket	Address area	Memory type
XA10, XA11	A0000 ... AFFFF	RAM 32k*8 #
XA12, XA13	B0000 ... CFFFF	RAM 64k*8 #

X18

4 o—o 3
2 o—o 1

X20

18 o—o 17
16 o o 15
14 o o 13
12 o o 11
10 o—o 9
8 o o 7
6 o—o 5
4 o o 3
2 o—o 1

X21

20 o o 19
18 o—o 17
16 o o 15
14 o o 13
12 o o 11
10 o—o 9
8 o o 7
6 o—o 5
4 o o 3
2 o—o 1

X32

8 o—o 7
6 o o 5
4 o o 3
2 o o 1

X33

8 o—o 7
6 o o 5
4 o o 3
2 o o 1

with a battery buffer

6.3.8.3 Fading out the memory area

If the signal SA = 1 is output via the bit register, accessing the memory area cannot be carried out.

6.3.9 Application instructions

6.3.9.1 Cable, serial interface

Attention is to be paid when connecting the serial interface, that the sum of the currents, which flow into the interface, equals the sum of the currents, which flow out of the interface. If this is not observed, the integrated interference suppression coils do not function.

Attention is also to be paid that the screen is always put on only one side. This should be on the side turned away from the 35 DS 91, if possible. If this is not possible, the screen is connected to the casing via the plugs X13 or X14. The maximum cable length for the RS423/RS4232C interface is 15 m. (see section 20.3.)

7 Memory cards

35 PS 91 R12: Memory card without error detection, 32 KBytes assembly.
35 PS 91 R13: Memory card with error detection, 128 KBytes assembly.
35 PS 91 R14: Memory card with error detection, 128 KBytes assembly.
35 PS 91 R22: Memory card without error detection, 512 KBytes assembly.

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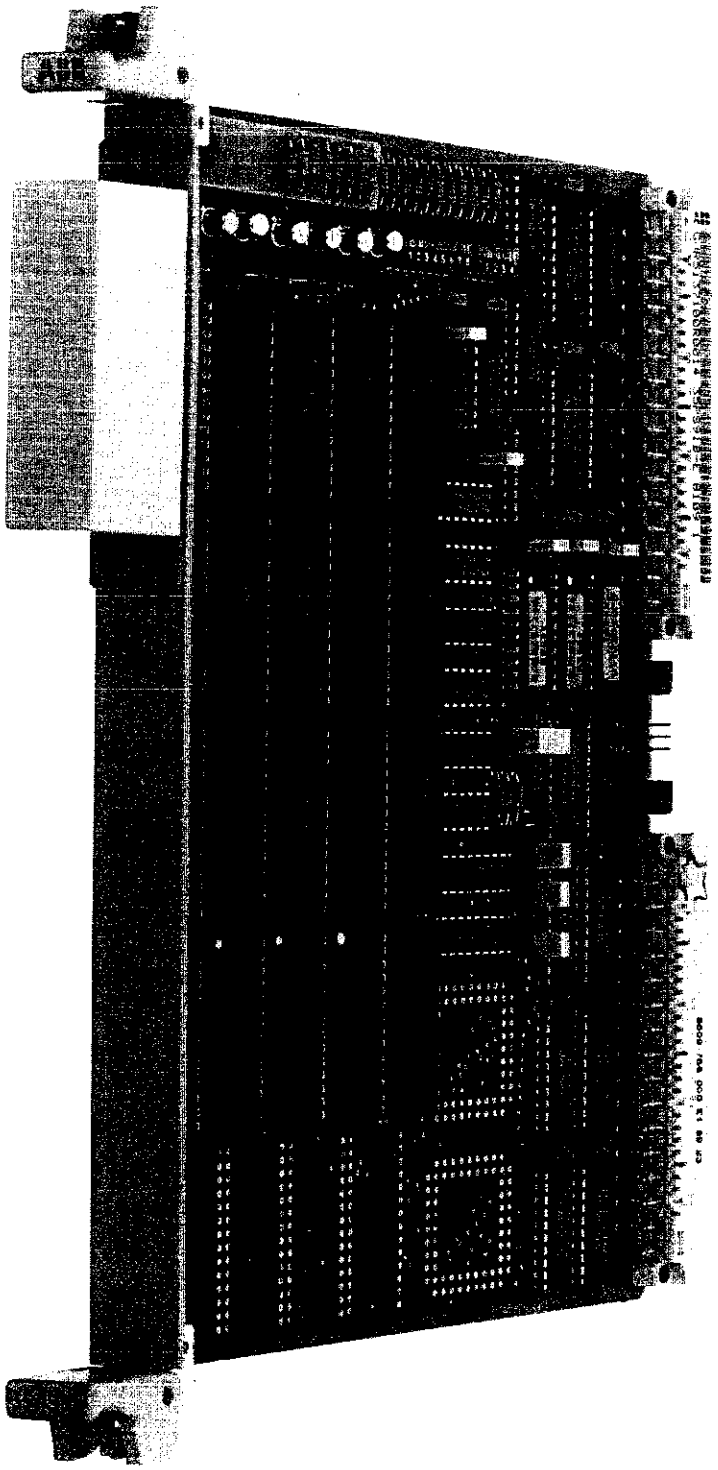
7.1 Memory card 35 PS 91 R12, R13 and R14



90 01 76

7.1.1 Technical data

Memory capacity	max.128 kbytes	
U_{b1} positive supply voltage	+ 5 V ± 5 %	
U_{SR} buffer voltage (lithium battery)	+ 2.9 V < U_{SR} < + 3.7 V	
	with error detection	without error detection
I_{B1} for U_{B1}	typically 1.5 A ± 20 %	typically 1.1 A ± 20 %
I_{SR} for U_{SR}	typically 30 µA ± 50 %	typically 30 µA ± 50 %
Power loss	7.5 W ± 20 %	5.5 W ± 20 %
Ambient temperature	0 °C ... + 55 °C	
Storage temperature	- 25 °C ... + 75 °C	
Humidity rating	F	
Mechanical stress when installed	VDE 160	
Writing or reading cycle from $\overline{BOV}$=0 to RDY=1	200 ns < T < 300 ns	
Input values	according to DIN 66 264	
Output values	according to DIN 66 264	
Dimension	1 pitch	
Weight	0.4 kg	
Order number for		
35 PS 91 R12, without error detection, 32 kbytes assembly	GJR5137100R12	
35 PS 91 R13, with error detection,128 kbytes assembly	GJR5137100R13	
35 PS 91 R14, without error detection, 128 kbyte assembly	JR5137100R14	
Accessories:		
Lithium battery 07 LB 20 R1	GJR5223500R1	
Lithium battery unit 35 LE 90 R1	GJR5146300R1	

7.1.2 Description

The battery-buffered CMOS memory card 35 PS 91 is a passive subscriber on the MPST bus.

7.1.2.1 Application

The unit serves as a data memory for

- CNC part programs
- RAM disk for the industrial computer
- MDS machine data sentences, etc.

7.1.2.2 Features

- Extension levels of the memory card: 32, 64, 96 and 128 kbytes.
- 16 pages for every 8 kbytes can be addressed.
- The memory card can be read in bytes or words.
- 1 ... 7 units can be operated at the same time.
- Option: automatic error detection and correction.

Note : the figure on page 7.1-1 shows the 35 PS 91 R14

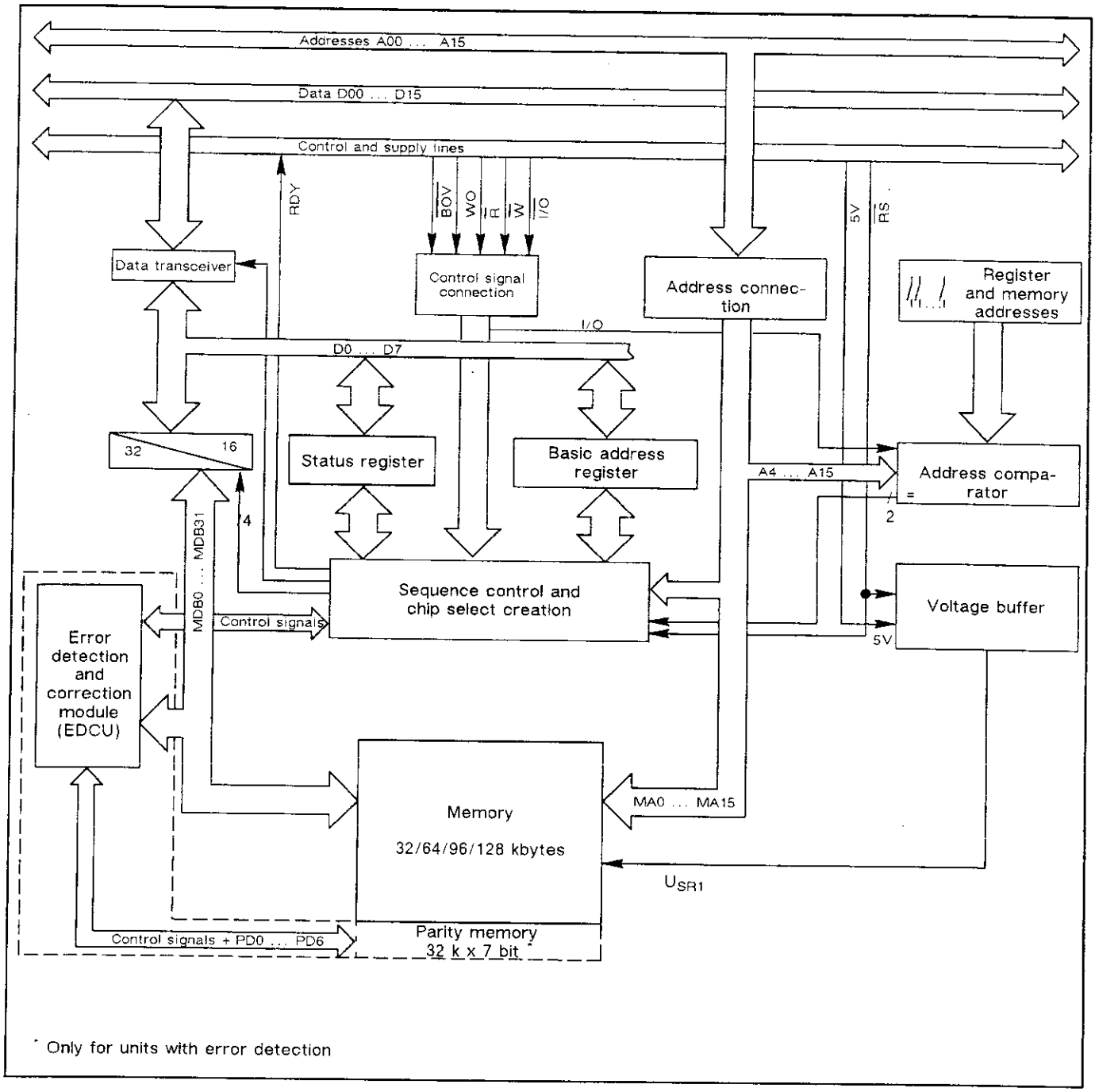


Fig. 7.1-1: Block diagram of the memory card 35 PS 91

7.1.2.3 Addresses

56 kbytes address capacity is available for the data memory on the MPST bus. A maximum of 7 units can be accommodated in this area. Each unit then has a window of 8 kbytes. 16 pages for every 8 kbytes can be applied to this window by an internal switchover on the card, which can be addressed. The maximum memory extension with 7 units amounts to 7 x 16 x 8 kbytes = 7 x 128 kbytes = **896 kbytes**.

7.1.2.4 Basic register

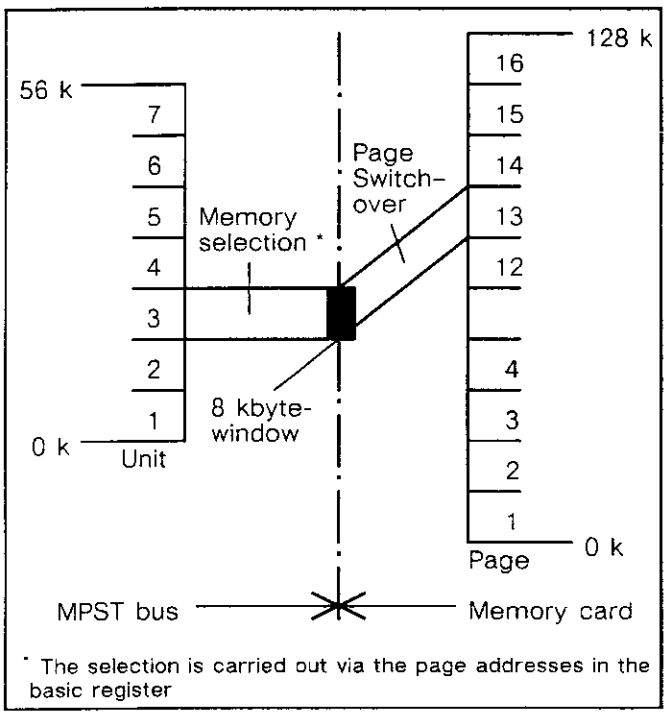
Every memory card has a basic register, which can be addressed like an I/O unit in the area of 56 ... 64 kbytes.

The 8 bit basic register gives information concerning:

- Page addresses: Bit D07 ... D04
- Operating modes:
  - * Format bit Bit D03
  - * Error bit Bit D01
  - * Occupied bit Bit D00

Bit D02 is not used.

Internal switchover, which can be addressed:



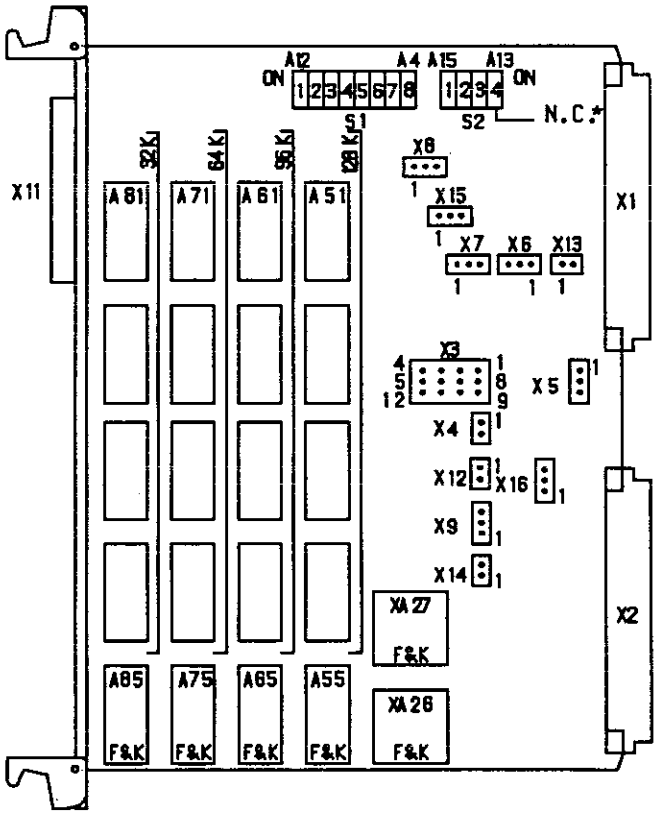
* The selection is carried out via the page addresses in the basic register

7.1.2.5 Battery

The battery for buffering the RAM slots are attached on the front panel of the unit. Changing the lithium battery or the lithium battery module is therefore possible without disconnecting the module (see also chapter 21.4 and 21.5).

7.1.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.



*N.C. = Not Connected

F & K is only assembled for units, which are equipped with error detection and error correction.

Fig. 7.1-2: Component side (top view)

7.1.4 MPST bus interfaces, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transmission	X1.24c	–	–
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	–	–	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

7.1.5 Addressing the memory

Addressing the memory includes 3 stages

- Memory selection via the MPST bus (A15 ... A13) — 1 of 7
- Page selection via the basic register (D07 ... D04) — 1 of 16
- Addressing the memory via the MPST bus (A12 ... A00) — 0 ... 8 kbytes

7.1.5.1 Memory selection

Distinguishing between 1 ... 7 units is carried out in the address area 0 ... 56 kbytes, which is foreseen for addressing the memory in accordance with the MPST bus determination. The memory card address is set with the switch S2.

Note:
The switch position ON logically corresponds to 0.

The switches S2.1 ... S2.3 are compared with the bits A15 ... A13 on the MPST bus.

Unit	Window	Switch 1 2 3 4	Address area
1	0 ... 8 kbytes	on on on d	0000H...1FFFH
2	8 ... 16 kbytes	on on off d	2000H...3FFFH
3	16 ... 24 kbytes	on off on d	4000H...5FFFH
4	24 ... 32 kbytes	on off off d	6000H...7FFFH
5	32 ... 40 kbytes	off on on d	8000H...9FFFH
6	40 ... 48 kbytes	off on off d	A000H...BFFFH
7	48 ... 56 kbytes	off off on d	C000H...DFFFH
–	prohibited*	off off off d	–

d = Switch position is insignificant
* reserved for the ABB Procontic T300 data channel area

7.1.5.2 Data channel address

The data channels, with which the basic register can be read or written, are between 57 and 64 kbytes in the upper address area in accordance with the MPST bus determination.

Each unit has a data channel address assigned to it via switch S1. The separate data channels are addressed by the MPST bus via A00 ... A03.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	Y	Y	Y	Y	Y	Y	Y	Y	Z	Z	Z	Z
ABB Procontic T300 code for the upper address area				1	2	3	4	5	6	7	8				
				Switch S1											

1 = permanently wired up
X = can be set with plug-in jumper X7
X7.1 - X7.2: A12 = 0
X7.2 - X7.3: A12 = 1 (Factory presetting)
Y = the data channel address of the card can be set with the switch S1.

Note:
The switch position ON logically corresponds to 0.
Z = Adressing the separate data channels. 3 channels are evaluated on the card:

The following operations are permitted in the separate channels:

	Channel address				Data in the basic register							
	A03	A02	A01	A00	D07	D06	D05	D04	D03	D02	D01	D00
Channel 0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Channel 2	0	0	1	0	R	R	R	R	R	R	R/W	R
Channel 4	0	1	0	0	R	R	R	R	R	R	R	R/W

R = Reading; W = Writing

7.1.5.3 Page selection

After addressing the memory card as an I/O unit (see point 7.1.5.2), the page address is loaded into the basic register via the data channel 0.

Basic register:

Page addresses 1 ... 16				Operating modes (not important for the page selection)			
D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	without error detection			
	:			d	d	d	d
	:			with error detection			
1	1	1	1	1	d	d	d

d = insignificant

7.1.5.4 Addressing the memory

The page, which is 8 kbytes large, is selected via the page address and addressed by the MPST bus with A12 ... A00 after the selection of the unit via A15 ... A13 (see point 7.1.5.1).

7.1.6 Operating modes

3 operating status are to be observed:

- Formating — only important for units with error detection and error correction
- Error detected — only important for units with error detection and error correction
- Card occupied

7.1.6.1 Occupied bit D00

The occupied bit D00 can be activated with the jumper X9.

Jumper zone **X9**:

1 - 2 The card is always active after the RESET (factory presetting).

2 - 3 The card is switched on or off by the MPST bus via D00.
Address: Data channel 4

D00 = 0: The unit is not active
D00 = 1: The unit is active

7.1.6.2 Error bit D01

The error bit is only effective for units with error detection and error correction.

D01 = 0: No error
D01 = 1: Error

If D01 = 1, an error, which cannot be corrected, occurred with a previous memory access. This error is displayed, until it is acknowledged.

The acknowledgement is carried out by addressing the data channel 2 and writing any data byte or data word into the basic register.

7.1.6.3 Format bit D03

The format bit is only effective with units with error detection and error correction.

D03 = 0: Formatting
D03 = 1: Saving

When using the memory card for the first time or if there is a voltage loss for the buffer battery, the unit must be formatted. The saving sign is created here and saved.

Each page of a unit must be formatted.

The "formatting" mode is set via the data channel D00.

D03 must be 0 in the data byte or data word to be written, and D04 ... D07 must include the address of the page to be formatted.

Example for the data word (as an example xx00H) for page 1:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	0	0	0	0	0	d	d	d

d = insignificant

Formatting the selected page is carried out by reading the memory area assigned to the units or writing it with any value (see point 7.1.5.1).

The operating mode saving must be selected again after the formatting and the error bit reset. The error detection is now functioning. Every memory address has the value 0 after the formatting has taken place.

7.1.6.4 Example for the setting and addressing

1. Four 35 PS 91 cards with error detection and error correction are operated using the MPST bus.

2. The memory card address is set on every card with the switches S2.1 ... S2.3.

Unit	Switch S2 1	2	3	4	Address area
1	on	on	on	d	0000H ... 1FFFH
2	on	on	off	d	2000H ... 3FFFH
3	on	off	on	d	4000H ... 5FFFH
4	on	off	off	d	6000H ... 7FFFH

d = insignificant

3. A data channel address is assigned to every unit to address the basic register.
   The status of A12 is determined with the plug X7; the address bits A04 ... A11 is determined with switch S1.

   If the jumper X7: 1 – 3 is plugged in, A12 = 1.

Unit	Switch S1 1	2	3	4	5	6	7	8	HEX address (Data channel 0)
1	on	on	on	on	on	on	on	on	F000H
2	on	on	on	on	on	on	on	off	F010H
3	on	on	on	on	on	on	off	on	F020H
4	on	on	off	on	off	on	off	on	F2A0H

   The addresses of the error registers (data channel 2) are then:

   Unit 1 F002H
   Unit 2 F012H
   Unit 3 F022H
   Unit 4 F2A2H

4. Formatting the example of unit 4
   The data word 0000H is first written on to the address F2A0H in order to format page 1.

   Page address: Format bit:
   D04 D05 D06 D07 D03 = 0
   0 0 0 0

   The bits D08 ... D15 are not evaluated. The memory area 6000H ... 7FFFH, which is assigned to unit 4, must then be evaluated.

   The procedure is the same to format other pages (change the page addresses accordingly!).

5. Resetting the memory mode with error correction is carried out after formatting page 16 by writing the data word 0008H to the address F2A0H.

   Page address: Format bit:
   D04 D05 D06 D07 D03 = 1
   0 0 0 0

   The first page, which is already formatted, is therefore selected again.

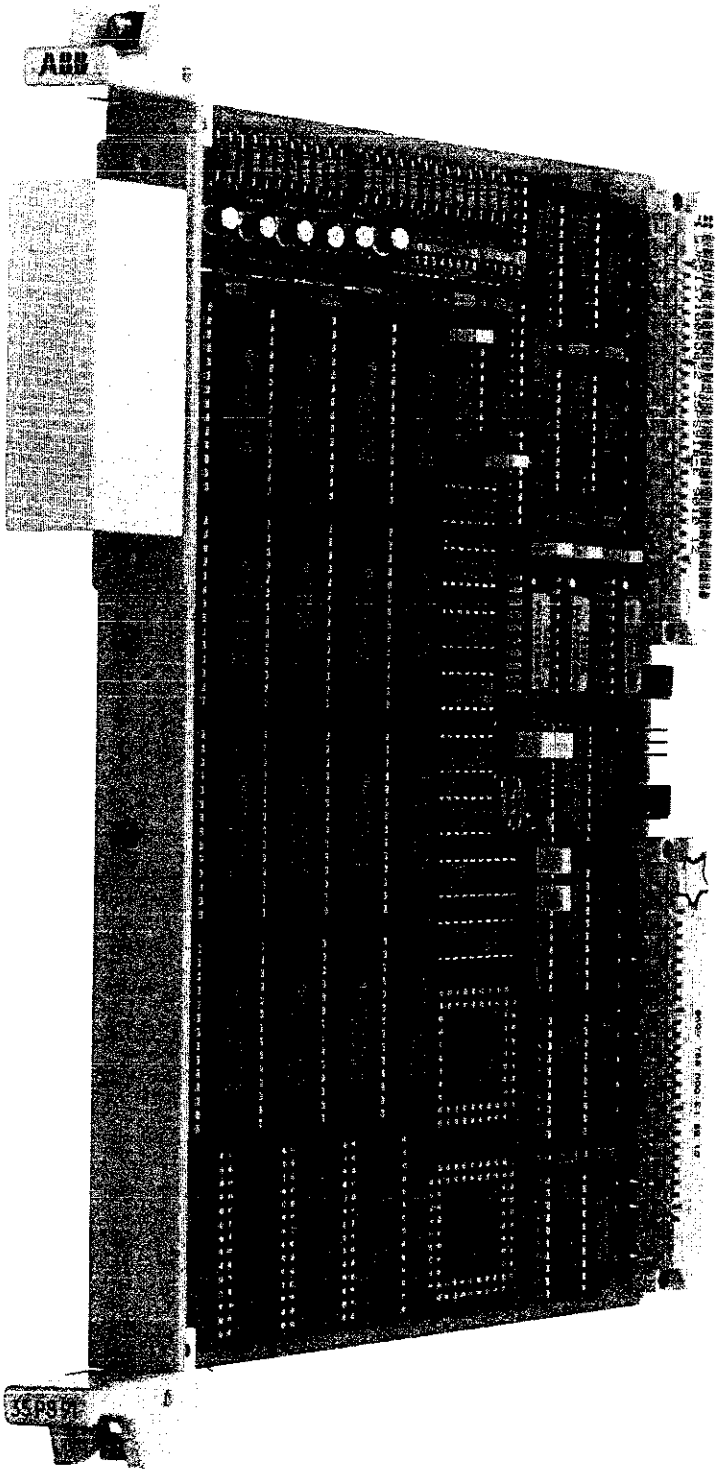
6. Address F2A2H is to be written with the data word 0000H to reset the error register (D01 = 0).

7.1.7 Settings

Plug	Factory settings without error detection and error correction	with error detection and error correction	User settings
X1	T300 bus		
X2	T300 bus		
X3	8-9, 7-10 6-11,5-12	1-8, 2-7 3-6, 4-5	
X4	open	open	
X5	open	open	
X6	2-3	1-2	
X7	2-3	2-3	1-2: A12 = 0 * 2-3: A12 = 1 **
X8	1-2	1-2	
X9	1-2	1-2	1-2: occupied bit D00 = 1 2-3: occupied bit D00 by the bus
X10	+ battery pole		
X11	– battery pole		
X12	1-2	1-2	
X13	1-2	1-2	
X14	offen	1-2	
X15	1-2	1-2	

* Basic register address : ExxxH
** Basic register address : FxxxH

7.2 Memory card 35 PS 91 R22



90 01 82

7.2.1 Technical data

Memory capacity	max. 512 kbytes
U_{S1} positive supply voltage	+ 5 V ± 5 %
U_{SR} buffer voltage (lithium battery)	+ 2.9 V < U_{SR} < + 3.7 V
	without error detection
I_{B1} for U_{B1}	typically 1.1 A, max. 1.5 A
I_{SR} for U_{SR}	typically 30 µA, max. 85 µA
Power loss	7.5 W ± 20 %
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Writing or reading cycle from $\overline{BOV}$=0 to RDY=1	200 ns < T < 300 ns
Input values	according to DIN 66 264
Output values	according to DIN 66 264
Dimension	1 pitch
Weight	1.0 kg
Order number:	
35 PS 91 R22, without error detection, 512 kbytes assembly	GJR5137100R22

Accessories:

Lithium battery 07 LB 20 R1	GJR5223500R1
Lithium battery unit 35 LE 90 R1	GJR5146300R1

7.2.2 Description

The battery-buffered CMOS memory card 35 PS 91 is a passive subscriber on the MPST bus.

7.2.2.1 Application

The unit serves as a data memory for

- CNC part programs
- RAM disk for the industrial computer
- MDS machine data sentences, etc.

7.2.2.2 Features

- Memory size 512 kbytes.
- 64 Pages can be addressed for every 8 kbytes.
- The memory card can be read in bytes or words.
- 1 ... 7 units can be operated at the same time.

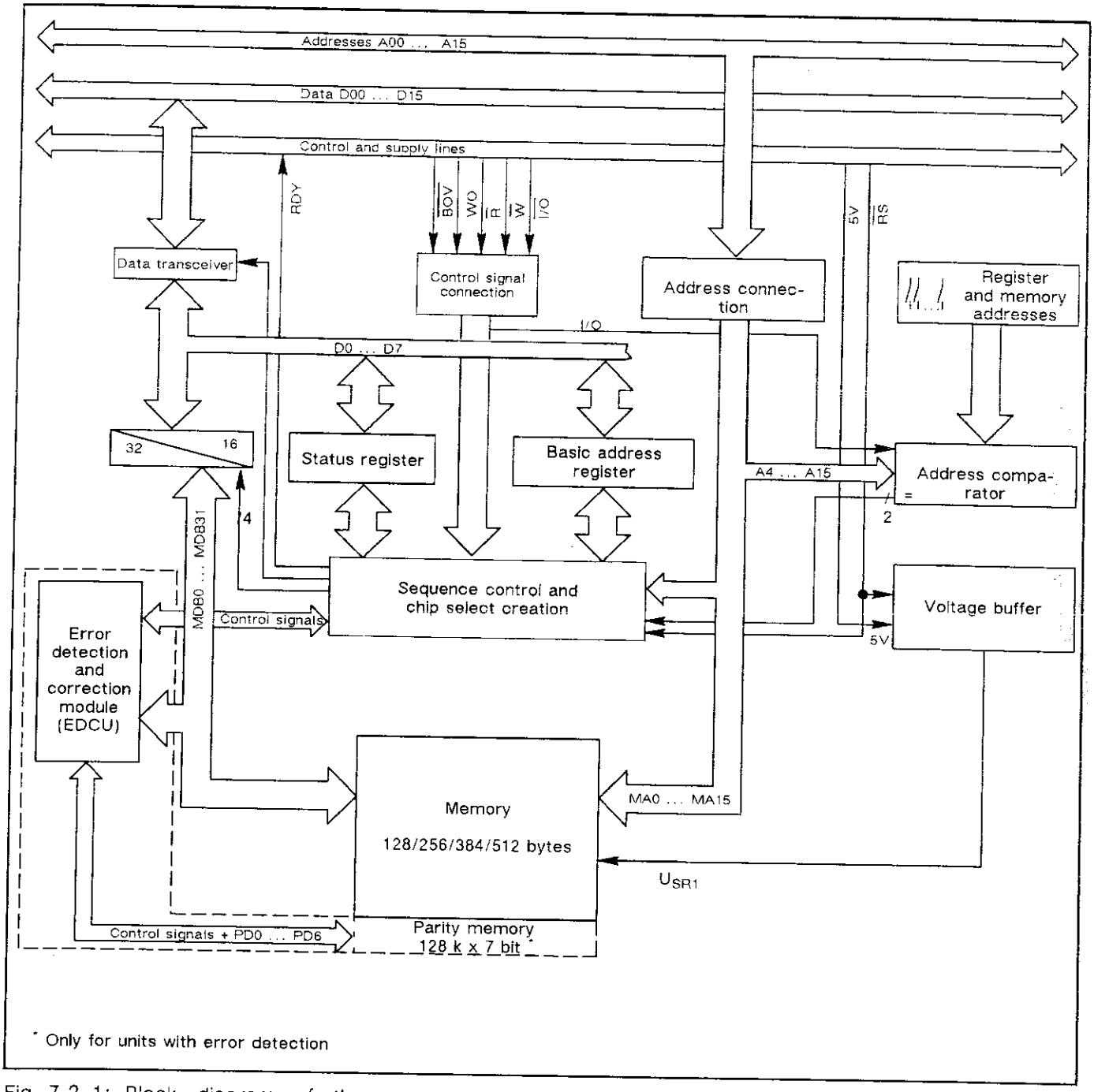


Fig. 7.2-1: Block diagram of the memory card 35 PS 91

7.2.2.3 Addresses

56 kbytes address capacity is available for the data memory on the MPST bus. A maximum of 7 units can be accommodated in this area. Each unit then has a window of 8 kbytes. 64 pages for every 8 kbytes can be applied to this window by an internal switchover on the card, which can be addressed. The maximum memory extension with 7 units amounts to 7 x 16 x 8 kbytes = 7 x 512 kbytes = **3584 kbytes**.

7.2.2.4 Basic register

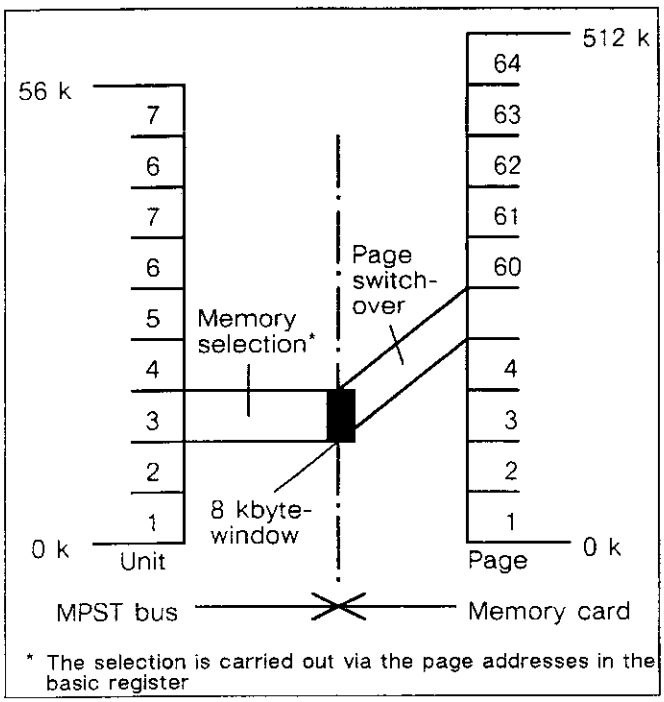
Every memory card has a basic register, which can be addressed like an I/O unit in the area of 56 ... 64 kbytes.

The 16 bit basic register gives information concerning:

- Page addresses: Bit D09 ... D04
- Operating modes:
  - * Format bit Bit D03
  - * Error bit Bit D01
  - * Occupied bit Bit D00

Bit D02 is not used.

Internal switchover, which can be addressed:



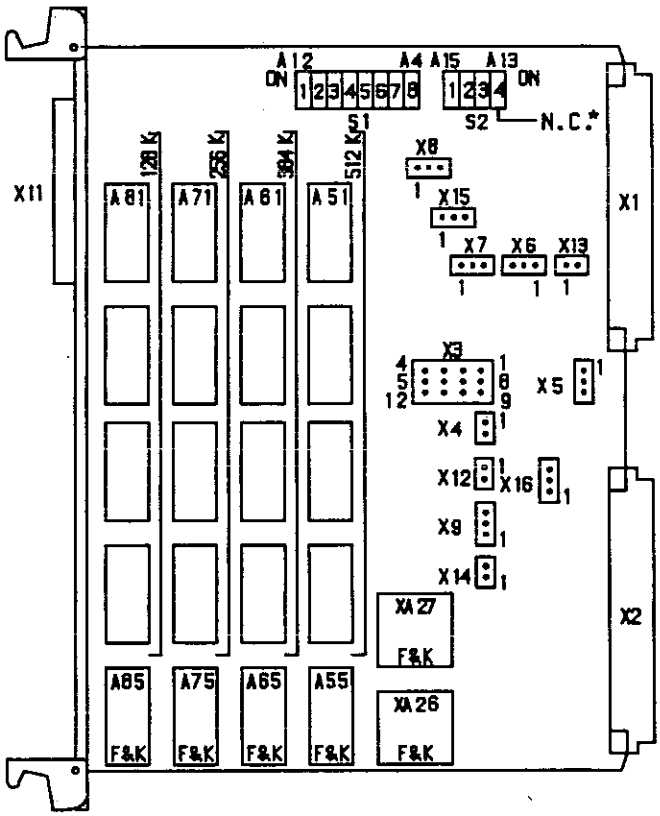
* The selection is carried out via the page addresses in the basic register

7.2.2.5 Battery

The battery for buffering the RAM slots are attached on the front panel of the unit. Changing the lithium battery or the lithium battery module is therefore possible without disconnecting the module (see also chapter 21.4 and 21.5).

7.2.3 Mechanical structure

Double-size plug-in printed-board assembly 4 R, 6 U x 160 mm.



* N.C. = Not Connected

F & K is only assembled for units, which are equipped with error detection and error correction.

Fig. 7.2-2: Component side (top view)

7.2.4 MPST bus interfaces, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transmission	X1.24c	–	–
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	–	–	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

7.2.5 Addressing the memory

Addressing the memory includes 3 stages

- Memory selection via the MPST bus (A15 ... A13) 1 of 7
- Page selection via the basic register (D07 ... D04) 1 of 64
- Addressing the memory via the MPST bus (A12 ... A00) 0 ... 8 kbytes

7.2.5.1 Memory selection

Distinguishing between 1 ... 7 units is carried out in the address area 0 ... 56 kbytes, which is foreseen for addressing the memory in accordance with the MPST bus determination. The memory card address is set with the switch S2.

Note:
The switch position ON logically corresponds to 0.

The switches S2.1 ... S2.3 are compared with the bits A15 ... A13 on the MPST bus.

Unit	Window	Switch 1	2	3	4	Address area
1	0 ... 8 kbytes	0	0	0	d	0000H...1FFFH
2	8 ... 16 kbytes	0	0	1	d	2000H...3FFFH
3	16 ... 24 kbytes	0	1	0	d	4000H...5FFFH
4	24 ... 32 kbytes	0	1	1	d	6000H...7FFFH
5	32 ... 40 kbytes	1	0	0	d	8000H...9FFFH
6	40 ... 48 kbytes	1	0	1	d	A000H...BFFFH
7	48 ... 56 kbytes	1	1	0	d	C000H...DFFFH
–	prohibited*	1	1	1	d	–

d = Switch position is insignificant
* reserved for the ABB Procontic T300 data channel area

7.2.5.2 Data channel address

The data channels, with which the basic register can be read or written, are between 57 and 64 kbytes in the upper address area in accordance with the MPST bus determination.

Each unit has a data channel address assigned to it via switch S1. The separate data channels are addressed by the MPST bus via A00 ... A03.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	Y	Y	Y	Y	Y	Y	Y	Y	Z	Z	Z	Z
ABB Procontic T300 code for the upper address area				1	2	3	4	5	6	7	8				
				Switch S1											

1 = permanently wired up
X = can be set with plug-in jumper X7
X7.2 - X7.2: A12 = 0
X7.2 - X7.3: A12 = 1 (Factory presetting)
Y = the data channel address of the card can be set with the switch S1.

Note:
The switch position ON logically corresponds to 0.
Z = Addressing the separate data channels. 3 channels are evaluated on the card:

The following operations are permitted in the separate channels:

	Channel address				Data in the basic register							
	A03	A02	A01	A00	D07	D06	D05	D04	D03	D02	D01	D00
Channel 0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Channel 2	0	0	1	0	R	R	R	R	R	R	R/W	R
Channel 4	0	1	0	0	R	R	R	R	R	R	R	R/W

R = Reading; W = Writing

7.2.5.3 Page selection

After addressing the memory card as an I/O unit (see point 7.2.5.2), the page address is loaded into the basic register via the data channel 00.

Basic register:

Page addresses1 ... 16				Operating modes (not important for the page selection)			
D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	without error detection d	d	d	d
	:			with error detection			
1	1	1	1	1	d	d	d

d = insignificant

7.2.5.4 Addressing the memory

The page, which is 8 kbytes large, is selected via the page address and addressed by the MPST bus with A12 ... A00 after the selection of the unit via A15 ... A13 (see point 7.2.5.1).

7.2.6 Operating modes

3 operating status are to be observed:

- Formatting — only important for units with error detection and error correction
- Error detected — only important for units with error detection and error correction
- Card occupied

7.2.6.1 Occupied bit D00

The occupied bit D00 can be activated with the jumper X9.

X9.1 – X9.2 The card is always active after the RESET (factory presetting).

X9.2 – X9.3 The card is switched on or off by the MPST bus via D00.
Address: Data channel 4

D00 = 0: The unit is not active
D00 = 1: The unit is active

7.2.6.2 Error bit D01

The error bit is only effective for units with error detection and error correction.

D01 = 0: No error
D01 = 1: Error

If D01 = 1, an error, which cannot be corrected, occurred with a previous memory access. This error is displayed, until it is acknowledged.

The acknowledgement is carried out by addressing the data channel 2 and writing any data byte or data word into the basic register.

7.2.6.3 Format bit D03

The format bit is only effective with units with error detection and error correction.

D03 = 0: Formatting
D03 = 1: Saving

When using the memory card for the first time or if there is a voltage loss for the buffer battery, the unit must be formatted. The saving sign is created here and saved.

Each page of a unit must be formatted.

The "formatting" mode is set via the data channel D00.

D03 must be 0 in the data byte or data word to be written, and D04 ... D07 must include the address of the page to be formatted.

Example for the data word (as an example xx00H) for page 1:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	0	0	0	0	0	d	d	d

d = insignificant

Formatting the selected page is carried out by reading the memory area assigned to the units or writing it with any value (see point 7.2.5.1).

The operating mode saving must be selected again after the formatting and the error bit reset. The error detection is now functioning. Every memory address has the value 0 after the formatting has taken place.

7.2.6.4 Example for the setting and addressing

1. For 35 PS 91 cards with error detection and error correction are operated using the MPST bus.

2. The memory card address is set on every card with the switches S2.1 ... S2.3.

Unit	Switch S2 1	2	3	4	Address area
1	on	on	on	d	0000H ... 1FFFH
2	on	on	off	d	2000H ... 3FFFH
3	on	off	on	d	4000H ... 5FFFH
4	on	off	off	d	6000H ... 7FFFH

d = insignificant

3. A data channel address is assigned to every unit to address the basic register.
   The status of A12 is determined with the plug X7; the address bits A04 ... A11 is determined with switch S1.

   If the jumper X7: 2 - 3 is plugged in, A12 = 1.

Unit	Switch S1 1	2	3	4	5	6	7	8	HEX address (Data channel 0)
1	on	on	on	on	on	on	on	on	F000H
2	on	on	on	on	on	on	on	off	F010H
3	**on**	**on**	**on**	**on**	**on**	**on**	**off**	**on**	**F020H**
4	**on**	**on**	**off**	**on**	**off**	**on**	**off**	**on**	**F2A0H**

   The addresses of the error registers (data channel 2) are then:

Unit 1	F002H
Unit 2	F012H
Unit 3	F022H
Unit 4	F2A2H

4. Formatting the example of unit 4
   The data word 0000H is first written on to the address F2A0H in order to format page 1.

Page address:				Format bit:
D04	D05	D06	D07	D03 = 0
0	0	0	0	

   The bits D08 ... D15 are not evaluated. The memory area 6000H ... 7FFFH, which is assigned to unit 4, must then be evaluated.

   The procedure is the same to format other pages (change the page addresses accordingly!).

5. Resetting the memory mode with error correction is carried out after formatting page 16 by writing the data word 0008H to the address F2A0H.

Page address:				Format bit:
D04	D05	D06	D07	D03 = 1
0	0	0	0	

   The first page, which is already formatted, is therefore selected again.

6. Address F2A2H is to be written with the data word 0000H to reset the error register (D01 = 0).

7.2.7 Settings

Plug	Factory settings without error detection and error correction	with error detection and error correction	User settings
X1	T300 bus		
X2	T300 bus		
X3	8-9, 7-10 6-11,5-12	1-8, 2-7 3-6, 4-5	
X4	open	open	
X5	open	open	
X6	2-3	1-2	
X7	2-3	2-3	1-2: A12 = 0 * 2-3: A12 = 1 **
X8	1-2	1-2	
X9	1-2	1-2	1-2: occupied bit D00 = 1 2-3: occupied bit D00 by the bus
X10	+ battery pole		
X11	- battery pole		
X12	1-2	1-2	
X13	1-2	1-2	
X14	offen	1-2	
X15	1-2	1-2	

* Basic register address : ExxxH
** Basic register address : FxxxH

8 PLC central units

35 ZE 93 R301: PLC central unit consisting of the processor card 35 ZP 93 R31, data interface 35 DS 91 R1 and the software package for the function block PLC 935 83 R401.

35 ZE 94 R101: PLC central unit *in preparation*.

8.1 Central unit, 35 ZE 93 R301 ..... 8.1- 1

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8.1.4.1 Front panel 8.1- 3

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8.1.4.3 Data interface 35 DS 91 R1 .. 8.1- 4

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8.1.4.4.1 Bus clock jumper X6 ..... 8.1- 5

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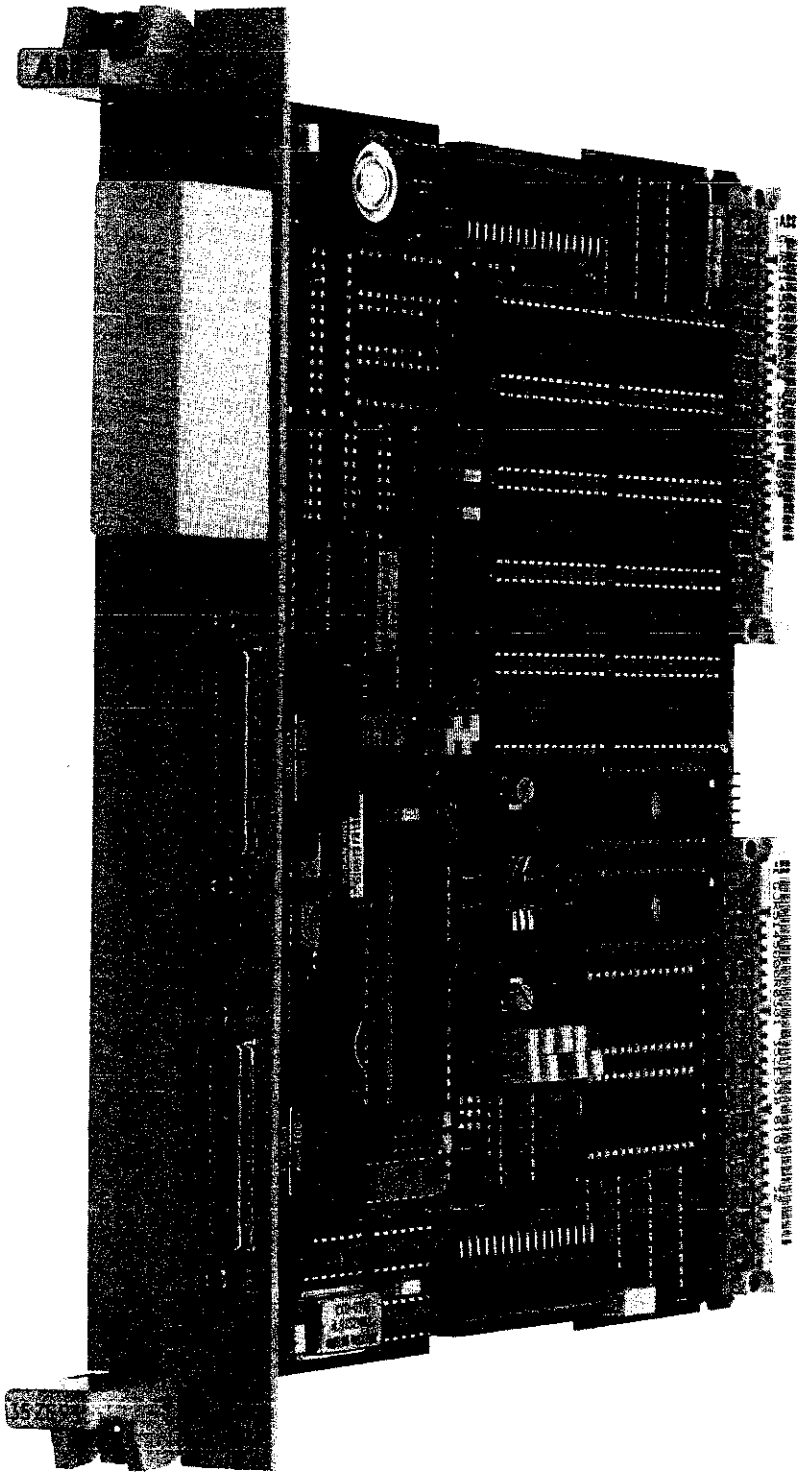
8.1.5 Extension by two serial interfaces using 35 DS 91 R1 ... 8.1- 6

8.2 Central unit, 35 ZE 94 R101
In progress **8.2- 1**

8.1 Central unit 35 ZE 93 R301



90 01 77

8.1.1 Technical data

Central unit PLC 35 ZE 93 R101	with 14 K instruction user program, bit and word processing, blocks and buffered flag range
Central unit:	
Processor	8086
Supply voltage	5 V ± 5 %
Current input	2.8 A ± 20 %
Power loss	15 W ± 30 %
Frequency clock	8 MHz
Interface unit:	
Number of interfaces	2
Interface 1	RS 232, RS 422 and 20 mA
Interface 2	RS 232, RS 422 and 20 mA
Memory extension	max. 256 KBytes
U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+15 V ± 5 %
U_{B3} negative supply voltage	−15 V ± 5 %
Power loss	2.5 W ± 20 %
I_{B1} for U_{B1}	typically 0.4 A, max. 0.65 A
I_{B2} for U_{B2}	typically 0.08 A, max. 0.15 A
I_{B3} for U_{B3}	typically 0.08 A, max. 0.15 A
Ambient temperature	0 °C ... + 55 °C
Storage temperature	− 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	2 pitches
Weight	2.2 kg
Order number	GJR5145000R301

Accessories:

Spare battery 07 LB 20 R1	GJR5223500R1
Battery module 35 LE 90 R1	GJR5146300R1
Comment additional assignment 35 PK 83 (upon request, not in the delivery scope of the central unit)	GJR5144800R1

8.1.2 Description

The central unit 35 ZE 93 is a PLC tested in factory. Its hardware consists of the following two components

- 35 ZP 93 R31
- 35 DS 91 R1

and the software function block

- 935 PC 83 R401

If the comment additional consignment 35 PK 83 R1 is required, this must be ordered separately by the user and installed for the unit 35 DS 91 R1 by means of the supplied installation instructions.

8.1.3 Supply condition and operating instructions

The **baud rates** of the user interface (plug X3) and the interface 1 (plug X4) is set to 9600 baud. The serial interface must also be set to 9600 baud for the ABB Procontic programming and test unit or the VT100 compatible terminal. (see chapter 6, Data interfaces)

The **subscriber address** for the MPST bus is set to "01H" on the jumper field X9 (see chapter 8.7)

- Test whether another central unit already has the set subscriber address. If this is the case, another subscriber address, which is not occupied, must be set on thejumper field X9 with the corresponding jumpers.

The **MPST bus clock** may only be output to the MPST bus by **one** central unit.

- Every central unit must be supplied exactly **once** by the MPST bus clock. The bus clock CC is switched on with the jumper X6. The bus clocks may not be output to the MPST bus via the jumper X6 with two or more units.
- The position of the plug-in jumpers is to be altered according to the following tables before the assembly is changed, e.g., configuration with the comment RAM memory.
- Always save your programs if you must remove the unit from the subrack in order to carry out changes to the setting on the 35 ZE 93 for example.
- Observing the electrical and mechanical installation guidelines in leaf 5 of the configuration folder is the prerequisite for using the 35 ZE 93.
- The interface plugs should not be disconnected when the voltage is on, if possible.

8.1.3.1 Initialisation by a cold start

A **cold start** is to be carried out in any case:

- before the first use of the 35 ZE 93
- after the 35 ZE 93 was plugged into the subrack, e.g., after changing the program memory
- after memory blocks on the 35 DS 91 were touched

8.1.4 Mechanical structure

8.1.4.1 Front panel

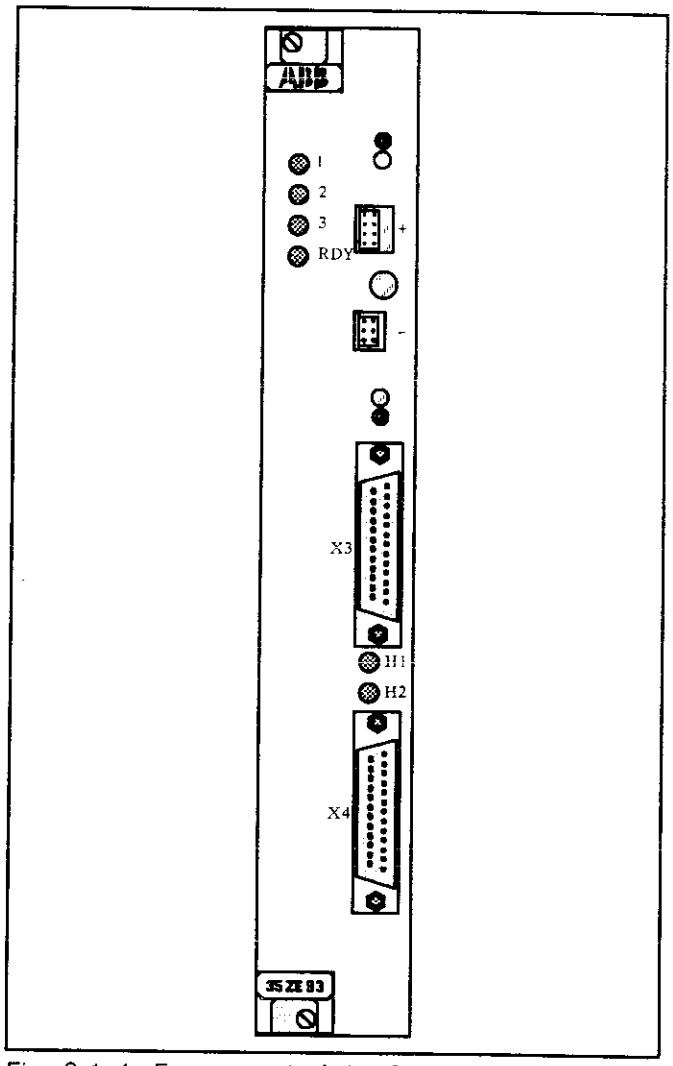


Fig. 8.1-1: Front panel of the 35 ZE 93 R301

8.1.4.1.1 Using the lithium battery module 35 LE 90 R1 for the first time

The supplied lithium battery module 35 LE 90 is not installed in the delivery status. This is to avoid loading the lithium battery before starting the device.

- The unit is to be installed in an ABB Procontic T300 subrack without plugging in the battery module. Switch on the voltage supply for the subrack. The capacitor located on the unit is loaded after approximally 5 to 10 minutes. The 35 LE 90 is to be mounted with the enclosed screws.
- Carry out the **cold start** so that a defined operating status is created. (see volume 8.2, chapter 17, Starting behaviour).

8.1.4.1.2 Battery change

The lithium battery or the lithium battery module can be replaced with the supply voltage to the subrack switched on.

8.1.4.1.3 Function of the LEDs on the front panel

The light-emitting diodes 1, 2, 3, RDY, H1 and H2 are located on the front panel of the central unit 35 ZE 93.

LED functions:

1 Displays that the PLC programs are running.
The LED 1 is switched on at the start of every program cycle and switched off again at the end of the program cycle. The length of time the LED 1 is switched on per program cycle is therefore only for short PLC programs.

2 POWER FAIL
The LED 2 displays that the signal POWER FAIL has been addressed. LED 3 is also switched on here.

3 Error display
The LED 3 displays on principle that an error has occurred.

RDY: READY
The LED RDY is directly connected to the READY pin of the processor. This LED must light up on principle, after the voltage has been switched on.

Consecutive light LED 1 ... LED 3:
If the PLC determines defective memories with a cold start, the PLC initialization is aborted, and the error is signalized by a consecutive light using the LEDs 1 ... 3.

H1 not used
H2 not used

Jumper	Pins	Meaning
X3	1-8 2-30 6-13-33 4-7-34 3-15 5-24	All settings with a sub printed board GJP5122910R1
X4	1-2	Transfer memory RAM 32K*8
X5	1-5-12-18 2-6-10-16 3-7-11-17 4-8-14 9-15	All settings with a sub printed board GJP5122920R1
X6	1-2	Jumper; bus clock No jumper; no bus clock X6 may only be plugged in for one unit, if there are several 35 ZE 93.
X7	1-2	Min. memory access time
X8	1-2	Transfer memory RAM 32K*8
X9	4-5,3-6,2-7	Subscriber address 01H Subscriber address adjustable from 1 ... 15

Table 8.1-3: Plug-in jumpers in the delivery status for 35 ZP 93

8.1.4.2 Processor card 35 ZP 93 R31

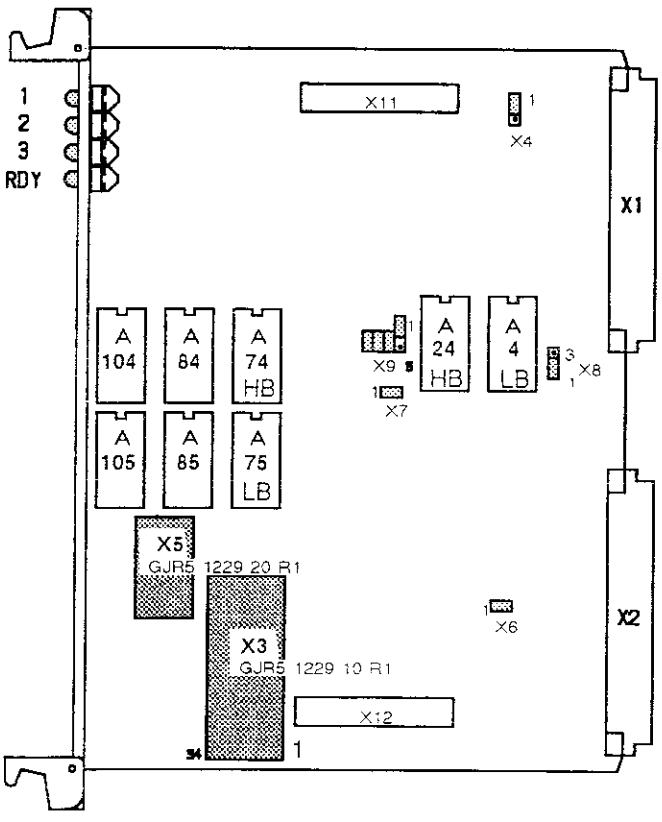


Fig. 8.1-2: Component side of the 35 ZP 93 (top view)

8.1.4.3 Data interface 35 DS 91 R1

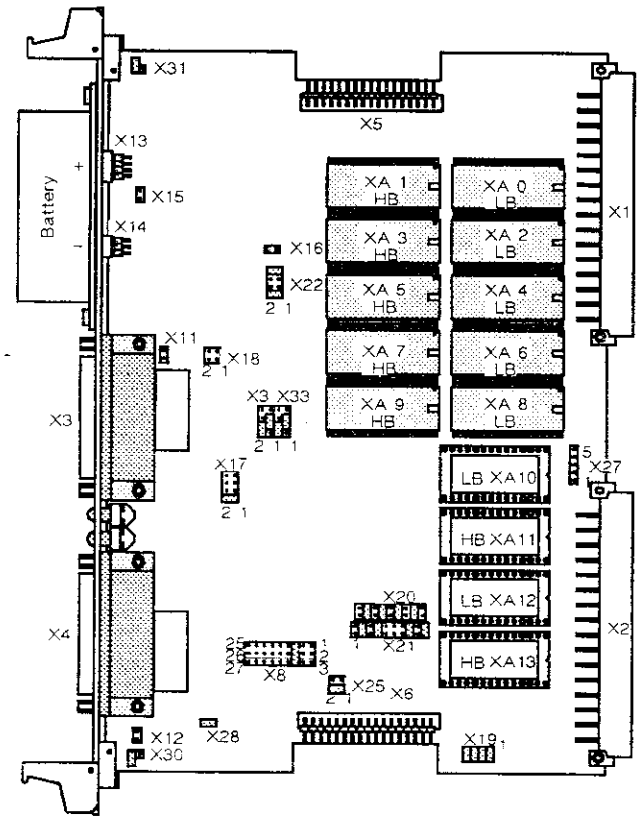


Fig. 8.1-4: Component side of the 35 DS 91 (top view)

Jumper	Pins	Meaning
X8	7–8–9	Baud rate channel A 9600 Baud (user interface) Baud rate channel B 9600 Baud (serial interface 1)
X11	Reserve plug-in jumper	special screen – 0 V connection, not required
X12	Reserve plug-in jumper	special screen – 0 V connection, not required
X15	no plug-in jumper	
X16	no plug-in jumper	
X17	1–2 5–6	35 ZE 93 clock switched on
X18	no plug-in jumper	Address setting for socket XA10–XA13
X19	1–2,3–4,5–6,7–8	Binary input for bit register
X20	3–4 7–8 11–12 15–16	XA10, XA11 memory EPROM 32 k x 8
X21	3–4 7–8 15–16 19–20	XA12, XA13 memory EPROM 64 k x 8 Comment EPROM
X22	1–2 7–8	RAM 62256 on XA6–XA9 with a battery buffer RAM 62256 on XA0–XA5 without a battery buffer
X24	no plug-in jumper	Ground-chip connection select for battery-buffered RAM
X27	no plug-in jumper	Alternative battery voltage to 35 LB 90 from the MPST bus
X28	1–2	Oscillator for channel A/B only for producer test purposes
X32	no plug-in jumper	
X33	no plug-in jumper	

Table 8.1-5: Plug-in jumpers in the delivery status on the interface card

8.1.4.4 Bus clock setting, subscriber address

8.1.4.4.1 Bus clock jumper X6

o—o PLC master, CCU or autonomous PLC.
1 2 The bus clock is switched on. Only plug in to **one central unit** in the ABB Procontic T300 system.

o—o PLC slave or PLC as an active subscriber
1—2 with the CCU, bus clock switched off

8.1.4.4.2 Subscriber address plug panel X9

The subscriber address from 0...15 can be set with a total of 4 jumpers on the plug panel X9 whereby "jumper plugged in" means logically 0 and "non-plugged in jumper" logically 1.

Adress	Jumpers in the plug panel X9 plugged in 4–5 2^3	3–6 2^2	2–7 2^1	1–8 2^0
0	o—o	o—o	o—o	o—o
1	o—o	o—o	o—o	o o
2	o—o	o—o	o o	o—o
3	o—o	o—o	o o	o o
4	o—o	o o	o—o	o—o
5	o—o	o o	o—o	o o
6	o—o	o o	o o	o—o
7	o—o	o o	o o	o o
8	o o	o—o	o—o	o—o
9	o o	o—o	o—o	o o
10	o o	o—o	o o	o—o
11	o o	o—o	o o	o o
12	o o	o o	o—o	o—o
13	o o	o o	o—o	o o
14	o o	o o	o o	o—o
15	o o	o o	o o	o o

8.1.4.5 Program memory with a comment RAM

The jumpers on the plug panels X20, X21, X32 and X33 are to be set as follows. All other plugs remain unaltered.

Jumper	Pins	Meaning
X18	3–4	XA10, XA11 RAM 32K*8 Address B0000..BFFFF
X20	1–2 5–6 9–10 17–18	XA10, XA11 Memory RAM 32 k x 8
X21	1–2 5–6 9–10 17–18	XA12, XA13 Memory RAM 32 k x 8
X32	1–2 5–6	XA12, XA13 RAM 32 k x 8 Address C0000..CFFFF XA10, XA11 RAM 32 k x 8 Address B0000..BFFFF
X33	1–2 5–6	XA12, XA13 RAM 32 k x 8 Address C0000..CFFFF XA10, XA11 RAM 32 k x 8 Address B0000..BFFFF

Table 8.1–6: Plug-in jumpers for operating with a comment RAM

8.1.5 Extension by two serial interfaces using 35 DS 91 R1

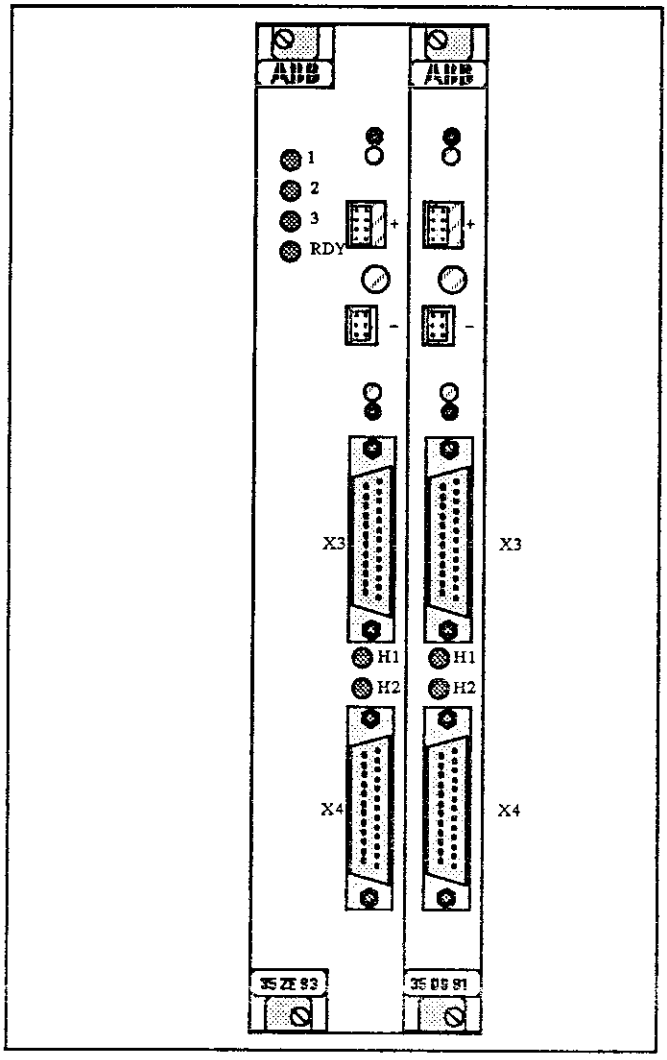


Fig. 8.1–7: 35 ZE 93 extended with 35 DS 91

The sub assembly 35 ZE 93 R301 can be extended by two serial interfaces. To this end, a sub assembly 35 DS 91 R1 is mounted to the 35 ZE 93 R301. The 35 DS 91 R1 has a separate front panel. The sub assemblies are mounted with the enclosed screws and connections.

Settings:

The connection for the jumper X17/3–4 must be plugged in on the second data interface 35 DS 91 R1.

- The connections for X17/5–6 and X17/1–2 are to be removed.

All other settings, e.g., baud rate, special shielding measures, etc., are to be taken from the description of the 35 DS 91 R1 (section 6.2).

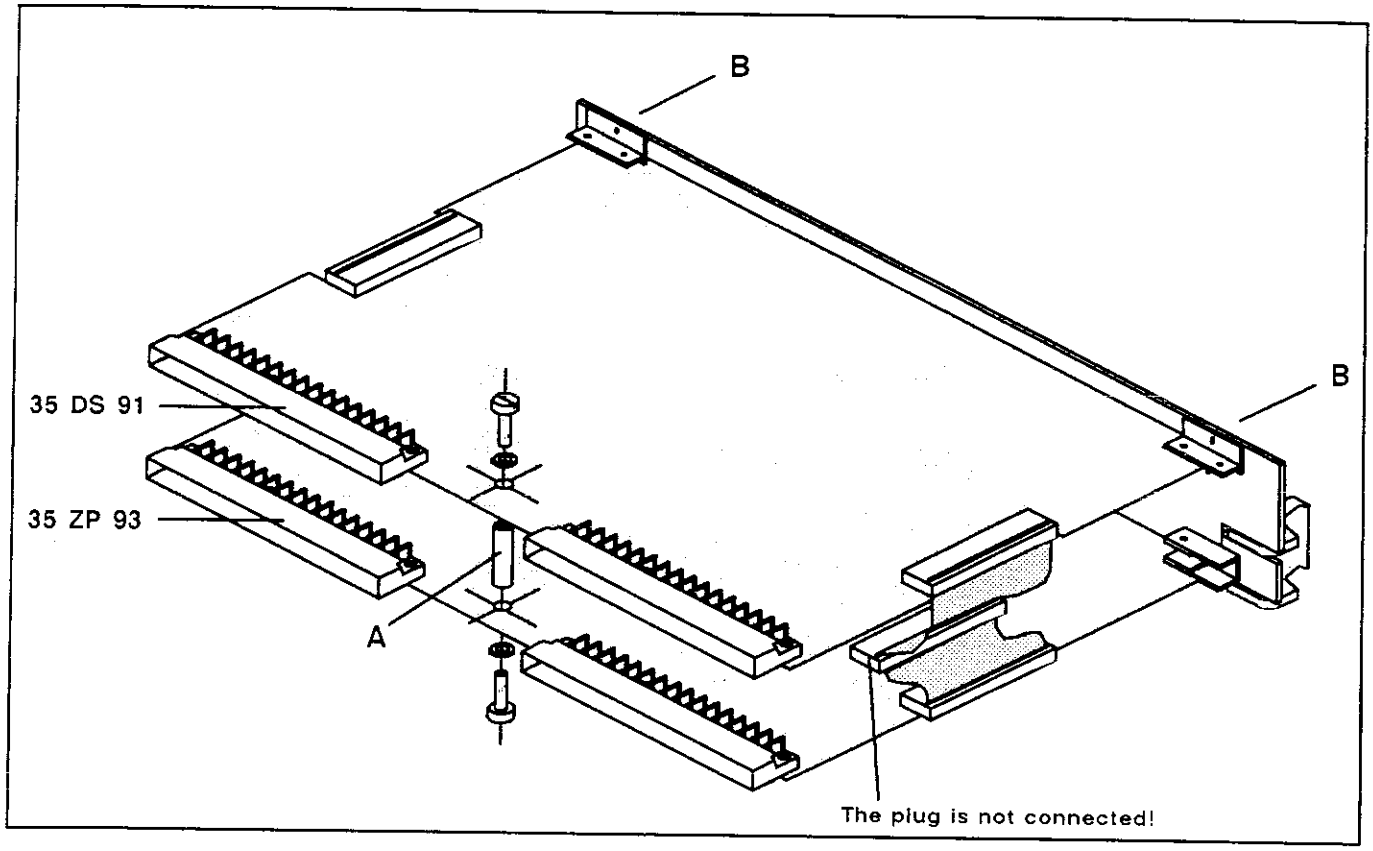


Bild 8.1-8: Dismantling the 35 ZE 93 from the printed boards 35 ZP 93 and 35 DS 91

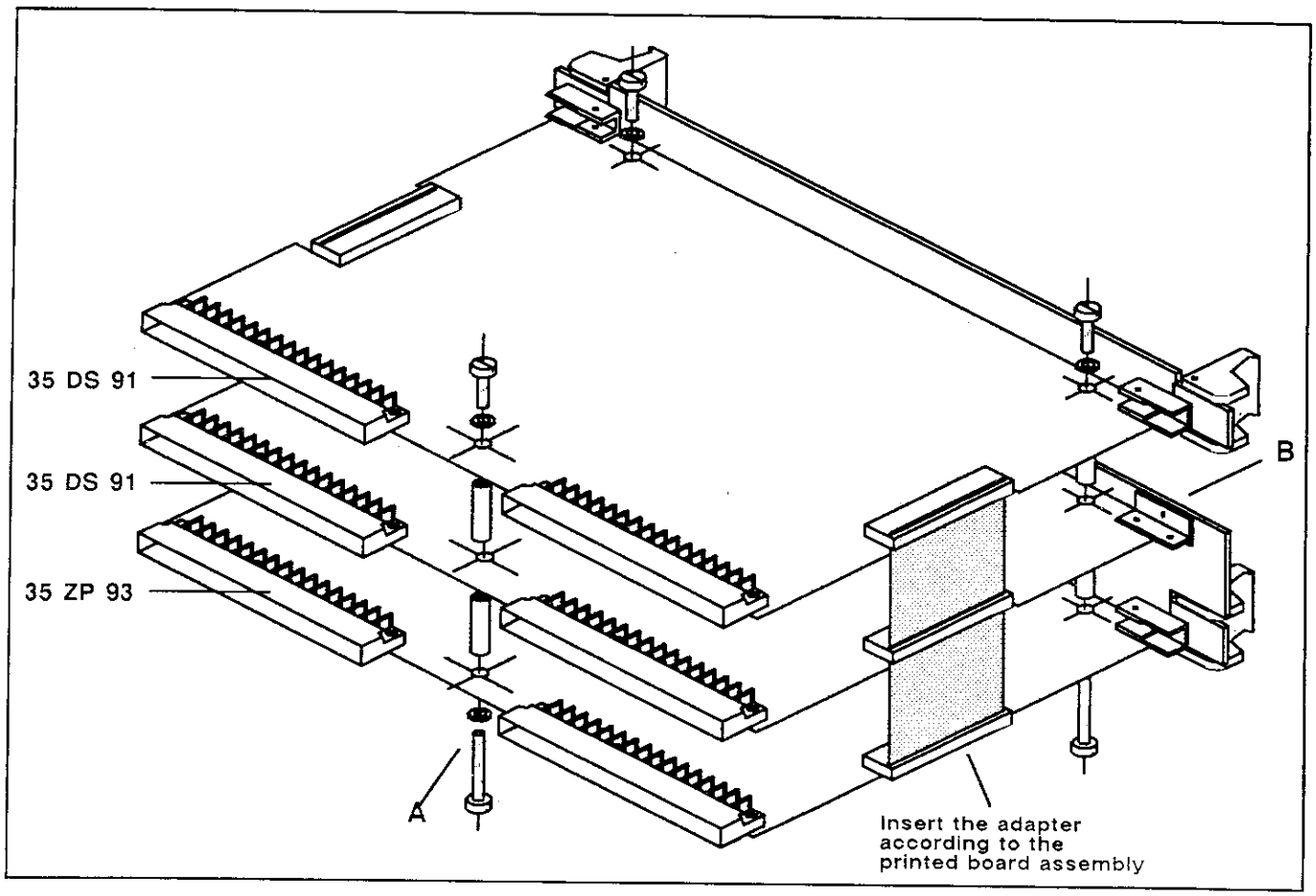


Fig. 8.1-9: Assembling the 35 ZE 93 with a second 35 DS 91

9 CNC units

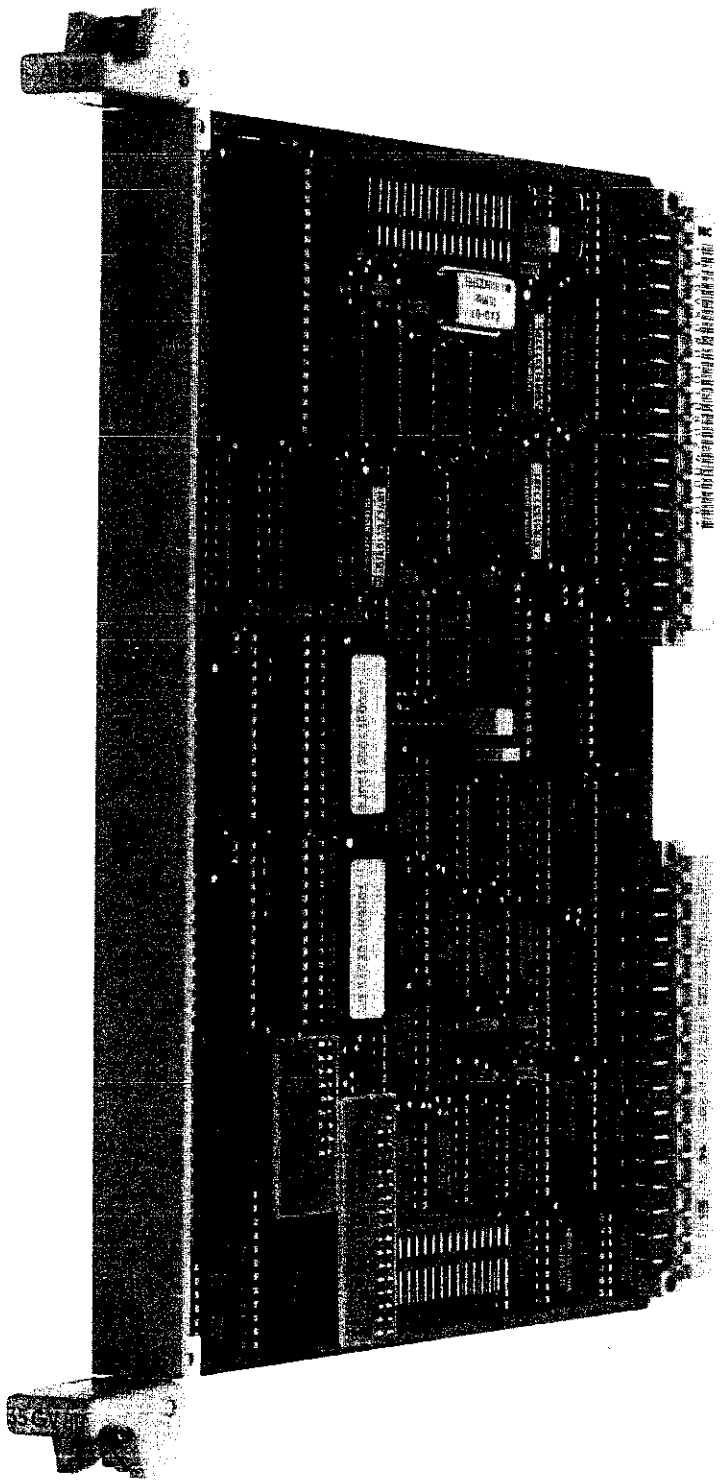
35 GV 80 R101: Positioning unit for 4 axes
35 GV 83 R101: Path control unit for 4 axes
35 ZS 86 R101: Central control unit to control 13 x 16 positioning axes and 13 x 4 path control axes

9.1 Positioning unit 35 GV 80 R101 ..... 9.1- 1
9.1.1 Technical data 9.1- 2
9.1.2 Description 9.1- 2

9.2 Path control unit 35 GV 83 R101 ..... 9.2- 1
9.2.1 Technical data 9.2- 2
9.2.2 Description 9.2- 2

9.3 Central control unit 35 ZS 86 R101 ..... 9.3- 1
9.3.1 Technical data 9.3- 2
9.3.2 Description 9.3- 2

9.1 Positioning unit 35 GV 80 R101



90 01 66

9.1.1 Technical data

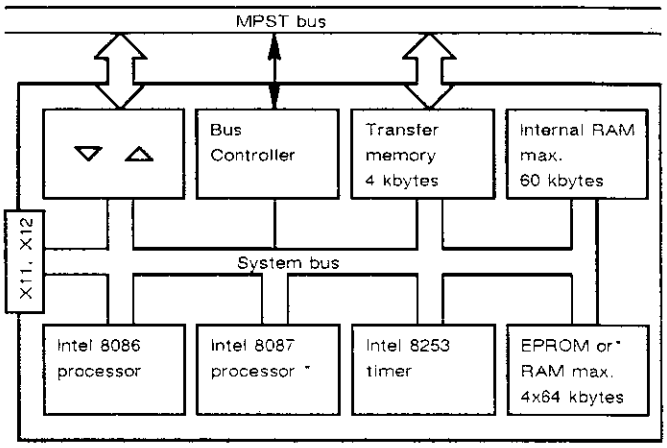
Central unit:	
Processor	8086
Coprocessor	8087
Supply voltage	5 V ± 5 %
Current input	2.8 A ± 20 %
Power loss	15 W ± 30 %
Frequency clock	5 MHz
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	1 pitch
Weight	1.2 kg
Order number	GJR5145300R101

9.1.2 Description

The positioning function block is written into the assembler of the micro processor Intel 8086. It has the following features:

- It can be configured via constant in the machine data sentence (MDS)
- A maximum of 4 controlled axes, selection via the machine data constant
- The position control clock depends on the number of the controlled axes. A time requirement of 0.7 ms occurs per axis and a basic time requirement of 2.2 ms must be added.
- Following error monitoring for the maximum value, can be indicated via the machine data constant per axis
- The control window can be indicated via the machine data constants for each axis
- The hardware limit switches of the axes are evaluated
- A resolution of the path measuring system can be given via the machine data constant for each axis. Possible range: 1 µm/increment to 100 µm/increment
- Separating the position control for the individual axes is possible. The corresponding axes are no longer fixed in one position in this way but nominal and actual values are still updated if the axes move due to foreign forces
- A drift compensation is possible in all axes. A correction value in the range ±127 increments can be preset in the machine data sentence for every axis
- Representation of the axes currently being moved together with their direction of movement, e.g., for the control release
- It is possible to delete and set the nominal and actual values in the individual axes
- All movements are executed with an acceleration limit; the value can be set for each axis via the machine data constant
- Two programmable functions: positioning and reference point movement
- Programming the positioning and reference point movement via control blocks in accordance with ABB Procontic T300 software determinations
- Exchange of data via the standard data blocks in accordance with the ABB Procontic T300 software determinations
- The use of an operating system is not foreseen
- Software scope: roughly 9 kbytes

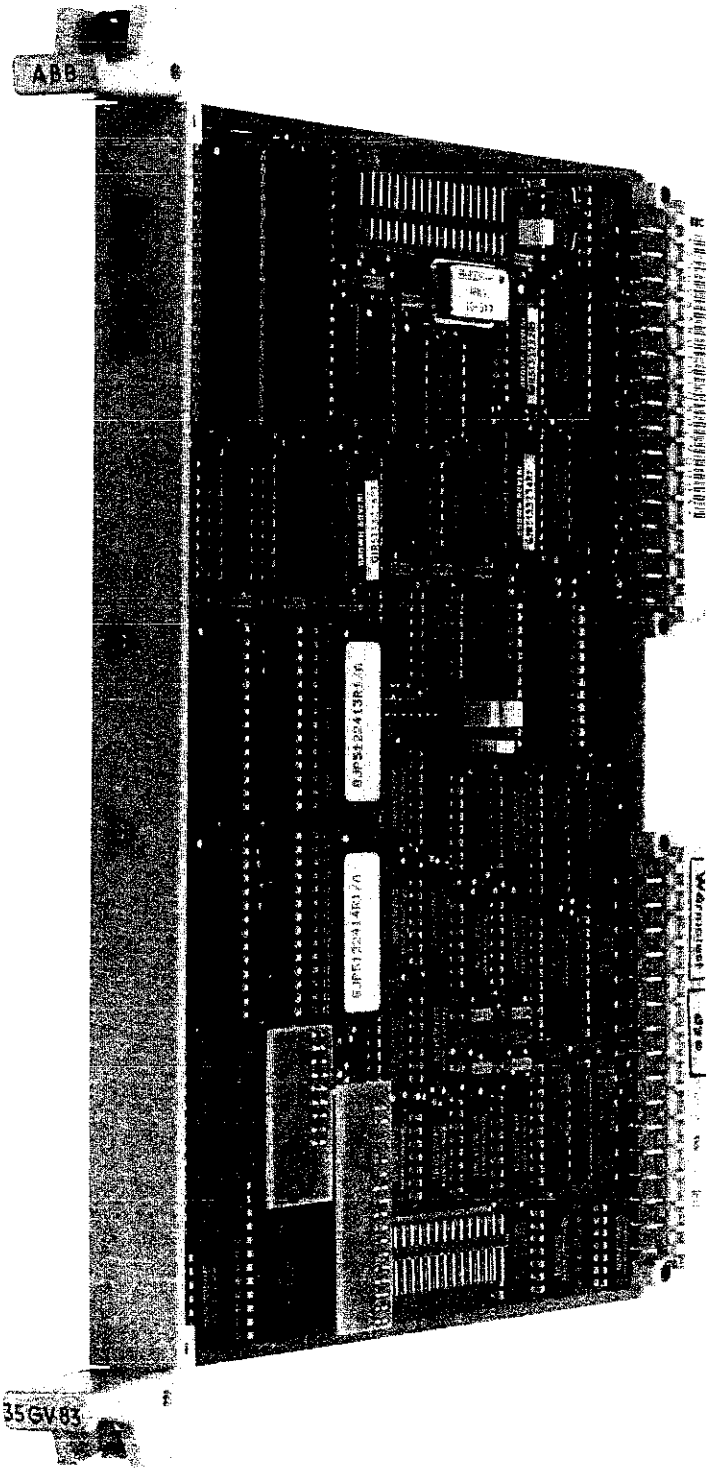
Note:
The positioning unit 35 GV 80 R101 is described exactly in the publication "POS-GEO Functional description, 935 GV 80 version: POS V7.4". This publication can be supplied upon request.



* Optional assembly

Fig. 9.1-1: Block diagram

9.2 Path control unit 35 GV 83 R101



90 01 65

9.2.1 Technische Daten

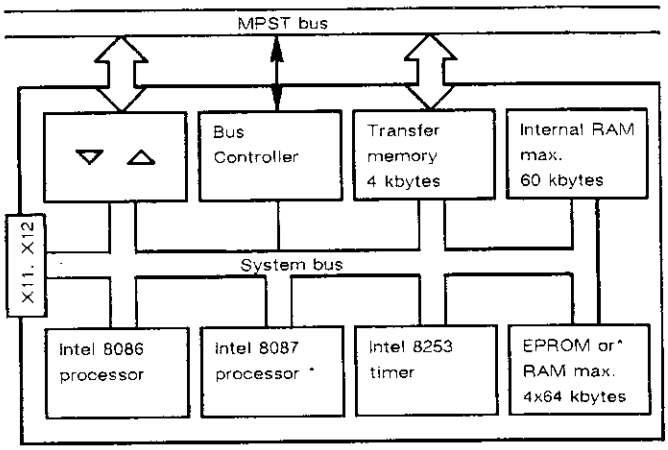
Central unit:	
Processor	8086
Coprocessor	8087
Supply voltage	5 V ± 5 %
Current input	2.8 A ± 20 %
Power loss	15 W ± 30 %
Frequency clock	5 MHz
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	1 pitch
Weight	1.2 kg
Order number	GJR5145400R101

9.2.2 Description

The path control function block is written into the assembler of the Intel 8086/8087 microprocessor. It has the following features:

- It can be configured via the constants in the machine data sentence (MDS)
- A maximum of 4 controlled axes, selection via the machine data constant
- Acceleration limit for reference point movement and target point movement. The acceleration course can be set via 3 constants of the machine data sentence. The acceleration and deceleration ramps are symmetrical.
- The following error monitoring can be switched between a static and a dynamic supervision. This can be set separately for each axis via 3 parameters each in the machine data sentence.
- The position control clock amounts to 5 ms
- The software limit switches of the axes are evaluated
- It is possible to delete the position nominal and actual values
- 2 orderable functions: target point movement and reference point movement
- Ordering the target point movement and reference point movement via control blocks in accordance with ABB Procontic T300 software determination
- Exchange of data via the standard data blocks in accordance with ABB Procontic T300 software determination.

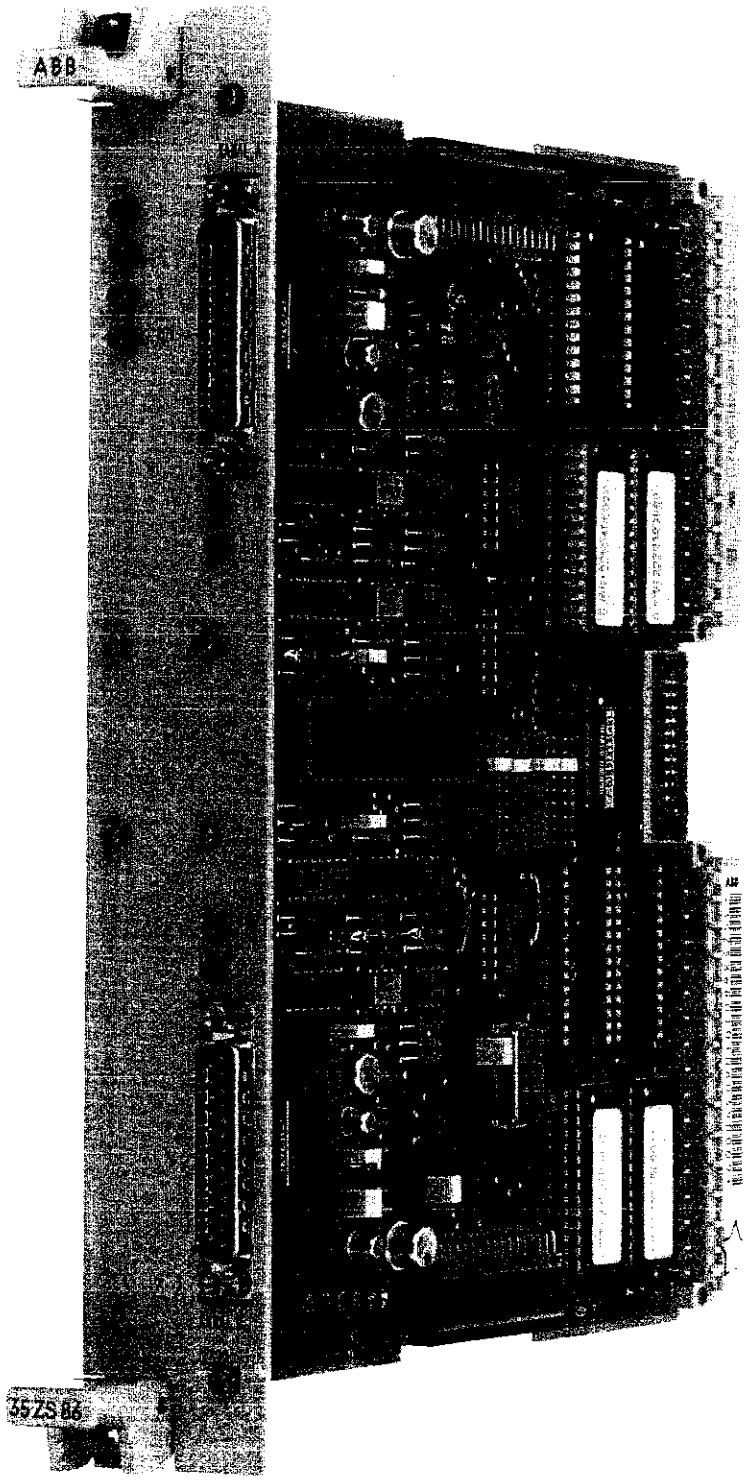
Note:
The path control unit 35 GV 83 R101 is described in detail in the publication "Path control function description 935 GV 83". This publication can be supplied upon request.



* Optional assembly

Bild 9.2-1: Block diagram

9.3 Central control unit 35 ZS 86 R101



90 01 91

9.3.1 Technical data

Central unit:	
Processor	8086
Coprocessor	8087
Supply voltage	5 V ± 5 %
Current input	2.8 A ± 20 %
Power loss	15 W ± 30 %
Frequency clock	5 MHz
Interface unit:	
Number of the interfaces	2
Interface 1	RS 232, RS 422 and 20 mA
Interface 2	RS 232, RS 422 and 20 mA
Memory extension	max. 256 kbytes
U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+15 V ± 5 %
U_{B3} negative supply voltage	-15 V ± 5 %
Power loss	2.5 W ± 20 %
I_{B1} for U_{B1}	typically 0.4 A, max. 0.65 A
I_{B2} for U_{B2}	typically 0.08 A, max. 0.15 A
I_{B3} for U_{B3}	typically 0.08 A, max. 0.15 A
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	2 pitches
Weight	1.2 kg
Order number	GJR5145500R101

9.3.2 Description

The central control unit 35 ZS 86 R101 is a universal unit with which it is possible to position and control the paths of several axes at the same time.
The software of the central control unit 35 ZS 86 R101 is designed for a maximum extension degree per system of 13 x 16 positioning axes, 13 x 4 path control axes or any combination of these two types.
The number of the axes to be held in their positions as well as all the machine-specific parameters (path resolution of the path measuring systems, acceleration and brake ramps, KV factors, etc.) can be configurated freely.
The intelligence of the system is divided into four separate units.

Central control (CCU):
- Treatment of the data for the geometry units and provision for the MPST bus
- Organisation and management of the system-internal sequences
- Dynamic management of the NC program memory
- Management of the buffered memory for the machine-specific parameters
- Simultaneous processing of sentences and programs for various geometry modules
- Communication with a superior master computer via a serial interface
- Initialisation and starting PLC programs

Geometry module for positioning (POS):
- 1 to 16 path-controlled axes
- max. drive speed of 65 m/min with1 µm resolutions
- modal axes
- reference point movement in 1 to 16 axes at the same time or consecutively in groups
- position control can be separated
- connection of different measuring systems via various axis cards
- recording releases, limit switches via binary input units
- absolute or relative programming
- programming selectively in mm, µm or increments
- drive path and speed (feed) programming for each axis
- G and M functions
- displaying all actual values
- single sentence mode
- programming mode

Geometry module for the path control (PATH):
- 2 to 4 path-controlled axes
- drive speed of 16 m/min with1 µm resolutions, max. 64 m/min with 4 µm path resolutions
- linear interpolation in 3 axes, 4th axis is towed
- circular interpolation in 2 axes, 3rd axis is towed
- level selection (x/y, y/z, z/x)
- connection of different measuring systems via various axis units
- recording releases, limit switches via binary input units
- absolute or relative programming
- programming selectively in mm, µm or increments
- path speed programming
- G and M functions
- displaying all actual values
- single sentence mode
- programming mode

Controlling the programmable memory (PLC):
- Time-controlled multi-program capacity
- integrated programming for the PLC
- access to several PLC processes via a serial interface
- connection to the master computer
- sub program technology (jumps)
- boolean instructions
- arithmetical instructions
- function blocks

Note:
The central control unit 35 ZS 86 R101 is described in detail in the publication "System descriptions CCU V8.0". This publication can be supplied upon request.

10 Axis units

35 PO 90 R101:	Single axis positioning unit,		with NC data memory,		1 serial interface,
	Input for incremental measuring systems,			± 10 V,	1 axis.
35 AE 92 R4:	Axis card,	2 axes.			
35 AE 92 R5:	Axis card,	4 axes.			
35 AE 92 R6:	Incremental input,	4-fold.			

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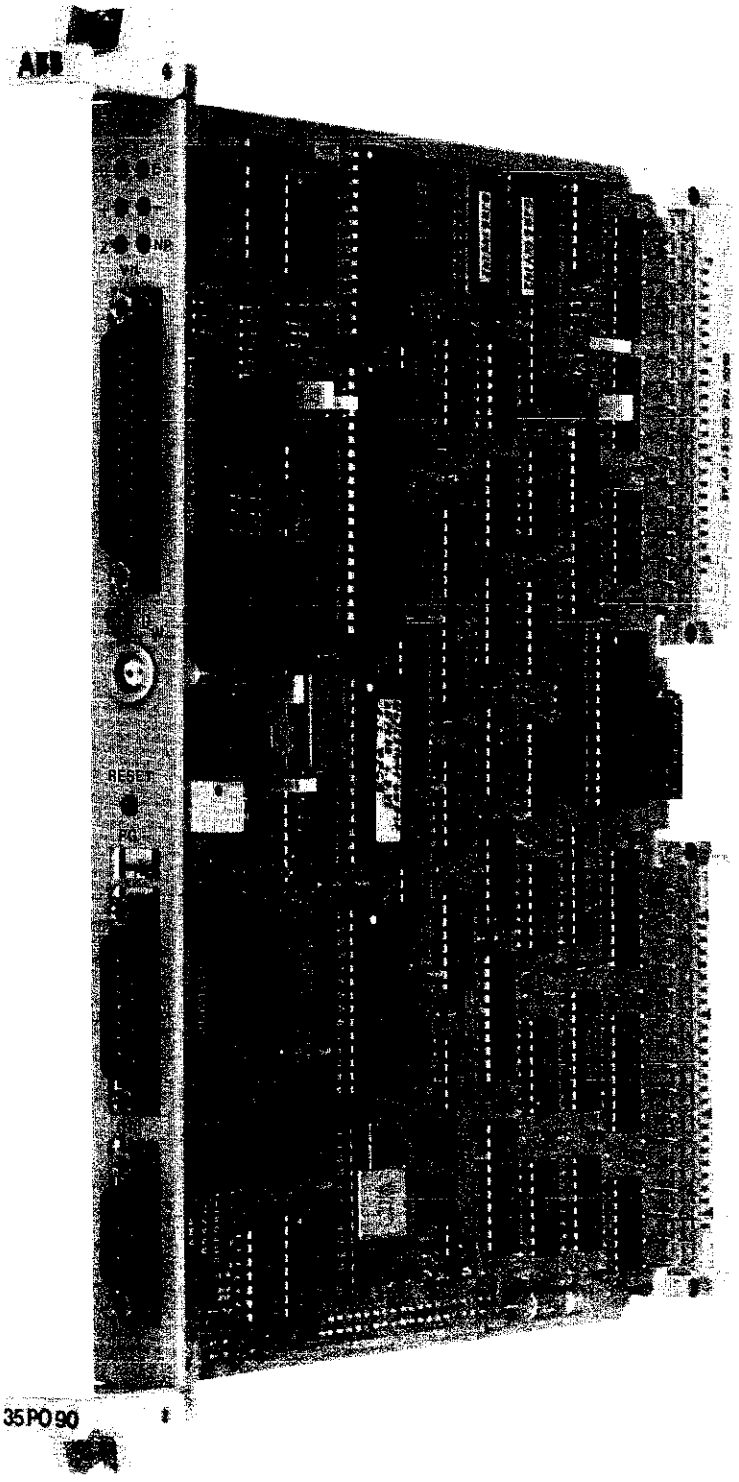
10.1 Single axis positioning unit 35 PO 90 R101



89 00 01

10.1.1 Technical data

U_{B1} pos. supply voltage	+ 5 V +5% / −3%
U_{B2} pos. supply voltage	+15 V +5% / −3%
U_{B3} neg. supply voltage	−15 V +5% / −3%
Up process voltage	+24 V ± 30% (including ripples)
I_{B1} for U_{B1}	typically 1.5 A, max. 2.4 A (without the supply for the incremental encoder)
I_{B2} for U_{B2}	max. 0.06 A (without the supply for the incremental encoder)
I_{B3} for U_{B3}	max. 0.06 A
Ip for Up	max. 0.05 A (without the supply for the operating units)
Total power loss	typ. 9 W, max. 13 W
Ambient temperature	0 °C ... +55 °C
Storage temperature	−25 °C ... +75 °C
Humidity rating	F
Mechanical stress	VDE 160 when installed
EMC category	See system data

Serial interface (V24)

RS422/ RS232C	can be switched over via jumper X1003
Transmission speed	2400 bauds
Transmission format	8 data bit, 1 stop bit, parity: even

Position encoder interface (PE)

Input switch with 26LS32	
Common-mode input voltage	max. ±25 V
Differencial - input voltage	max. ±25 V
Operating point	± 0.2 V
Line terminal U_{a1}, U_{a2}	RC element 120 Ω / 1 nF
U_{a0}	RC element 120 Ω / 680 pF
Min. flank clearance of the encoder signals U_{a1}/U_{a2}	2 µs
Max. encoder frequency	100 kHz

Set value interface (Uw)

Output voltage with "full scale"	±10 V
Arithmetical resolution	4.88 mV/bit
Max. Output current	±3 mA
Output inductivity of the bifilar reactor	typ. 140 µH
Effective inductivity	typ. 1.5 µH

Initiator interface (INI)

Max. input voltage	24 V ± 30%
Input voltage, 0 Signal	<= 5 V
Input voltage, 1 Signal	> 13 V
EingangsstromInput current	< 5 mA

MPST bus interface X1, X2

The in- and output values of the MPST bus plug X1 and X2 correspond to	DIN 66 264
Dimensions	1 pitch
Weight	1.1 kg
Order number	GJR5144100R101

10.1.2 Accessories for the 35 PO 90 single axis positioning unit

Operating and programming unit 35 AB 50	
Order number	GJR5139200R102
Elektronic switchover and control logic 35 US 50 b	
Order number	GJR5141800R101
Software for the personal computer 935 AM 50	
Order number	GJR5512000R202
Dialogue cable 35 AK 10, 35 PO 90 – 35 AB 50/PC	
R1 (2.5 m); Order number	GJR5139300R1
R2 (5 m); Order number	GJR5139300R2
R3 (10 m); Order number	GJR5139300R3
R4 (20 m); Order number	GJR5139300R4
Dialogue cable 35 UK 20, 35 PO 90 – 35 US 50	
R1 (1 m); Order number	GJR5142000R1
Engine speed set value cable 35 AK 30	
R1 (2,5 m); Order number	GJR5139500R1
R2 (5 m); Order number	GJR5139500R2
Initiator cable 35 AK 40	
R1 (2,5 m); Order number	GJR5139600R1
R2 (5 m); Order number	GJR5139600R2
Position encoder cable 35 AK 60	
R5 (5 m) Order number	GJR5142200R5
R6 (10 m); Order number	GJR5142200R6
R7 (20 m); Order number	GJR5142200R7
Position encoder cable 35 AK 70 for AXODYN® inverter, construction DRH	
R1 (2.5 m) Order number	GJR5142300R1
Incremental position encoders (for adapter flanges with a location hole with a diameter of 50 mm)	
500 pulses per revolution, Order number	GJV3075101R1
1000 pulses per revolution, Order number	GJV3075101R2
Proximity encoders (Initiators)	
NJ 5–18 GK 50-E3 (closed-circuit current), Order number	GJV3200001R2
NJ 5–18 GK 50-E2 (working current), Order number	GJV3200003R2

10.1.3 Description

The 35 PO 90 R101 single axis positioning unit serves the automatic positioning of a servo drive in the ABB Procontic T300 control system. It is almost identical in its function to the unit 07 PO 60 from the ABB Procontic T200 control system and the 35 AM 50 unit from the AXUMERIK® m system.

The 35 PO 90 single axis positioning unit controlled by a micro controller processes user programs consisting of NC sets, which it stores and manages itself. The 35 AB 50 operating unit serves to program the NC sets and displays.

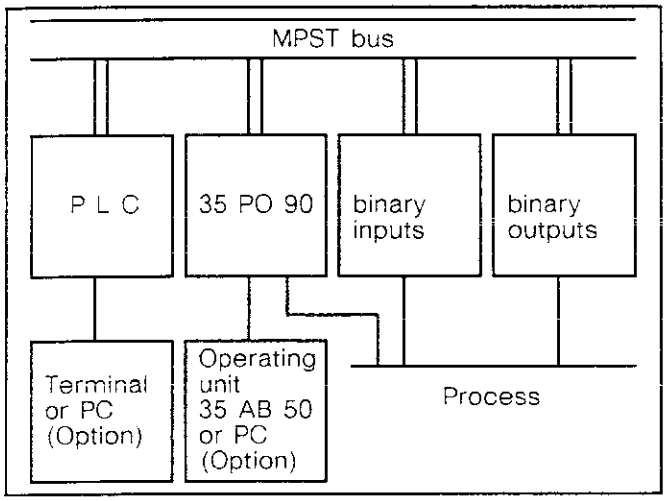
The user program archiving on an PC as well as the user program input and transmission from the PC to the 35 PO 90 can be done with a IBM compatible PC, e.g. Compaq PC. These are allowed by the PC software 935 AM 50.

A maximum of 256 35 PO 90 single axis positioning units can operate in an ABB Procontic T300 system at the same time. Each unit can be inserted in the basic subrack or in extension subracks.

The control of the user program sequence via the MPST bus is supported by special PLC blocks (POKANF, POKO and POKEND).

The 35 AB 50 operating unit (or the personal computer) and all the process signals are connected to the front panel of the units via interfaces and pin connections. Light-emitting diodes (LEDs) are present to signalize operating status.

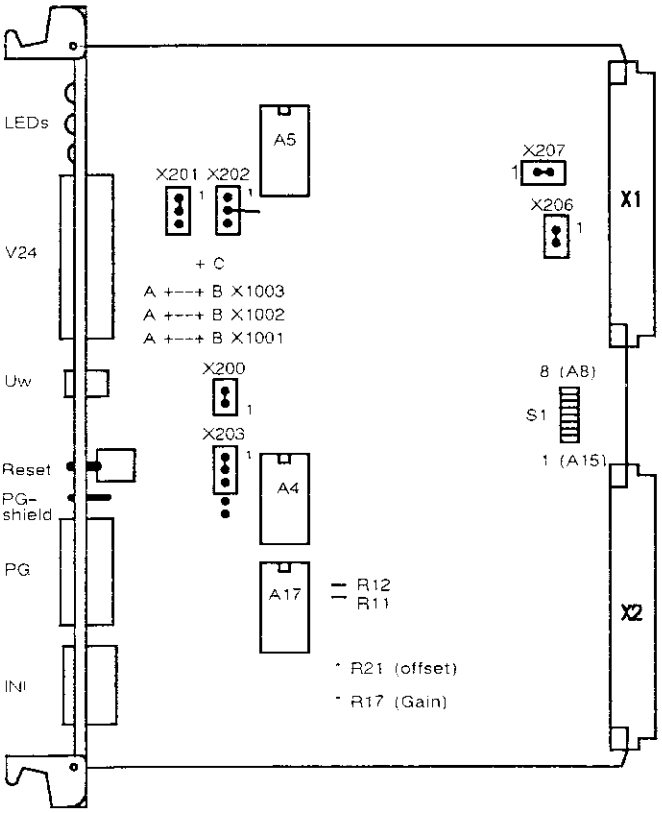
Example for the system configuration with the 35 PO 90:



10.1.4 Hardware description

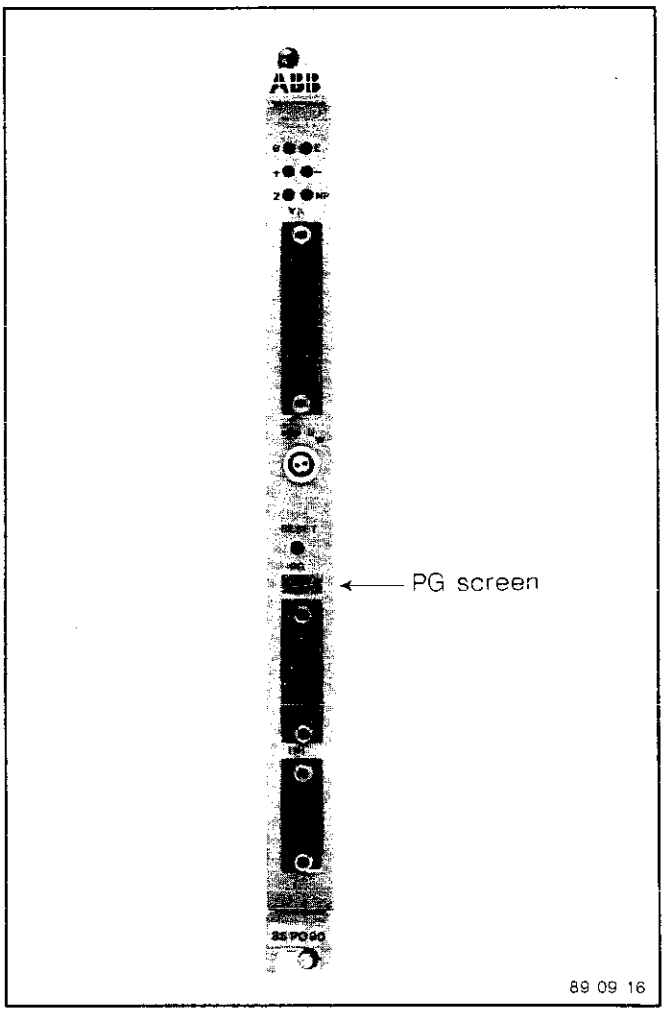
10.1.4.1 Printed board

Unit in the double-size Europcard format 160 x 233.4 mm, 1 pitch.



The drawn jumpers correspond to the factory settings; see also section 10.1.4.5, Settings.

10.1.4.2 Front panel



Meaning of the LEDs:

B: 35 PO 90 for PLC- positioning operating (see MPST bus output axis ready)
E: The limit position is approached
+: Positive drive direction
-: Positive drive direction
Z: Axis in the target window
NP: Maschine zero point (reference point) is approached

System cable connections:

V24: Serial interface (35 AB 50 operating unit or personal computer)
Uw: Speed set value
PG: Position encoder
INI: Initiators

Reset button:

Reset: Single card reset

10.1.4.3 Summary of the plugs

Code	Interface, plug	Design	Pole
X7 (V24)	Operating unit or personal computer	SUB-D plug	25
X6 (PG)	Incremental sensor input	SUB-D plug	15
X3 (Uw)	Set value output	Special plug	2
X4 (INI)	Initiator input	SUB-D plug	9
X1	MPST bus	DIN 41612, part 2, construction form C	30
X2	MPST bus	DIN 41612, part 2, construction form C	30

10.1.4.4 Assignments

MPST bus interface, plugs X1, X2
Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U_{B1}	5 V voltage	X1. 2c	U_{B1}	5 V voltage
X1. 4a	U_{B1}	5 V voltage	X1. 4c	U_{B1}	5 V voltage
X1. 6a	U_{B3}	- 15 V voltage	X1. 6c	U_{B2}	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{PFD}$	Power Failure Detect
X1.26a	-	-	X1.26c	-	-
X1.28a	$\overline{BB}$	Bus Busy	X1.28c	$\overline{RBB}$	Reset BusBusy
X1.30a	$\overline{SRQ}$	Service Request	X1.30c	$\overline{HSRQ}$	Hold Status SRQ
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{BOV}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	SYNC	Synchronisation signal	X2.20c	$\overline{CC}$	Central Clock
X2.22a	-	-	X2.22c	$\overline{RS}$	Reset
X2.24a	$\overline{W}$	Write	X2.24c	$\overline{R}$	Read
X2.26a	$\overline{I/O}$	I/O memory area	X2.26c	-	-
X2.28a	$\overline{DMARQ}$	DMA Request	X2.28c	DMACK	DMA Acknowledge
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

Serial interface (V24)

PIN	Signal name	Meaning	Comment	I/O
X7.1	Screen	Protective ground		
X7.2	/TxD	Transmit data	RS422/232C	O
X7.3	/RxD	Receive data	RS422/232C	I
X7.7	GND	Signal ground		
X7.9	0 V	Operating unit supply	closed only for X1002	O
X7.10	+24 V	Operating unit supply	closed only for X1001	O
X7.18	TxD	Transmit data	RS422	O
X7.21	RxD	Receive data	RS422	I

Position encoder interface (PG)

PIN	Signal name	I/O
X6.1	Screen	
X6.2	Encoder supply ext. +5V/+15V (X203)	O
X6.3	Encoder supply 0 V	O
X6.4	Encoder supply 0 V	O
X6.5	Encoder supply 0 V	O
X6.6	Encoder supply 0 V	O
X6.7	Encoder supply ext. +5V/+15V (X203)	O
X6.8	Track A	I
X6.9	Track /A	I
X6.10	Track B	I
X6.11	Track /B	I
X6.12	Track /C	I
X6.13	Track C	I

Speed set value interface(Uw)

PIN	Signal name	I/O
X3.1	Uw = +/- 10V	O
X3.2	Uwn = 0 V	O
	Screen	

Initiator interface (INI)

PIN	Signal name	I/O
X4.1	0 V (signal) and 0 V (Up)	I
X4.2	Release	I
X4.3	Limit position +	I
X4.4	Limit position -	I
X4.5	Reference point initiator	I
X4.6	Reserved	I
X4.8	Supply of the 35 PO 90 with the 24 V (UP)	I
X4.9	Supply of the 35 PO 90 with the 24 V (UP)	I

10.1.4.5 Settings

Setting the module number through switch S1
A module number must be set on the 35 PO 90 (switch S1). If several 35 PO 90 units operate in the same ABB Procontic T300 system, a different module number must be set on each 35 PO 90 unit.

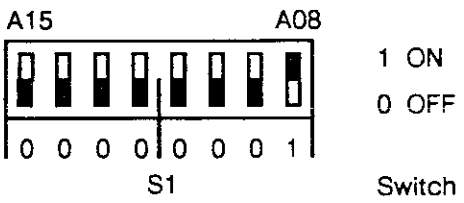
The module number is a part of the ABB Procontic T300 address. The T300 address is in the passive subscriber area of the MPST bus. The module number serves to address the 35 PO 90 by the PLC.

Attention is to be paid during the configuration to the fact, that overlaps of the ABB Procontic T300 address areas of the 35 PO 90 with memory cards or other passive T300 subscribers are avoided (recommendation: start with 0 when assigning the 35 PO 90 module numbers).

Assignment of the module number to the MPST bus address area:

Module number	ABB Procontic T300 Address area
0	2000:FF00 - 2000:FFFF
1	2000:FE00 - 2000:FEFF
:	: :
255	2000:0000 - 2000:00FF

Example: Setting the module number with switch S1:



This example shows module number 1 (00000001 B).

Jumpers

Jumper	Position	Meaning
X200	1-2 *	Processor clock ON
X201	1-2 *	A5 = 8 K * 8 EEPROM
X202	open *	A5 = 8 K * 8 EEPROM
X203	1-2 *	Internal encoder supply +5 V
X203	2-3	Internal encoder supply +15 V
X203	open	External encoder supply
X206	1-2 *	Position evaluation clock ON
X207	1-2 *	Watchdog ON

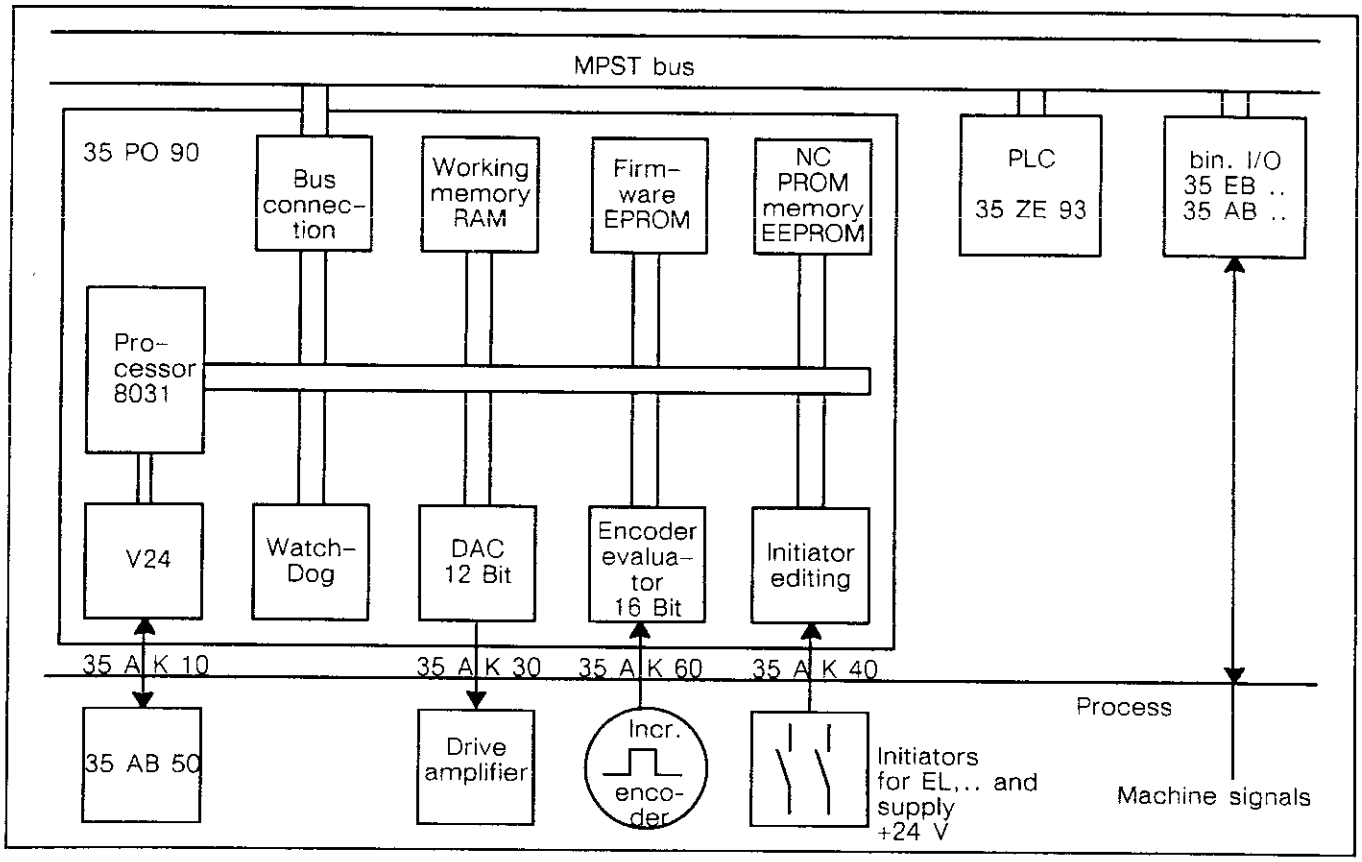
* Factory presetting

Soldering jumpers

Soldering jumper	Position	Meaning
X1001	A-B *	Operating unt +24 V: on
X1001	open	Operating unit +24 V: off
X1002	A-B *	Operating unit +0 V: on
X1002	open	Operating unit +0 V off
X1003	A-B *	Serial interface X7 on RS422
X1003	A-C	Serial interface X7 on RS232C

* Factory presetting

10.1.4.6 Block diagram



10.1.5 Firmware description

10.1.5.1 Functional summary

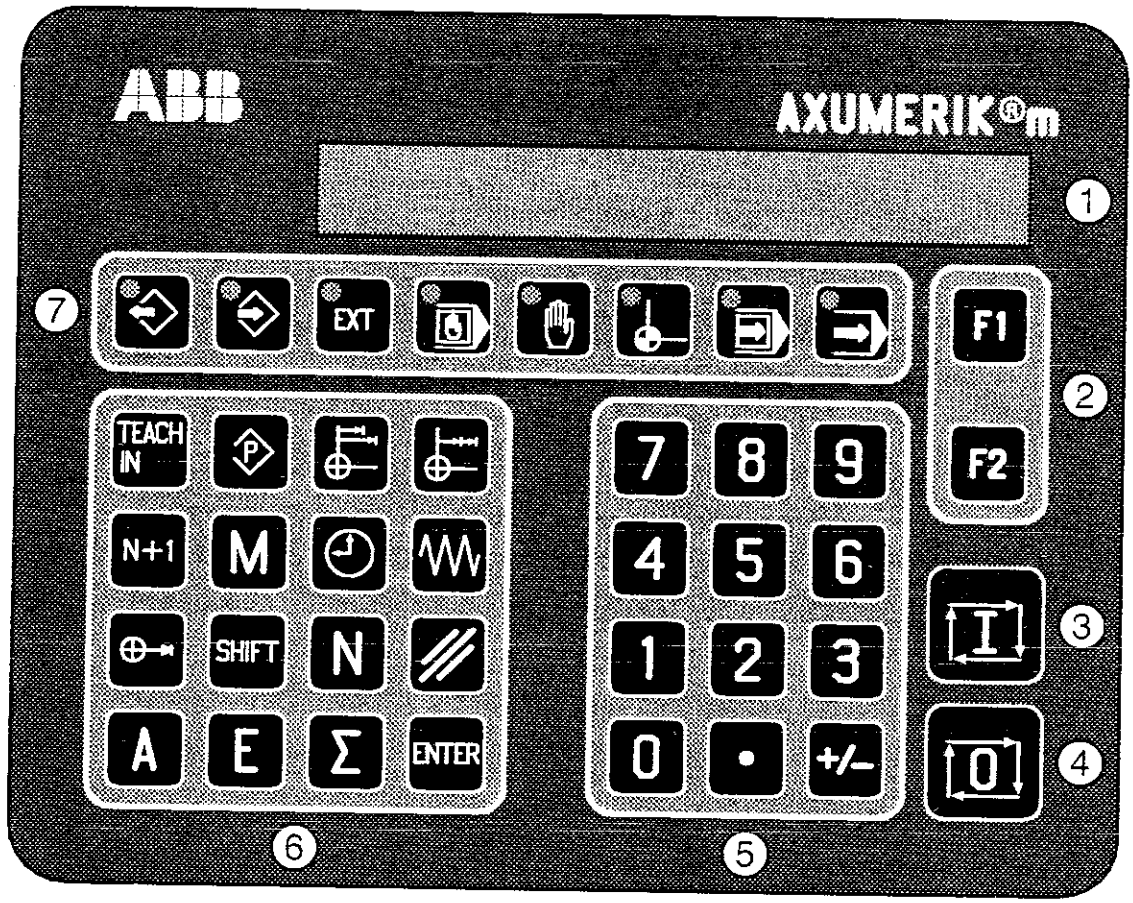
Access to the 35 PO 90:
- Programming with the 35 AB 50 operating unit or in the DNC mode (Compaq PC)
- Operating the programmed 35 PO 90 is possible without an operating unit (controlled by PLC)

Programming and operation:
- Programming in NC sets:
  - Machine data set for 20 machine-specific parameters
    - Maximum traversing speed 12m/min with 1 µm resolution
    - Programmable start-up and braking ramps 10 ms to 10 s
    - Single, double and 4-fold evaluation of the position encoder
    - Progamming the position set values in any desired unit of measurement
    - Software limit switches
    - Soft or hard reference point traversing selectively
  - Positioning sets
    - Positioning area ± 7 decades
    - Start-up and braking linear or according to a $\sin^2$ characteristic line
    - Traversing speed setable by the software
    - Teach-in of position set values
  - Sub program sets (loop sets)
  - Special sets
    - Moving to the reference point
    - Zero point shift
    - Manual control
    - Tool correction
    - Speed override
    - Programmable flag positions
- 4 user program segments in a non-volatile memory (EEPROM)
  - The above-mentioned NC set types are available in every program segment.
- The user program sequence can be controlled in various operating modes either by the operating unit, by the PLC or by the PC.

Differences between AXUMERIK® m and 35 PO 90:
The basic difference between the 35 PO 90 and the AXUMERIK® m is that the 35 PO 90 does not have the binary in-/outputs of the AXUMERIK® m. These binary in-/outputs serve for the communication between the AXUMERIK® m and a PLC in the external operating modes. The PLC communicates with the 35 PO 90 via its MPST bus in- and outputs.

Exchange of data between the 35 PO 90 and the PLC:
- The exchange of data between an active ABB Procontic T300 subscriber (PLC, IR 86 etc.) and the 35 PO 90 is carried out via the MPST bus in- and outputs of the 35 PO 90 (see sections 10.1.5.5.1 and 10.1.5.5.2).
- The 35 PO 90 is a passive T300 subscriber. It does not have active (automatic) access to other T300 units.
- The 35 PO 90 must be controlled by an active T300 subscriber(PLC, IR 86) in the external operating modes.
- Special PLC blocks support the operation of the 35 PO 90 (935 PC 83 starting from R0401 BLOCK POKO, POKANF and POKEND).

10.1.5.2 Operating and programming unit 35 AB 50



1 – 16-digit alpha-numerical display of the key assignments:

2 – Special function keys:
- F1 : Start-up and brake characteristic
- F2 : Axis selection (with 35 US 50)

3 – Start key

4 – Stop key

5 – Digit input with a sign and a decimal point

6 – Function keys for programming the set parameters (from the top left-hand corner to the bottom right-hand corner):
- Teach-in
- Parameter selection
- Absolute measuring system (ABS)
- Incremental measuring system (INC)
- Subset (N+1)
- Machine function (M-fct))
- Dwell time (DWELL)
- Feed (FEED)
- Zero point shift
- Shift key
- Set number (N)
- Delete key
- Starting set number (STAE)
- Ending set number (ENDS)
- Loop number (sum)
- Enter key

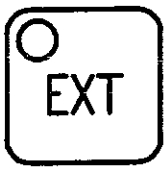
7 – Keys for the operating modes (from left to right):
- EPROM writing (out of service !)
- EPROM reading (out of service !)
- EXTERNAL
- Manual entering of data
- Manual control
- Moving toreference point
- Operating unit: automatic single set
- Operating unit:automatic subset

10.1.5.3 Operating modes

An operating mode is not selected, when the supply voltage is switched on. The selection of an operating mode can be carried out using an operating unit (keys for the operating modes), via the PLC (operating mode selection) or via the PC (in the DNC mode).

10.1.5.3.1 Keys for the operating mode

External:



Activating an external operating mode depending on the status of the external "operating mode selection" (only if a key for the operating mode was previously active).

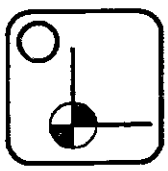
Manual entering of data:

The set data can be programmed and altered via the keyboard for the operating modes in this operating mode. Position set values can be accepted by "teach-in" in positioning sets.

Manual control:

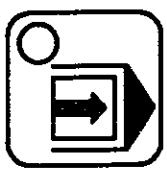
The axis can be moved by means of the "sign key" and the "start key" with the speed pogrammed in the corresponding manual control set in this operating mode. The axis moves in the direction pregiven with the "sign key", while the "start key" is pressed. The drive direction is saved, until the "start key" is released.

Move to reference point:



The axis approaches its reference point in its operating mode, after the direction has been preselected with the "sign key" and the "start key" has been pressed. The speed is the speed programmed in the corresponding reference point set. The programmed machine function is output.

Key for the automatic single set mode (Bed/AE):

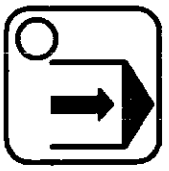


If this operating mode is selected and a set (e.g., M030) is recalled, this set is executed, after the "start key" has been pressed. If a subset is programmed in this set (N+1 ± 255), this is also executed, when the "start key" is pressed again, if a new set was not selected via the keyboard. If there is no subset given (N+1 = 255), the program processing is interrupted, when N255 has been executed. A new set must be selected.

The positioning procedure is interrupted with the "brake mode in case of failure" programmed in the machine data set, if the "stop key" is pressed. The processing of the interrupted set is continued at the same position, if the "start key" is pressed again, if another set was not selected.

The subset number appears in the display with a comment and its position actual value, when the set position has been reached. The programmed machine function is output.

Key for the automatic subset mode (Bed/AF):



As for Bed/AE except for the fact that the subsets are automatically processed as well, if the "start key" was pressed once, until there is subset programmed in a set (N+1 = 255) the downtime between two positions corresponds to the programmed "dwell time".

10.1.5.3.2 External operating modes

An external operating mode is requested via the PLC (MPST bus input "operating mode selection"). It becomes active only if the MPST bus outputs "operating mode quit" match the selection. An external operating mode remains valid after an alteration to the "operating mode selection",until the "operating mode quit" has been adapted accordingly.

The operating unit is not absolutely necessary in all external operating modes. It serves to display the set numbers and the position actual values and offers the possibility of a program abortion after the "brake mode in case of failure" programmed in the MDS in all external operating modes with the "stop key" as well as the display of the ABB Procontic T300 in- and outputs.

External automatic single set mode (Ext/AE):
A set is selected by the PLC and started with a "start" in the operating mode EXT/AE. The continued sequence is determined by the subsets. The CNC only gives the "start" signal (0 -> 1 flank necessary), after a set has been processed, to start the subset. If there is no subset programmed in a set (N+1 = 255) or if the "set number" is set to N255, the program sequence is interrupted after "start" and the processing of set N255 ("set executed" becomes 0 for 200 ms).The new selection of a set is necessary.

If a set, which has already been executed in the same program sequence, is a subset in a set, this program is executed continuously, until it is interrupted by pressing the "stop key" on the operating unit or by the PLC (set number N255, no other "start" signals changing the "operating mode selection").

The program sequence can be continued at the same position, after it has been interrupted with the "stop key" , by pressing the "start key" and a new "start" signal from the PLC. The programmed "machine function" is output.

External automatic subset mode (Ext/AF):
The 35 PO 90 is given a set with the "set number" in the operating mode Ext/AF and started with the "start" signal. The subsequent program sequence is determined by the programmed subsets. The PLC only gives a single "start" signal (permanent signal). The other start signals are given internally, when the programmed dwell time is over, while the "start signal"=1. If there is no " subset" programmed in a set (N+1=255), the program sequence is interrupted, after the set N255 has been executed ("set executed" becomes 0 for 200 ms).

If a set, which has already been executed in the same program sequence, is a subset in a set, this program is continuously executed, until it is interrupted by pressing the "stop key" on the operating unit or by the PLC ("start" signal = 0 or changing the "operating mode selection"). If the "set number" is altered to N+1= 255 after an interrupted positioning procedure and before another "START", the set processing is interrupted, after the set N255 has been executed ("set executed" becomes 0 for 200 ms). Another set must be selected.

The program sequence can be continued at the same position, after the interruption of the program sequence with the "stoo key" by pressing the "start key" and another " start" signal from the PLC. The programmed "machine function" is output.

External (Ext):
In this operating mode the 35 PO 90 includes all the control signals from the master control (PLC), which also determine the program sequence.

The program sequence can be continued at the same position, after the interruption of the program sequence with the "stop key" by pressing the "start key" and another " start" signal from the PLC. The programmed "machine function" is output.

The special sets, " move to reference point", "manual control" as well as the "teach-in" function can be activated in the operating mode "Ext".

10.1.5.3.3 DNC mode

The DNC mode enables the central archiving of the 35 PO 90 NC programmed on a PC as well as editing and printing out 35 PO 90 NC programs via the PC. All NC sets can be read out, altered and stored in the EEPROM (user program memory) by the PC in the DNC mode (according to the selected user program segment).

The DNC mode is supported by the PC software 935 AM 50 (see section 10.1.6).

The DNC mode between the 35 PO 90 and the PC is only possible, if neither the keys for the operating modes nor an external operating mode is active (MPST bus input "operating mode selection" and MPST bus output "operating modes quit" = 0, or the keys for the operating modes were reset with the "external" key. If the DNC mode is to be realised without the 935 AM 50 PC software, the telegram frame described in the interface protocol section is to be observed. The interface protocols for the DNC mode are also described in the interface protocol section.

RAM mode:
The RAM mode is a special form of the DNC transfer. It serves as a fast DNC transfer for position sets and the machine data set.

The sets transmitted via the serial interface are stored in the working memory (RAM) and not in the non-volatile program memory (EEPROM) of the 35 PO 90. The program memory remains unaltered here.

Direct DNC transfer:
A position set can be transmitted and started (even in parts) by means of a DNC telegram (without the PLC "start" signal).

Reading out the position actual value by DNC:
The actual position value of the 35 PO 90 referring to the machine reference point can be read out by means of a DNC telegram.

10.1.5.4 Programming

All the sets listed in section 10. 1. 5. 4. 2 result in a "user program segment" (UP segment). 4 UP segments are available in the non-volatile EEPROM. The user therefore has the possiblility of storing all the set numbers 4 times. The user selects the currently active

UP segment via the PLC. Note the instruction in section 10.1.5.5.1, paragraph: UP segment. Programming the 35 PO 90 is carried out in sets with the 35 AB 50 operating unit or by transmitting the NC program from a PC to the 35 PO 90 in the DNC mode.

10.1.5.4.1 Function keys for the operating units

Teach-in:

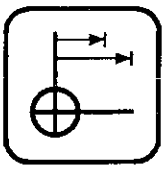
This is only effective in the operating mode "Ext" or "manual entering of data". The teach-in programming means: move the axis into the desired position in the set-up mode (manual or touch mode) and set this position actual value as the position set value of a position set.

Procedure with the "operating mode manual entering of data":
- Move the axis into the desired position.
- Select the operating mode "manual entering of data".
- Recall of the set to be programmed, e.g. N70 with the keys: N, 0, 7, 0
- Press the "teach-in " key -> the position actual value appears in the display of the operating unit.
- Setting the position actual value as the position set value of the selected set with the "enter" key.
- Enter the other set parameters (FEED, DWELL, N+1, etc.) as before.

Parameter selection:

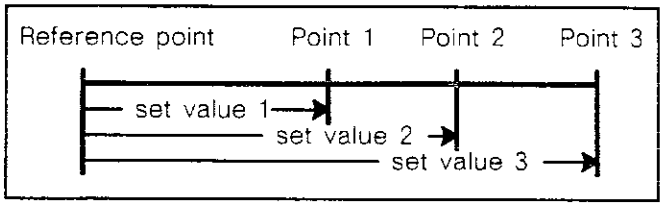
Selection of the parameters P01 to P20 of the machine data set. This is only effective in the operating mode and "manual entering of data".

Absolute measuring system (ABS):



The entered position set value refers to a fixed reference point.

Example:

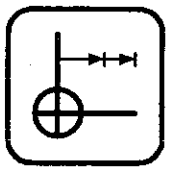


Set value 1 = 350 increments
Set value 2 = 600 increments
Set value 3 = 1100 increments

The position set value set 1 must be re-activated to return from point 3 to point 1.

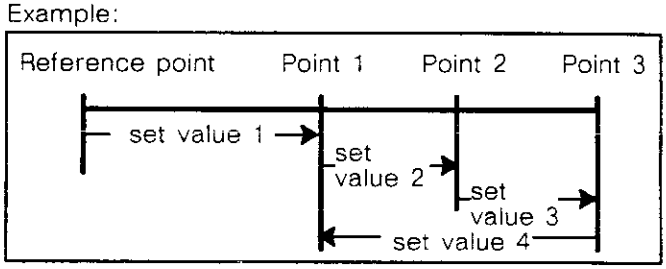
This is only effective in the operating mode "manual entering of data".

Incremental measuring system (INK):



The entered position set value refers to the position actual value before the "start" of the set.

Example:



Set value 1 = 350 increments
Set value 2 = 250 increments
Set value 3 = 500 increments
Set value 4 = -750 increments

The position set value 4 must be activated to return from point 3 to point 1.

This is only effective in the operating mode "manual entering of data".

Subset (N+1):

Entry of the subset (0 - 255).

The subset indicates, with which set the program is to be continued according to the operating mode. It must always be programmed during the program compilation (subset operating modes). If a program is to be ended, "N + 1" = 255 must be programmed.

If the same number is programmed in a set as a subset, this set is executed according to the operating mode (e.g., Bed/AF), until the program sequence is interrupted (e.g., "stop key") (only significant for an incremental measurement input).

This is only effective in the operating mode "manual entering of data".

M FUNCTION (Machine function):

The "machine function" of a set (-999 to +1000) is output during the set processing.
If the "machine function" of a set was programmed positively, it is output, when the set processing is finished.

If the "machine function" of a set was programmed negatively, it is output with the start of the set processing.

An output "machine function" is available in the MPST bus outputs, until it is overwritten by another output of a machine function.

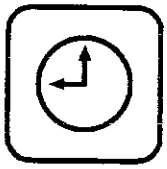
If the machine function is programmed to the value 1000, there is no machine function ouput in this set. The last output machine function remains valid. This is used, if the same subset is to be accessed from, e.g., wo different sets with a different machine function. The PLC can as certain using the machine function, which set accessed the subset, after the subset has been executed, and proceed accordingly.

Example:

N020, Machine function 02, N + 1 = 120
N050, Machine function 05, N + 1 = 120
N120, Machine function 1000

This is only effective in the operating mode "manual entering of data".

Dwell time (DWELL):



Key to recall the dwell time of the parameter. Programming possible from - 0,1 s to 327 s .

'Programming of "DWELL" = 0 s to 327 s:
The subset is automatically started in the automatic subset operating modes, when the programmed dwell time is over.

Programming "DWELL" = - 0.1 s:

The position set value of the set is moved over (without exact positioning). The subset is executed without another start signal.

It is not allowed to program "DWELL" = - 0.1 in 2 consecutive sets.

The machine function of a set with DWELL = - 0.1 is only output, if it was programmed negatively.

This is only effective in the operating mode "manual entering of data".

Feed (FEED):

This is only effective in the operating mode "manual entering of data":

Key to recall the parameter drive speed. The programming is possible from 0 to 32752.
If the programmed FEED value is above the parameter Vmax (P04 MDS), the speed Vmax is used for the set processing.

The feed can also be entered or displayed in the desired unit of measurement by means of P11 MDS.

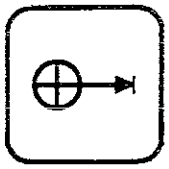
The following is valid for P11 MDS = 0: incremental input of FEED in increments/(1/12.5) s

See section: set types (enter P11 MDS)

A switchover from the position actual value display to the speed actual display can be carried out by means of the FEED key during the position mode.

The following is valid:
- Speed display for P11 MDS = 0:
  Display = FEED actual value / 16
- Speed display for P11 MDS ≠ 0:
  FEED actual value display in the corresponding unit of measurement.

Zero point shift:



Key to recall the position actual value parameter for the zero point shift sets.

This is only effective in the operating mode "manual entering of data".

Shift key:

The individual set parameters are switched forwards in sequence when entering a set by means of the "shift key".
This is only effective in the operating mode "manual entering of data".

Set number (N):

Key to select the set numbers in the operating modes "manual entering of data", Bed/AE, and Bed/AF.

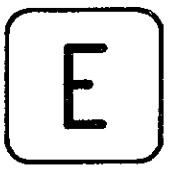
Delete key:

This is only effective in the operating mode "manual entering of data": Incorrect entries can be deleted with the delete key (only before confirmation of the entry with the "enter key").
For all operating units and external operating modes except for "manual entering of data": the error messages displayed on the operating units are acknowledged with the "delete key".

Start set (A):

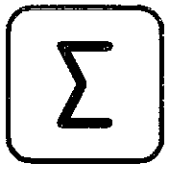
This is only effective in the operating mode "manual entering of data": Selection of the "start set" set parameter when entering the loop set.
For all operating modes except for "manual entering of data":
Display of the MPST bus outputs on the operating unit (see section 10.1.5.5.1 and section 10.1.5.5.2).

End set (E):



This is only effective in the operating mode "manual entering of data": Selection of the "end set" set parameter when entering a loop set.
For all operating modes except for "manual entering of data":
Display of the MPST bus inputs on the operating unit (see section 10.1.5.5.1 and section 10.1.5.5.2).

Number of loops:



Selection of the "number of loops" set parameter when entering a loop set.
This is only effective in the operating mode "manual entering of data".

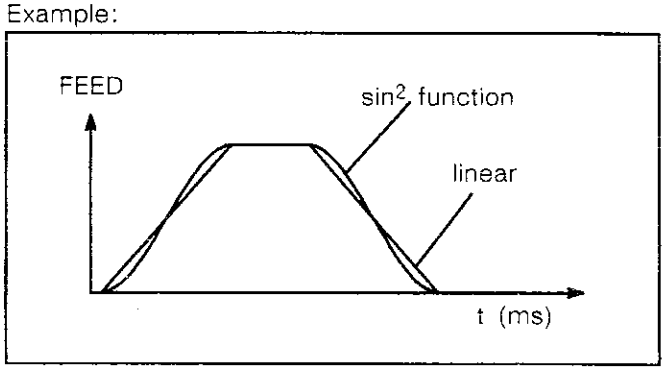
Enter key:

Saving a programmed or an altered set in the non-volatile memory of the 35 PO 90 (in the currently selected user program segment). This is only effective in the operating mode "manual entering of data".

Acceleration and brake characteristic (F1):

When entering a position set, the key "F1" selects, whether the entered start and brake ramps (MDS) are moved in a linear way or according to a $\sin^2$ function.

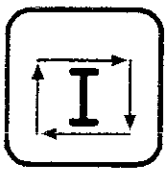
Example:



Axis switchover (F2):

This is only effective when working with the 35 US 50 (electronic switchover logic for operating a maximum of 6 units 35 PO 90 via an 35 AB 50 operating unit or a PC): Selection of the 35 PO 90 via the operating unit.
See AXUMERIK® m system description, section 18, Electronic switchover logic.

Start key:

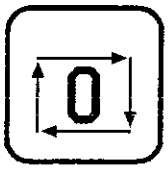


Starting a previously selected set in the operating modes "Bed/AE" and "Bed/AF".
Starting the axis in the operating mode "move to reference point".
Moving the axis in the operating mode "manual control" (while the "start key" is pressed).

Renewed start of the axis drive after an interruption of the set processing (with enable initiator = 0 and "stop key" pressed) in the keys for the operating modes (except for "manual entering of data").

Releasing the 35 PO 90 for starting the axis drive again after an interruption of the set processing with the "stop key" in all external operating modes.

Stop key:



Interrupting the positioning procedure with the "brake mode in case of failure" determined in P08 (MDS). This is effective in all operating modes, except for "manual entering of data".

10.1.5.4.2 set type and set structure

The sets listed in this section are available to the user in all 4 UP segments. Changing the switchover according to section 10.1.5.5.1 (section, UP segment).

Set types:

- Loop sets
- Position sets
- Special sets:
  - Machine data set (MDS)
  - Move to reference point
  - Manual control
  - Zero point shift
  - Flag positions
  - Tip sets
  - Speed override
  - Length correction sets
  - Scale factor
  - Software code

Loop sets:
Number of sets: 16

Set numbers: 00 to 15

Set contents:

Set no.	Start set	End set	Number of loops
N	16-165	16-165	0-255

Subset
0-255

Position sets:
The position set value entry is carried out depending on P11 MDS (P11 ≠ 0 → entry in the unit of measurement selected with P11, e.g., in mm).

Number of sets: 112

Set numbers: 16 - 127

Set contents:

Set no.	Measuring system	Acceleration and brake characteristic	Sign	Position set value
N	ABS/INK	lin/sin²	+/-	0-9999999

Feed	Dwell time	Machine function	Subset
0-32752	-0,1-327	-999 - +1000	0-255

Move to reference point (positive drive direction):
Number of sets: 4

Set numbers: 132, 160, 161, 162

Set contents:

Set no.	Feed	Dwell time	Machine function	Subset
N	0-32752	0-327	-999 - +1000	0-255

Move to reference point (negative drive direction):
Number of sets: 4

Set numbers: 133, 163, 164, 165

Set contents:

Set no.	Feed	Dwell time	Machine function	Subset
N	0-32752	0-327	-999 - +1000	0-255

Manual control (positive direction):
Number of sets: 1

Set numbers: 134

Set contents:

Set number	Feed
N	0-32752

Manual control (negative direction):
Number of sets: 1

Set numbers: 135

Set contents:

Set number	Feed
N	0-3272

Zero point shift:
The previous position set value is replaced by the position set value given in the zero point shift set after its recall. The entry of the position set value is carried out depending on P11 MDS (P11 ≠ 0 -> entry in the unit of measurement selected with P11 e.g., in mm).

Number of sets: 4

Set numbers: 148, 149, 150, 151

Set contents:

Set no.	Dwell time	Machine functions	New position set value
N	0-327	-999 - +1000	+/-9999999

Subset
0-255

Flag positions:
Positive flag position value:
If the axis moves over a flag position in the positive direction, the corresponding MPST bus output is set. If the axis moves over a flag position in the negative direction, the corresponding MPST bus output is then reset.

Negative flag position value:
If the axis moves over a flag position in the negative direction, the corresponding MPST bus output is then set. If the axis moves over a flag position in the positive direction, the corresponding MPST control output is then reset.

Number of sets: 3

Set numbers: 144, 145, 146

Set contents:

Set no.	Flag position
N	+/-9999999

Tip sets (postive drive direction):
The axis is moved by the set value given in the comment after the "start" of a tip set.

Number of sets: 4

Set numbers: 152, 153, 154, 155

Set contents:

Set no.	Feed	Subset	Comment
152	0-32752	0-255	+1 INK
153	0-32752	0-255	+10 INK
154	0-32752	0-255	+100 INK
155	0-32752	0-255	+1000 INK

Tip sets (negative drive direction):
The axis is moved by the set value given in the comment after the "start" of a tip set.

Number of sets: 4

Set numbers: 156, 157, 158, 159

Set contents:

Set no.	Feed	Subset	Comment
156	0-32752	0-255	-1 INK
157	0-32752	0-255	-10 INK
158	0-32752	0-255	-100 INK
159	0-32752	0-255	-1000 INK

Override sets:
Activating the internal speed correction values (override) is carried out via the PLC. If an internal override is active, the axis is moved with 0 to 120% of the parameter "FEED" (depending on the override value programmed in the override set).

Number of sets: 2

Set numbers: 136, 137

Set contents:

Set no.	Override value
N	0-120

Length correction sets (tool correction):
Activating a length correction value is carried out via the PLC. If an internal length correction is active, the length correction value is added to the position set value of the position set. The input of the length correction value is carried out depending on P11 MDS (P11 ≠ 0; input in the unit of measurement selected with P11, e.g., in mm).

Number of sets: 2

Set numbers: 138, 139

Set contents:

Set no.	Length correction value
N	-9999999 - +9999999

Scale factor:
Activating the scale factor is carried out via the PLC. If the scale factor is active, the following number of increments is moved with the execution of "INK" programmed position sets: position set value x scale factor (0 to 200%).

If the scale factor is active, the absolute position value is approached with the execution of "ABS" programmed position sets (position set value x scale factor (0 to 200%)).

Number of sets: 1

Set numbers: 140

Set contents:

Set no.	Scale factor
140	0-200

Software code:
Display of the 35 PO 90 firmware version number on the operating unit in the operating mode "manual entering of data".

Number of sets: 1

Set numbers: 999

Set contents:

Set no.	Version number
999	35 PO 90 FW Vx.x

Machine data set:
All the machine-specific parameters are stored in the machine data set. The MDS is activated with the switchover of the UP segment according to section 10.1.5.5.1 (section: UP segment).

Number of sets: 1

Set numbers: 190

Set contents:

Set no.	Parameters P01-P20
190	See the table for the parameters of the machine data set

Parameters of the machine data sets:

Parameter number	Meaning	Minimum value	Maximum value	LLevel	Unit
P01	Kp factor	0.01	19.50	0.01	
P02	Positive software limit switch	0	+9,999,999	1	Incr. *
P03	Negative software limit switch	0	-9,999,999	1	Incr. *
P04	Maximum feed (Fmax)	0	32,752	1	$\frac{\text{Incr.}}{(1/12.5)\text{s}}$ *
P05	Acceleration time (acceleration ramp)	10	10,000**	1	ms
P06	Brake time (brake ramp)	10	10,000**	1	ms
P07	Reserved (standard entry = 0)				
P08	Brake ramp in case of failure 1 = set value and set following error to 0 2 = processing the following error 3 = along the brake ramp	1	3	1	
P09	Drift constant	0	9	1	5 mV
P10	Maximum permitted following error	0	32,752	1	Incr. *
P11	Transfer factor	0	3,200.0	0.1	
P12	Sensor evalution, single double or 4-fold		1, 2, or 4		
P13	Decimal places	0	4	1	
P14	Acceleration and brake characteristic for manual operation and move to reference point 0 = linear 1 = $\sin^2$		0 or 1		
P15	Move to reference point 0 = soft reference point drive 1 = hard reference point drive		0 or 1		
P16	Reserved (standard input = 0)				
P17	Upper setting limit UW max +	0	+2,047	1	
P18	Lower setting limit UW min -	0	-2,047	1	
P19	Target window	0	32,752	1	Incr. *
P20	Reserved (standard input = 0)				

* for P11 = 0, all other inputs in desired scale.
** for P04 > 10, 000 (with P11 = 0);
otherwise see p04 description

Note: When entering the MDS with the 935 AM 50 PC software, note section 10.1.6.4 (935 AM 50 PC software, special features when working with XEDiT).

P01 Kp factor:
The Kp factor is a proportional amplification factor, which results from the quotient of the set speed (Uw) and the difference between the position actual value and the position set value (following error).

A Kp factor of 1.00 means that the D/A converter (Uw) jumps approx. 5 mV per increment of the following error.

Note:
Entry of values < 0.1 as a Kp factor is generally not sensible. A rounding error of max. ± 0.01 can occur between the entry and display of the Kp factor.

P02/P03 software limit switches:
The user can limit the maximum traversing range of the machine with the software limit switches.

This is valid for position sets, tip sets and in the operating mode "manual control".

If the axis reaches a position value, which corresponds to one of the software limit switches, the axis stops according to the "brake mode in case of failure" determined in P08 (MDS) and output the corresponding error message on the operating unit.

If the value 0 is programmed for both software limit switches (supply status), the software limit switches are put out of service.

The software limit switches are only activated after a reference point drive.

A zero point shift by means of the sets N148 to N151 has no effect on the software limit switches.

The entry value of the software limit switches depends on P11.

P04 maximum feed (max. drive speed):
The maximum drive speed must always be programmed due to the 35 PO 90 internal standards. The entry value for P04 is dependent on P11. The value of Fmax is calculated as follows:

a) For the measuring input in increments (P11 = 0):
n max -> max. speed of the motor
Gc -> Encoder constant
Aw -> Encoder evaluation (P12 MDS)
R1 -> Motor/encoder transformation ratio

$$Fmax = \frac{\text{increments evaluated by 35 PO 90}}{(1/12.5)\ \text{seconds}}$$

The factor 1/12.5 results due to the 35 PO 90 internal numerical representation. Attention should be paid during the configuration to the fact, that a value > 10,000 results for Fmax (see P05/P06).Maximum value of Fmax = 32,752 incr./(1/12.5) s for P11 = 0

$$Fmax \quad \frac{n\ max \times Ec \times Aw}{12.5 \times R1} \quad \frac{\text{incr.}}{(1/12.5)s}$$

Example:
n max = 3,000 U/min = 50 rev./s
Ec = 1,000 incr./rev.
Aw = 4
R1 = 1/1 (e.g.,the encoder sits directly on the drive)

$$Fmax = \frac{50 \times 1000 \times 4}{12.5 \times 1} \frac{\text{incr.}}{(1/12.5)s}$$

$$Fmax = 16{,}000 \frac{\text{incr.}}{(1/12.5)s}$$

Fmax entry: 16,000

b) For the dimension entry in the desired measuring system (P11 ≠ 0):

$$Fmax = \frac{\text{Distance covered by the axis}}{\text{Second}}$$

Attention should be paid to the fact, that a value > (10.00 x 12.5)/P11 results for Fmax (see P05/P06).

Maximum value: Fmax = 32752 x 12.5 / P11 mm/s (for P11 ≠ 0)

n max -> Max. speed of the motor
R2 -> Motor/axis transformation ratio
H -> Spindle pitch

$$Fmax = \frac{n\ max \times H}{R2}\ mm/s$$

Example:

n max = 3,000 rpm = 50 rev./s
R2 = 2/1 (motor turns with twice as many revolutions as opposed to the axis)
H = 5mm/rev.

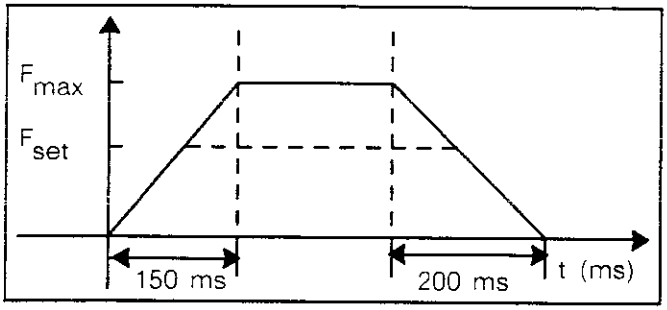
$$Fmax = \frac{50 \times 5}{2}\ mm/s = 125\ mm/s$$

Fmax entry: 125

P05/P06 acceleration and brake ramps:
The acceleration and brake times can be set in the range of 10 ms to 10 s, if Fmax has a significantly large value (see the diagram).

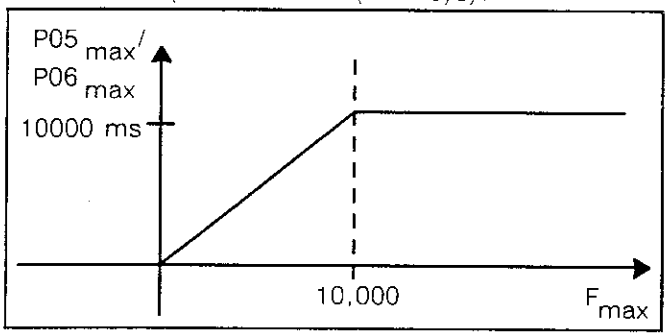
The given values are valid referring to P04 for all positions. e.g., if the transversing speed of a set is smaller than Fmax, this set speed is also obtained faster.

Example: P05 = 150ms, P06 = 200ms



The maximum value of P05 and P06 depends on P04 MDS (Fmax) and P11 MDS (transmission factor). If the value of P04 > 10,000 (with P11 = 0), values from 10 ms to 10 s can be programmed for P05/P06. If the value of P04 is smaller than 10,000 (with P11 = 0), a correspondingly smaller value can only be entered for P05 or P06.
(Example: P04 = 3,999, P11 = 0 => P05/P06max = 3,999).

For P11 = 0 (Fmax in incr./(1/12.5)s):



P08 brake mode in case of a failure:
I.e., after "enable" = 0, pressing the "stop key", releasing the "start key" for a manual control or after moving to the limit positions.

1: Set the set value and following error to zero (immediate, jolty stop of the axis)
2: Process the following error (the set processing is interrupted and the collected following error is still moved (without a ramp).
3: Along the brake ramp (the set processing is interrupted, the 35 PO 90 outputs a brake ramp, the brake ramp and the collected following errors are still moved.

If the positioning is interrupted in the brake mode 1 (e.g., the "enable initiator" is set from 1 -> 0), while the MPST bus output "position reached" is already set, the current actual position is accepted as the new set position of the 35 PO 90 (see also the function of the initiator signals).

P09 Drift constant:
The Kp factor can be enlarged by means of the drift constant for small following errors. An accurate position is guaranteed in this way.

P10 Max. permitted following error:
The MPST bus output "following error" is set, if the entered value is exceeded. The amount of P10 depends on P11.

P11 Transmission factor:
The transmission factor offers the possibility of processing position and speed values in any unit of measurement as well as displaying them (the entry in mm was selected each time in the examples). If P11 ≠ 0 is programmed, P11 should be entered before Fmax (P04) and all the position values.

The transmission factor is defined as follows:

$$P11 = \frac{\text{incr. evaluated by the 35 PO 90}}{\text{distance covered by the axis}}$$

E_c -> encoder constants
A_w -> encoder evaluation (P12 MDS)
R_3 -> encoder/axis transformation ratio
H -> spindle pitch

$$P11 = \frac{Ec \times Aw \times R3}{H}$$

Example:
E_c = 1000 Incr./rev.
A_w = 4
R_3 = 2/1 (The encoder turns with twice the speed as opposed to the axis)
H = 5mm/rev.

$$P11 = \frac{1000 \times 4 \times 2}{5} \frac{\text{Incr./rev.}}{\text{Rev./mm}} = \underline{1600\ \text{Incr./mm}}$$

P12 encoder evaluation:
The pulse rate of the incremental position encoder can be evaluated singly, doubly or 4-fold. Changing the resolution is achieved.

P13 Decimal places:
The number of the desired decimal places is entered with P13.

P13 is only effective, if P11 ≠ 0 and is only valid for position values.

P14 acceleration and brake characteristic for manual control or reference point drive:
The acceleration and brake characteristic for "manual control" and "move to reference point" is selected with P14.

0 -> linear
1 -> sin^2 function

P15 Move to reference point:
it is determined with P15, with which brake mode (P08) the 35 PO 90 reacts during the "move to reference point" to the approach of the limit positions or of the machine zero point.

0 -> move to soft reference point (brake mode 3)
1 -> move to hard reference point (brake mode 1)

P17/P18 Setting limits:
The positive or negative maximum output voltage of the 35 PO 90 can be limited for the set value output (Uw) with P17 or P18.

Uw max - = P18 x 4.88 mV

Uw max + = P17 x 4.88 mV
Example:

P17 = 1000, P18 = -2047 => -10V < Uw < +4.88 V

P19 Target window:
If the position actual value of the axis is within the position set value ± the target window, the MPST output target window is set. The output value for P19 depends on P11.

10.1.5.5 MPST bus interface

Total overview of the MPST bus interface:

T300 Address 2000:	Bit number	Meaning
0XX00H	0 ... 7	free
0XX01H : 0XX0FH	0 ... 7 : 0 ... 7	MPST bus Inputs
0XX10H : 0XX20H	0 ... 7 : 0 ... 7	free
0XX21H : 0XX2FH	0 ... 7 : 0 ... 7	MPST bus Outputs
0XX30H : 0XX40H	0 ... 7 : 0 ... 7	free
0XX41H : 0XX49H	0 ... 7 : 0 ... 7	Reserved for 35 PO 90 test software
0XX50H : 0XXFEH	0 ... 7 : 0 ... 7	free
0XXFFH	0 1 2 ... 7	Data channel status bit "START" Data channel status bit "FREE" n.c. (is always read = 1)

XX -> inverted module number of the 35PO90

The 35 PO 90 MPST bus interface is a memory area, which is 256 bytes large (data channels).

A part of this memory area undertakes the function of the binary in-/outputs for the AXUMERIK® m. This part of the MPST bus interface is called the MPST bus in-/outputs of the 35 PO 90 in the following.

The 35 PO 90 program sequence can be controlled by the PLC via the MPST bus in-/outputs.

The PLC makes special blocks available to operate the MPST bus in-/outputs of the 35 PO 90 (POKANF, POKO and POKEND, see PLC block catalogue). The user configurates the MPST bus in-/outputs of the 35 PO 90 via PLC flags in the PLC program.

10.1.5.5.1 MPST bus inputs

T300 Address 2000:	Bit number	Meaning
0XX01H	0 ... 7	Set no. 0H to 0FFH
0XX02H	0 ... 1 2 3 4 ... 5 6 ... 7	Select operating mode 0H to 3H Start Teach in Enable mode 0H to 3H free
0XX03H	0 ... 7	UP segment 0H to 0FFH
0XX04H 0XX05H	0 ... 7 0 ... 7	Override selection 0H to 0FFH Override value 0H to 0FFH
0XX06H 0XX07H 0XX08H 0XX09H 0XX0AH	0 ... 7 0 ... 7 0 ... 7 0 ... 7 0 ... 7	Select length correction 0H to 0FFH Length correction: lowest byte Length correction: low-mid byte Length correction: high-mid byte Length correction: highest byte 32 bit in the binary compliment
0XX0BH 0XX0CH 0XX0DH 0XX0EH 0XX0FH	0 ... 7 0 ... 7 0 ... 7 0 ... 7 0 1 2 ... 7	Reserve word 1 (LB) Reserve word 1 (HB) Reserve word 2 (LB) Reserve word 2 (HB) Delete the error number Reserve bit 1 free

Set number:

- For the selection of the NC set in all external operating modes
- Value range:
  0B to 011111111B (0 to 255)

Operating mode selection:

- Selection of external operating modes.
  The PLC can select an external operating mode, after the supply voltage has been switched on or after the selection of the operating mode "Ext" on the operating unit. Wait after selecting an operating mode, until the operating mode is active (see operating mode quit). A position set, for example, can only be executed, when this has taken place.

Value	Operating mode
0	No external operating mode selected
1	Ext/AE is selected
2	Ext/AF is selected
3	Ext is selected

Start:

- Starting a positioning procedure in all external operating modes and for "teach-in" via the PLC.
- Operating modes Ext and Ext/AE:
  The currently selected NC set is started by a 0 -> 1 change of the start bit. The "start" bit must be set to the value 1 at least, until it was acknowledged by the output "set executed" or "start quit".
- Operating mode Ext/AF:
  The selected NC set is started by a 0 -> 1 change of the start bit. The programmed subsets are executed, while the start bit remains set to 1.

teach-in:

- If the teach-in bit is set from 0 -> 1 in the operating mode external, the current actual value of the axis is accepted as the position set value for the position set determined by the set no. with a 0 -> 1 change of the "start" bit.
  The "start" bit must be set to 1 for at least 50ms.

Enable mode:

- The input determines how the 35 PO 90 reacts to a change at the enable initiator input.
  Description of the enable modes: see section 10.1.5.6, Function of the initiator signals.
- Value range:
  0B to 11B (0 - 3)

Value	Operating mode
0	Enable mode 1 active
1	Enable mode 2 active
2	Enable mode 3 active
3	Enable mode 1 active

UP segment:
- Selection of the user program segment. 4 program segments are available to the user for NC programs in the non-volatile memory (EEROM).
- All the set numbers mentioned in the section: set types are available within each UP segment.
- The user decides with the selection, whether the MDS and the flag sets of the newly selected UP segment should be activated (UP segment selection > 128) or not (UP < 128).
- A time delay occurs when activating the MDS for the reaction to the first "start" signal of a set after the UP segment switchover.

- Value range:
  0B to 011111111B (0 to 255)

Value	UP segment	
0 to 3	UP segment 1 to 4 are active	MDS and flag set are not activated
4 to 14	35 PO 90 serial unit: UP segment 1 is active	
	Only with 32k x 8 RAM assembly! accordingly: UP segments 5 to 15 are active	
15 to 127	UP segment 1 is active	
128 to 131	UP segment 1 to 4 are active	MDS and flag set are activated
132 to 142	35 PO 90 serial unit: UP segment 1 is active	MDS and flag set are not activated
	Only with 32k x 8 RAM assembly! accordingly: UP segments 5 to 15 are active	MDS and flag set are activated
143 to 255	UP segment 1 is active	MDS and flag set are not activated

Override selection:
- For the activation of the internal or external speed correction value (override).

- Value range:
  0B to 11111111B (0 to 255)

Value	Operating mode
0	No override is active
1	External override is active
2	Internal override for N136 is active
3	Internal override for N137 is active
4 to 255	No override is active

Override value:
- Value of the external override

- Value range:
  0B to 11111111B (0 to 255)
  Internal limit to 120

Length correction selection:
- For activating the internal or the external length correction value as well as the scale factor. The selection of the length correction as well as the external length correction value, if necessary, must be active at the "start" of a set already.

- Value range:
  0B to 11111111B (0 to 255)

Value	Operating mode
0	No length correction value is active
1	External length correction value is active
2	Internal length correction value for N138 is active
3	Internal length correction value for N139 is active
4	Scale factor for N140 is active
5 to 255	No length correction value is active

Length correction value:
- Value of the external length correction.

- Value range:
  80 00 00 01H to 7F FF FF FFH (B compliment)
  Internal limit to -9999999 to +9999999

Reserve I word 1:
Reserved

Reserve I word 2:
Reserved

Deleting the error number:
= 1 -> the error number (see ABB Procontic T300 output "error number") is deleted (set to 0).
= 0 -> the error number is not deleted. If the input is set permanently, no error numbers are displayed in the output "error number".

Reserve I bit 1:
Reserved

10.1.5.5.2 MPST bus outputs

T300 Address 2000:	Bit number	Meaning
0XX21H	0	Axis is ready for operation
	1	Limit position +
	2	Limit position -
	3	Following error
	4	Position reached
	5	Sentence executed
	6	Start quit
	7	Loop executed
0XX22H	0	Dwell time
	1 to 2	Operating modes quit (0 to 3)
	3 to 7	Free
0XX23H	0 to 7	Watchdog byte
0XX24H	0 to 7	Machine function bit 0 ... 7
0XX25H	0 to 3	Machine function bit 8 to 11 (0H to 3E7H)
	4	Free
	5	Flag 1
	6	Flag 2
	7	Flag 3
0XX26H	0 to 7	8 Section flags Bit 0 to 7 -> sections Flag 1 to 8
0XX27H	0 to 7	Position actual value,lowest byte
0XX28H	0 to 7	Position actual value,low-mid byte
0XX29H	0 to 7	Position actual value,high-mid byte
0XX2AH	0 to 7	Position actual value,highest byte 32 bit dual in the binary compliment
0XX2BH	0 to 7	Error number (LB)
0XX2CH	0 to 7	Error number (HB)
0XX2DH	0 to 7	Reserve word 1 (LB)
0XX2EH	0 to 7	Reserve word 1 (HB)
0XX2FH	0	Reserve bit 1
	1	Reserve bit 2
	2 to 7	Free

Axis ready:
- is set to 1 after switching on the supply voltage, if a 35 PO 90 internal test was carried out with a positive result.
- is set to 0, as long as the enable initiator has the value 0.
- shows that the axis is ready for an external positioning operation. It is set to 0 in the operating modes Ext, Ext/AE and Ext/AF, if a positioning operation was interrupted with, e.g., the "STOP" key on the operating unit or by "enable" 1 -> 0 change and also if an operating mode was selected with an operating unit.
- is set to 0 during a DNC transfer.

Limit position +:
- is set to 1, while the limit position recorder (positive drive direction) is approached.
- is otherwise set to 0.

Limit position -:
- is set to 1, while the limit position recorder (negative drive direction) is approached.
- is otherwise set to 0.

Following error:
- is set to 0 after switching on the supply voltage.
- is set to 1, if the maximum following error determined in the MDS (MDS P10) (difference between the position actual value and the position set value) is exceeded. It is set to 0, if the maximum following error is not reached.

Position reached:
- is set to 1, while the axis is located in the target window (MDS P19).
- is otherwise set to 0.

set executed:
- is set to 1 after switching on the supply voltage.
- is set to 0, if the set was started and set to 1 again, if a set is executed (internal reference input variable setting is finished and the axis is in the target window, or after a positioning abortion with enable = 0, if the enable mode 2 or 3 is selected.

Start quit:
- is set to 0 after switching on the supply voltage.
- is set to 1, if a set was started ("set executed" 1 -> 0 change).
- is not set to 0 again by the 35 PO 90, if the set is executed.
- is set to 0 again (acknowledged) by the PLC (PLC block POKO).
- The user can detect the execution of short sets (set execution time < PLC cycle time) with the output "start quit", even if the output "set executed" is set to 1 again after the "start" of the short set, before the PLC has detected "set executed" = 0.
- The output "start quit" should therefore always be evaluated in addition to "set executed".

Loop executed:
- is set to 1 after switching on the supply voltage.
- is set to 0, if a loop set was started. It is set to 1 again, if the loop is processed or after a positioning abortion with enable initiator 1 -> 0, if the enable mode 2 or 3 is selected.

Dwell time:
- is set to 1 after switching on the supply voltage.
- is set to 0 after the start of the set and set to 1 again after the execution of a set and after the programmed dwell time is over or after a positioning abortion with enable initiator 1 -> 0, if the enable mode 2 or 3 is selected.

Operating modes:
- Acknowledgement of the currently active operating mode:
  is set to 0 after switching on the supply voltage.

Value	Operating mode
0	No external operating mode is active
1	Ext/AE is active
2	Ext/AF is active
3	Ext is active

Watchdog byte:
- is set to 1 after switching on the supply voltage.
  Is used by the PLC block POKO to detect a cold start of the 35 PO 90.

Machine function:
- All the machine function bits are set to 0 after switching on the supply voltage.
- The machine function is output in a binary way.
- Positive sign of the machine function:
  - The machine function of a set is output after the set processing with "set executed".
- Negative sign of the machine function:
  - The machine function of a set is output with the start of the set.
- If the machine function value was entered as 1,000, no machine function is output in this set.
- The output of a machine function overwrites the previous one.
- Value range:
  0H to 03E7H (0 to 999)

FLAG 1:
- The flag output is output depending on the position set value stored in the program (set N144) and the axis position actual value. Observe the note in section 10.1.5.5.1 (section: UP segment) after switching over the UP segment.
- Positive flag position value:
  - if the axis drives over a flag position in the positive direction, the corresponding flag is set. If the axis drives over a flag position in the negative direction, the corresponding flag is reset.
- Negative flag position value:
  - if the axis drives over a flag position in the negative direction, the corresponding flag is set. If the axis drives over a flag position in the positive direction, the corresponding flag is reset.

FLAG 2:
- Flag position 2 (N145): For the description, see FLAG 1.

FLAG 3:
- Flag position 3 (N146): For the description, see FLAG 1.

8 section flags:
- are set to 1 after switching on the supply voltage.
- All the section flags are set to 0 after the start of the position set.
- A section flag is set to 1 again after 1/8 of the drive path of the set.

  1/8 -> Section flag 1 =1
  2/8 -> Section flag 1 and 2 =1
  3/8 -> Section flag 1 to 3 = 1
  4/8 -> Section flag 1 to 4 = 1
  5/8 -> Section flag 1 to 5 = 1
  6/8 -> Section flag 1 to 6 = 1
  7/8 -> Section flag 1 to 7 = 1
  8/8 -> Section flag 1 to 8 = 1

  All the section flags are set to 0 after a positioning abortion with the enable initiator and to 1 again in the enable mode 2 or 3.

Position actual value:
- Position actual value of the axis in the absolute measurement referring to the reference point.
- Value range:
  80 00 00 01H - 7F FF FF FFH (B compliment)

Error number:
- Display of the 35 PO 90 error numbers:
  - Set to 0 after switching on the supply voltage
  - The output of an error number overwrites the previous one
  - Deleting (set to 0) the output, see section 10.1.5.5.1 (section: "Deleting the error number"
  - The error number 0FFFFH means: the 35 PO 90 could not identify an error message.

Reserve 0 word 1:
- Reserved

Reserve 0 bit 1:
- Reserved

Reserve 0 bit 2:
- Reserved

10.1.5.5.3 Display of the MPST bus in-/outputs

The current status of the MPST bus in-/outputs and of the initiators (e.g., when starting the device) can be displayed by means of the operating unit.

An operating mode (except for "manual entering of data") must be selected here.

E00:

7	6	5	4	3	2	1	0
			Reserve input	Ref. point init.	Neg. limit posit. init.	Pos. limit posit. init.	Release init.

E01 ... E15:
MPST bus inputs display 0XX01H to 0XX0FH (see MPST inputs overview).

A01 ... A15:
MPST bus outputs display 0XX21H to 0XX2FH (see MPST outputs overview).

10.1.5.6 Function of the initiator signals

Limit position initiators (closed-circuit current principle):
- If a 0V signal is on one of the limit position initiator inputs, the 35 PO 90 brakes with the "brake mode in case of a failure" (MDS P08).
- The "move to limit position" LED lights up.
- The corresponding error message appears on the display of the operating unit.
- If the limit positions are not required, the limit position initiator inputs are to be switched with +24 V (Up). The 24 V (Up) required for this should be taken from X4.8.
- Leaving the limit positions is only possible in the operating modes "move to reference point" and "manual control" as well as in the operating mode "Ext" with reference point drive and manual control.

Reference point initiator (working current principle):
- If a +24 V level is put on the reference point initiator input during a reference point drive, the 35 PO 90 sets its internal position actual value counters to zero.
- The LED "move to reference pointed" lights up.
- A software routine ensures that the reference point is always approached from the same direction (corresponding to the reference point set no.), independent of the position of the axis at the "start" of the "move to reference point". A prerequisite here is that the limit position initiators are active.
- Attention is to be paid to the fact, that the reference cam has at least the length of the path to dampen the reference point initiator. The path is the distance covered by the axis during a position encoder rotation (caused by the encoder zero track pulse).

Enable initiator:
If the enable initiator input is not switched, the start of a positioning procedure is not possible. The correspond-

ing error message appears on the display of the operating unit (ERROR 20).

3 enable modes can be selected via the MPST bus input "enable mode".

Enable mode 1:
- If the enable initiator is set to zero (1 -> 0 change), while the axis is moving, the axis stops after the "brake mode in case of a failure" programmed in the "MDS" P08. The interrupted set can be continued with a renewed "start" after switching on the enable initiator again.
- If the enable initiator is set to 0 (1 -> 0 change), while the output "set executed is 1 (positioning procedure completed) and the "brake mode in case of a failure" is set to 1, the current position actual value is then accepted as the new position set value.

Enable mode 2:
- As for enable mode 1, except for the fact that the partly processed set is interrupted after the interruption of the positioning procedure with a 1 -> 0 change of the enable initiator.
- The following MPST bus outputs are reset with the 1 -> 0 change of the enable initiator to its starting position (after supply voltage ON):

'Position reached'	= 1
'Target window'	= 1
'Set executed' = 1	
'Loop executed'	= 1
'Dwell time'	= 1
'8 section flags'	= 0FFH
'Following error'	= 0

The current position actual value is accepted as the new position set value. A newly selected set is started after switching on the enable initiator again and a renewed "start".

Enable mode 3:
- As for enable mode 2, except for the fact that the position control of the 35 PO 90 is not active while the enable initiator has the value 0. The 35 PO 90 internal position actual value counters remain active.

10.1.5.7 Software versions

The currently available software versions include the following:

Unit rubric: R0101/B
SW versions: V1.2

Changes:
V1.2: first version

Note: The software version number can be prompted in the operating mode "manual entering of data" by recalling the set N999.

10.1.5.8 Interface protocols

General:
The exchange of data between the 35 PO 90 and the 35 AB 50 operating unit or a PC is executed in a half duplex way.

The 35 PO 90 has 5 types of telegrams at its disposal:
- Reset telegram
- Display telegrams
- LED telegrams
- Key telegrams
- DNC telegrams

The 35 AB 50 operating unit informs the 35 PO 90 of its readiness using the reset telegram after switching on the supply voltage.

Display telegrams are sent by the 35 PO 90 and output by the 35 AB 50 operating unit on the alpha-numerical display.

LED telegrams serve the 35 PO 90 to switch on or off the LED of the operating keys of the 35 AB 50 operating unit.

Key telegrams are sent by the 35 AB 50 operating unit. They inform the 35 PO 90, that a key on an operating unit has been pressed. The user can simulate the operating unit from a PC by means of key telegrams.

DNC telegrams serve the user or the 935 AM 50 PC software to transmit NC sets.

Setting the serial interface:

RS422/RS232:	adjustable via X1003 depending on the requirement (see section "Settings")
Data format:	8 data bits + parity even
Character set:	AECII characters
Baud rate:	2400 baud

Note:
The initiator plug (INI) must also be plugged in all the time for the DNC operation. (X4, PIN 6 must be on +24 V (Up))

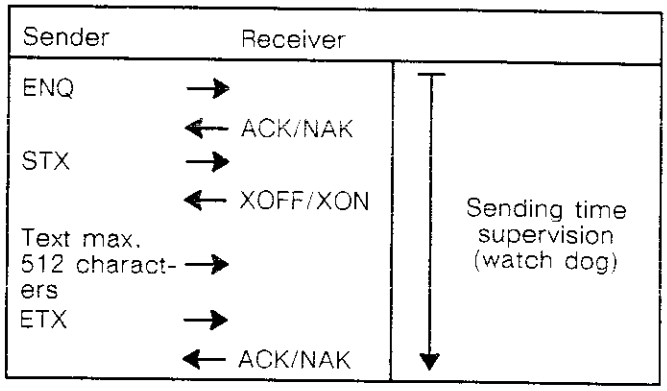
Control characters:

ASCII value	Characters	Meaning
02H	STX	Telegram start
03H	ETX	Telegram end
05H	ENQ	Request to receive
06H	ACK	Ready to receive and positive acceptance of receipt
0AH	LF	Deletes display, cursor remains in its position
0DH	CR	Cursor is positioned on the first character in the display
11H	XON	Continuation of transfer after an interruption with XOFF
13H	XOFF	Interruption of transfer
15H	NAK	Not ready to receive and negative acceptance of receipt
18H	CAN	Cancels a not yet complete control function on the display
1AH	SUB	is interpreted as CAN
1BH	ESC	Initiates a control function on the display
7FH	DEL	Rub out

General telegram frame:

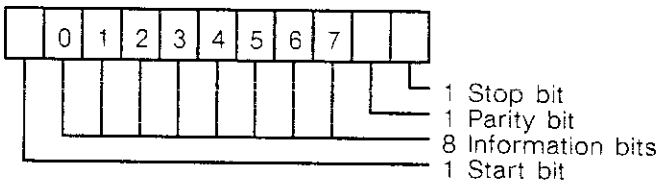
The following telegram frame is to be observed to communicate with the 35 PO 90:

- The sending station enquires whether the other station can receive, by sending ENQ cyclically (in the control time rhythm) and starts a sending time of the control timer at the same time.
- If the other station is ready to receive, it acknowledges the enquiry with ACK. If it is not ready to receive, it acknowledges the enquiry with NAK. The sender must start the telegram transmission from the start in the case of a negative acknowledgement.
- The sending station transmits a telegram, which starts with STX, contains a maximum of 512 text characters and ends with ETX after a positive acknowledgement of the enquiry.
- The receiving station can interrupt the transmission procedure with XOFF during the text transmission phase. The receiving station must be able to accept at least 8 more characters after receiving XOFF. The receiving station enables the transmission again with XON.
- The sending station waits for a positive acknowledgement from the receiving station with ACK after the transmission of the characters ETX.
- If the sending station receives this acknowledgement during the control time period, the transmission of the telegram is completed.
- If the sending station does not receive this acknowledgement during the control time period or it receives a negative acknowledgement with NAK, the telegram has not been transmitted and the sending station must begin the transmission from the start.



General telegram format:

The individual characters have the following structure



Reset telegram:

The operating unit informs the 35 PO 90 of its readiness by means of the reset telegram after switching on the 35 AB 50 supply voltage.

Telegram format:

STX TFF ETX

Reset telegram code

Display telegrams:
The following telegram serves the display of the operating unit 35 AB 50.

Telegram format:

STX max. 512 characters of text ETX

Text to be displayed

The character scope, which can be shown, includes the ASCII characters 20H to 5FH.

The first text character of a display diagram may not be a telegram code (T, I, C, D).

The following AECII characters can be part of a text of a display telegram. They affect the display. They are not displayed.

- LF deletes the display; the cursor remains in the current position.
- CR positions the cursor on the first character in the display.
- DEL (Rub out) positions the cursor to the left by one character and deletes the character.

Other display effects can be caused by means of escape control sequences:

- ESC | Pn C Moving the cursor to the right by n characters (Default = 1).
- ESC | Pn D Moving the cursor to the left by n characters (Default = 1).
- ES Initiating a power-up reset of the display controller.
- ESC # 8 makes all the display segments bright; the cursor position is maintained. An ESC control sequence, which has not yet been completely transmitted, can be interrupted with the AECII characters CAN or SUB.

LED telegrams:
A LED telegram informs the operating unit 35 AB 50, that a LED (in an operating mode key) is to be switched on or off.

Telegram format:

STX I LED no. LED status ETX

LED status after the transmission 0 -> OFF, 1 -> ON
LED no. acc. to the keyboard layout of
LED telegram code

If a LED no. is not known to the operating unit, the telegram is ignored without a return message.

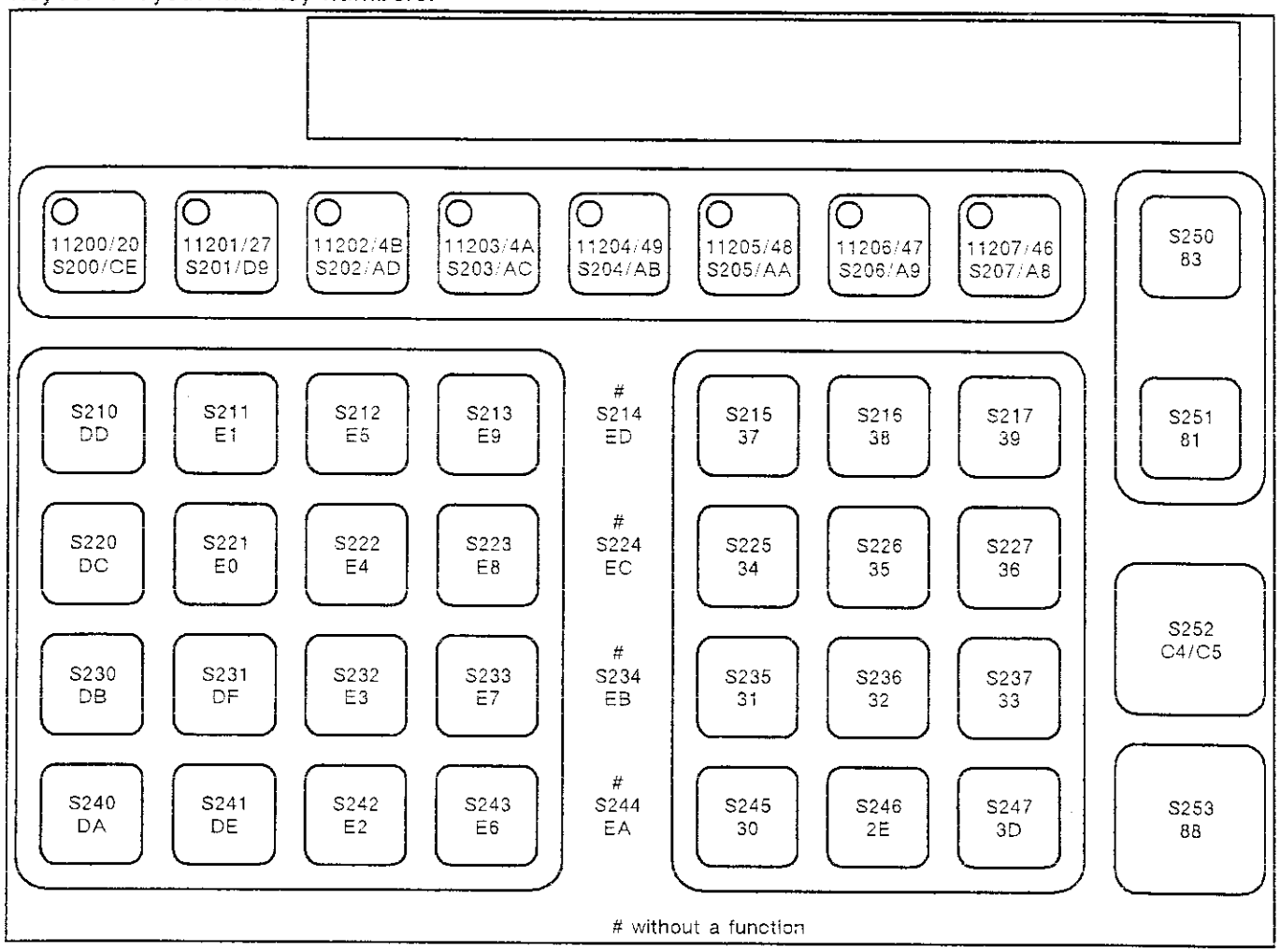
Key telegrams:
Key telegrams inform the 35 PO 90, that keys on the 35 AB 50 operating units have been pressed.

Telegram format:

STX T key no. ETX

Key code
Key telegram code

Keyboard layout with key numbers:



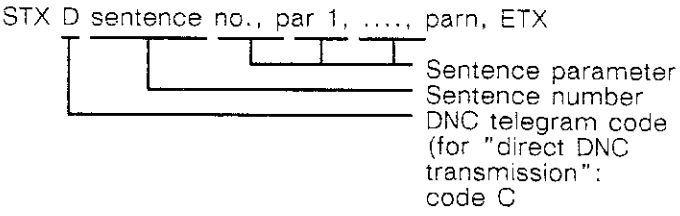
DNC telegrams:
The PLC causes the 35 PO 90 to execute a DNC function with a DNC telegram. The 35 PO 90 executes the DNC function and answers with a CNC answer telegram, if necessary.

The transmission of DNC telegrams is only allowed when a axis stands still (exception: reading the position actual value). The 35 PO 90 does not allow any other telegrams during the DNC telegram processing.

If an error is detected during the interpretation or the processing of a DNC telegram, the 35 PO 90 outputs an ERROR message.

The 35 PO 90 allows other telegrams (from the PC) only after accepting this ERROR message by the PC.

Telegram format for the CNC telegram between the PC and the 35 PO 90:



The sentence number decides which CNC function is executed.

A comma must be transmitted after the set number and after every parameter.

If a programmed parameter is not to be changed, it does not have to be transmitted. If this is the case, two commas one after the other are transmitted.

Only one comma must be put after the last parameter to be changed. Further commas are not to be changed.

Programming NC sets:
All the NC sets of the 35 PO 90 can be programmed (altered) by means of the DNC telegram.

To this end, a CNC telegram together with the corresponding set number and the parameters to be altered is transmitted to the 35 PO 90.

Set number: 0...190

Example, position set:

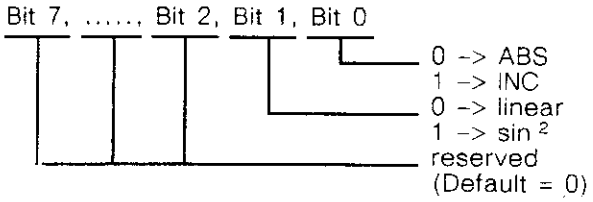
Set number:	20
INC/ABS:	INC (see code byte)
Position:	+ 1234567 INC/(1/12.5) s
FEED:	is not to be changed
DWELL:	2.0 s
MFCT:	123
N+1:	is not to be changed

STX, 1, +1234567,,20,123, ETX
see code byte

Coded telegram:
02 44 30 32 30 2C 31 2C ... 2C 03

Code byte:
Each position set includes a code byte.

The code byte includes the information, whether the position set value of the set is to be approached in an incremental or absolute way and whether it is to be moved with linear or sin^2 ramps.



RAM mode:
If the user program must be altered very fast or frequently in the DNC mode, the user can select the RAM mode.

The RAM mode is allowed for position sets and for the machine data set.

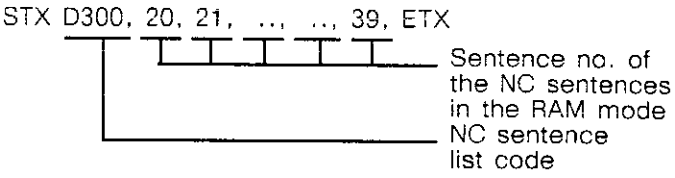
If the RAM mode is selected for an NC set, it is stored in the working memory (RAM) of the 35 PO 90 after the transmission in the DNC mode and not programmed into the non-volatile EEPROM. The NC set with the same set number in the EEPROM is ignored and no longer altered, after the RAM mode was selected for this set. The user selects the RAM mode while transmitting an NC set list to the 35 PO 90. All the NC sets not listed in the NC set list are processed as before (from the EEPROM).

The 35 PO 90 NC program can be mixed from sets for which the RAM mode was selected, and from sets, for which the RAM mode was not selected. The RAM mode has no effect on the operating modes like automatic single set mode and automatic subset mode.

The NC set list and all the NC sets stored in the RAM are deleted after switching off the 35 PO 90 supply voltage. The NC set list may include a maximum of 80 NC set numbers. A maximum of 20 NC set numbers per DNC telegram may be transmitted. If the NC set list is longer than 80 set numbers, the NC set numbers, which were first transmitted, are overwritten.

Entering the set number 255 in the NC set list indicates the end of the NC set list for the 35 PO 90.

Example, RAM mode:
- transmitting the NC set list (in 2 parts here).



STX D300, 40, 41, .., 58, 190, ETX

- transmitting a complete position set (see also NC set programming).

STX D20,1, +1234567, 5000, 20, 123, 21, ETX

- altering a set parameter (here: position set value) of the position set stored in the RAM.

STX D20,, +2345678, ETX

Reading out the NC set:
The 35 PO 90 is forced to output all the NC sets from N0 to N190 of the selected user program segment with the following telegram.

The end of the NC set output is coded by the 35 PO 90 by a telegram with the contents "D222".

Telegram to be transmitted:

STX D222, ETX

Reading out the code for the NC set

The 35 PO 90 is forced to output a single NC set of the selected user program segment with the following telegram.

The end of the NC set output is coded by the 35 PO 90 by a telegram with the contents D222.

Telegram to be transmitted:

STX D222, 20, ETX

Set no., the output of which is requested

Reading out the code for the NC set

Direct DNC transmission:
A position set can be transmitted (also in parts) and started immediately (without the PLC "start" signal) by means of the following DNC telegram. Reference point drive sets can also be transmitted and started in the "direct DNC transmission".

Telegram to be transferred:

STX C20, , +1234567, ETX

Position set value

Set no. (16 to 127 poss.)

Direct DNC transmission code

Function:
- The position set value and other parameters are stored in the EEPROM (RAM).
- The NC set is executed.
- Another DNC telegram is allowed after the acceptance of the DNC answer telegram (see below) by the PC. I.e., no transmission of telegrams to the 35 PO 90 is possible during the positioning procedure.
- Errors occurring during the positioning procedure are handed on to the PC as ERROR messages.
- A position set interrupted by, e.g., the enable initiator cannot be continued at the same position (a renewed selection by "direct DNC" causes a renewed execution of the set).

Acknowledgement of the 35 PO 90 by executing the position or reference point drive set:

STX C020 ETX

Set no. of the executed position sentence

Direct DNC transfer code

Reading out the position actual value by DNC:
The current position value of the 35 PO 90 refering to the machine reference point can be read out by means of the following DNC telegram:

STX D333, ETX

Reading out the code for the position actual value

Example for the 35 PO 90 answer telegram:

STX 1234567ETX

Current position value

STX 0ETX

Current position value

STX- 1ETX

Current position value

10.1.5.9 Error messages

No.	Error
4	Subset does not exist
5	Set type does not exist
6	Loop depth is exceeded
7	Position set is required
8	Position set depth is larger than 2 (with "flying overdrive" set
9	Dummy initialisation is active. The axis cannot be transversed. A new start is only possible after interrupting the voltage or a reset
10	Loop interrupt; subset is missing
11	Selection of a manual control set in this operating mode is not possible
15	Check sum in the 35 PO 90 program memory is incorrect (system error)
20	Enable is missing
21	Positive limit position is reached
22	Negative position is reached
23	Both limit positions are reached at the same time
24	Reference measurement counter overflow
25	Different directions are selected (with the "flying overdrive" set
30	Selected jog direction is not possible
31	Positive and negative SW limit switches are reached
32	"Positive" SW limit switch was reached
33	"Negative" SW limit switch was reached
40	The check sum in EEPROM is not correct
41	EEPROM cannot be programmed
50	Brake ramp limit is reached (brake ramp is too large or Fmax too small)
51	Brake ramp is not in the range (time range: 10 ms to 10,000 ms)
52	Start-up ramp is not in the range (time range: 10 ms to 10,000 ms)
53	Start-up ramp limit was reached (Umax is too low or the acceleration time was too large)
63	KV factor is negative
64	Acceleration ramp is negative
65	Brake ramp is negative
66	Target window is negative
67	Brake mode is negative
68	Drift constant is negative
69	Sensor evalution is not 2 or 4
70	Upper limit value is negative
71	Lower limit value is negative
72	Position control differential is negative
73	Devisor is negative
74	Sign of the maximum speed is negative
75	Sign of the maximum following error is negative
76	Brake mode is not 1, 2 or 3
77	Acceleration and brake ramp generation is not clear
78	Sign of the transmission factor is not positive
79	Selection of the decimal places is not in the limits 0 - n point - 3
102	On checking the parameter range limits, it was found that they were exceeded
103	There is no operating mode change possible at the moment
104	Operating modes selection is missing

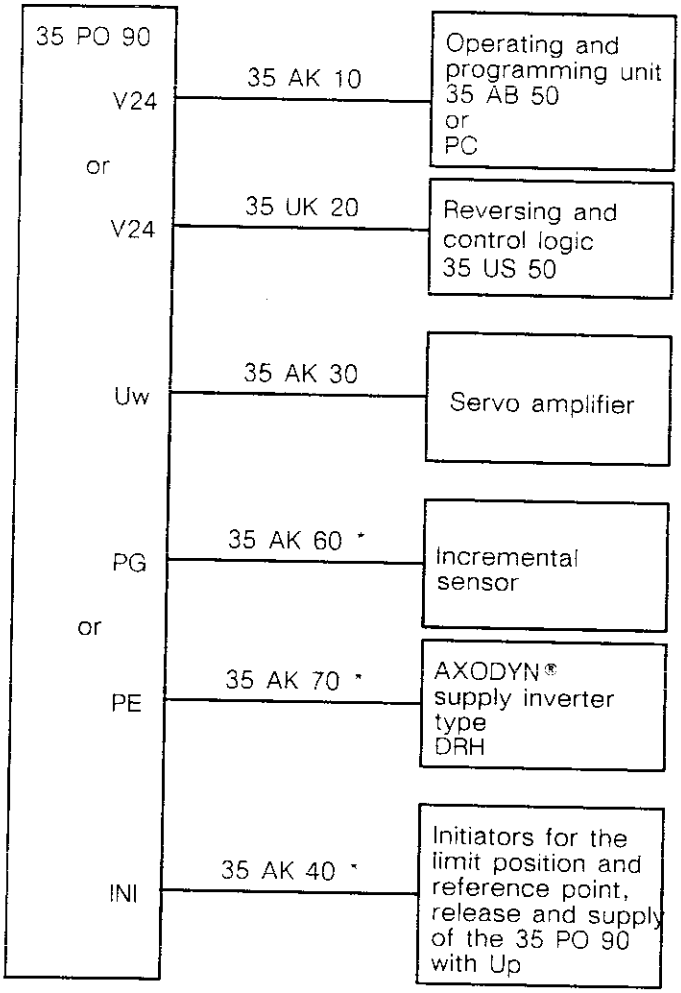
No.	Error
105	A set was not selected
106	The selected set is not implemented
107	Teach in is not possible, since the selected sentence does not have a set value
108	The selected function is not meaningful at the moment
109	The parameter key is only meaningful together with the machine data
110	The selected set contains no set value
111	The selected set contains no machine function
112	The selected set contains no dwell time
113	The selected set contains no feed
114	The selected set contains no zero point
115	The set contains no parameters
116	The set contains no loop set
117	The traversing direction cannot be changed at the moment
118	The decimal key has no function at now
120	The machine parameter with this no. does not exist
125	The selected set does not have a possible subset
126	The selected function key does not have a meaning
127	The start key is meaningless in this op. mode
128	The decimal keys are meaningless now
129	Selection of a set, which is not released in the automatic mode
130	Selection of a set, which is not released for the PLC
131	Selection of a set during the set processing is not possible
202	The start signal is not allowed at the moment
203	The set selected by the PLC is not allowed in this operating mode
204	Teach in request, although the set is still being processed
205	Teach in request, although the ready signal = 0
206	Teach in request, although the ready signal was removed in the meantime
207	The selected set is not capable of teach-in

DNC error messages:

300-380	As for the errors 00 to 80
393	Invalid set no. for direct DNC transmission
394	Display buffer is not empty (system error)
395	The set is not enabled
396	Limits exceeded, e.g. forbiden parameters
397	No comma after this set
398	The position set is not yet completely processed (no start is possible)
399	Incorrect operating mode is selected

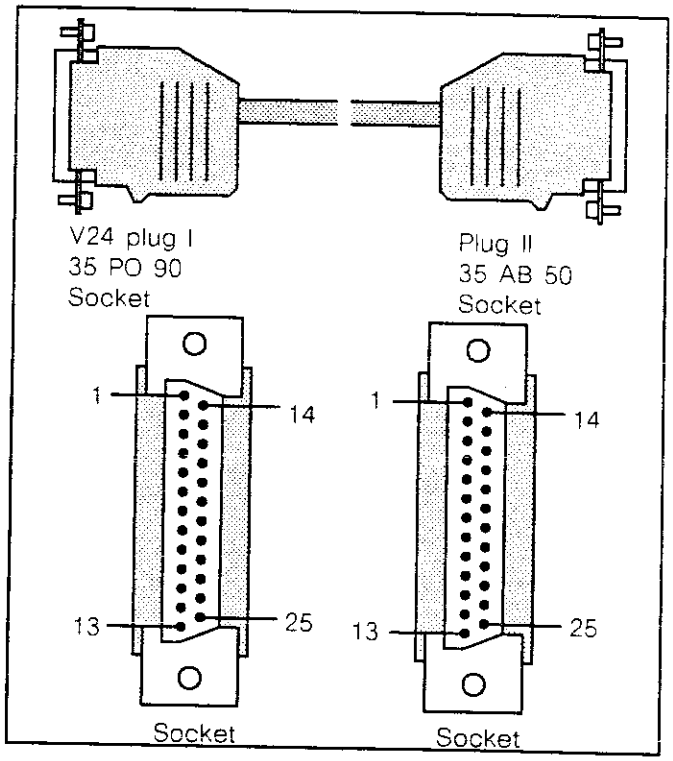
10.1.6 Application instructions

10.1.6.1 System cables



* Please observe the earthing and wiring concept!

Dialog cable 35 AK 10:

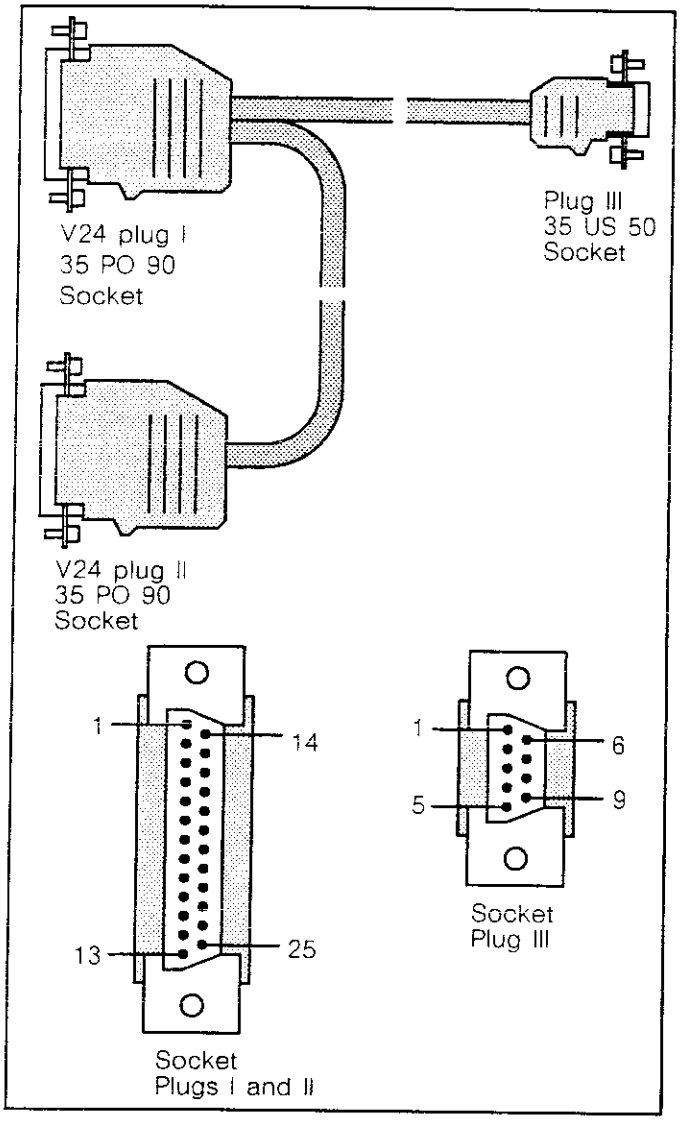


Plug I for 35 PO 90	Plug II for 35 AB 50 or PC	Signal	Cable colour
1	1	Screen	
2	3	$\overline{\text{TXD}}$ ($\overline{\text{RXD}}$)	white
3	2	$\overline{\text{RXD}}$ ($\overline{\text{TXD}}$)	brown
4	4	Jumper 4/5	
5	5		
6	6	Jumper according to 20	
7	7	Signal GND	green
9	9	0 V	red
10	10	+ 24 V	grey
18	21	TXD (RXD)	pink
20	20	Jumper according to 6	
21	18	RXD (TXD)	blue

The transmission speed (baud rate) between the 35 PO 90 and the operating and 35 AB 50 programming unit or the personal computer amounts to 2400 baud.

Do not insert or unplug the plug with the voltage switched on, since the 35 PO 90 unit can be destroyed by short-circuits with the metallic plug edge of the cable 35 AK 10. If the 35 AB 50 operating and programming unit is not installed in a stationary way, the 35 AK 10 system cable is to be connected permanently to the operating unit.

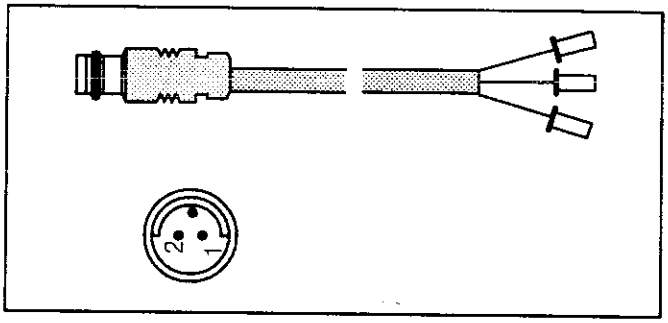
Dialog cable 35 UK 20:



Plug III 35 PO 90 2nd unit Pin	Signal	Plug I 35 PO 90 1st unit Pin	Signal	Plug III 35 US 50 Pin	Signal	Cable colour
				1	PGND Screen	
		10	RxD	2	1 TxD	yellow
		3	/RxD	3	1 /TxD	green
		9	TxD	4	1 RxD	grey
		2	/TxD	5	1 /RxD	pink
10	RxD	15	*	6	2 TxD	brown
3	/RxD	11	*	7	2 /TxD	white
9	TxD	13	*	8	2 RxD	red
2	/TxD	8	*	9	2 /RxD	blue

* These plug connections only serve as solder tags for interconnecting the signals between plug III and plug II. These connections are not assigned in the V24 interface of the 35 PO 90 (NC).

Speed set value cable 35 AK 30:



Plug connection	Cable colour	Signal
1	white	Uw = +/– 10 V
2	brown	UWN = 0 V
–	green	Screen

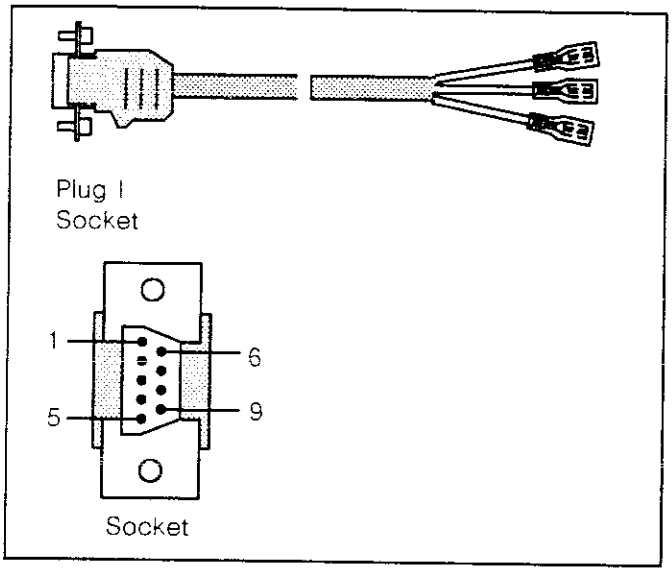
The 35 UK 20 cable connects two units of the 35 PO 90 type with the 35 US 50 electronic reversing and control logic.

The unit 35 US 50 offers the possibility of operating and programming a maximum of six 35 PO 90 units with one 35 AB 50 operating unit or a PC.

The unit description for the 35 US 50 can be found in the AXUMERIK® m system description (order number GATS 1320 01 R1001).

Caution:
The plug may not be inserted or unplugged with the voltage switched on.

Initiator cable 35 AK 40:



Plug connection	Cable colour	Support sleeve code	Signal
1	red	11	0 V
2	white	1	Release
3	brown	2	+ limit position
4	green	3	– limit position
5	yellow	4	Reference point
6			Reserved input
7			Jumpers 6, 7 and 8
8			+ 24 V–
9			+ 24 V–
–	pink	00	free
–	blue	10	free
–	grey	5	free

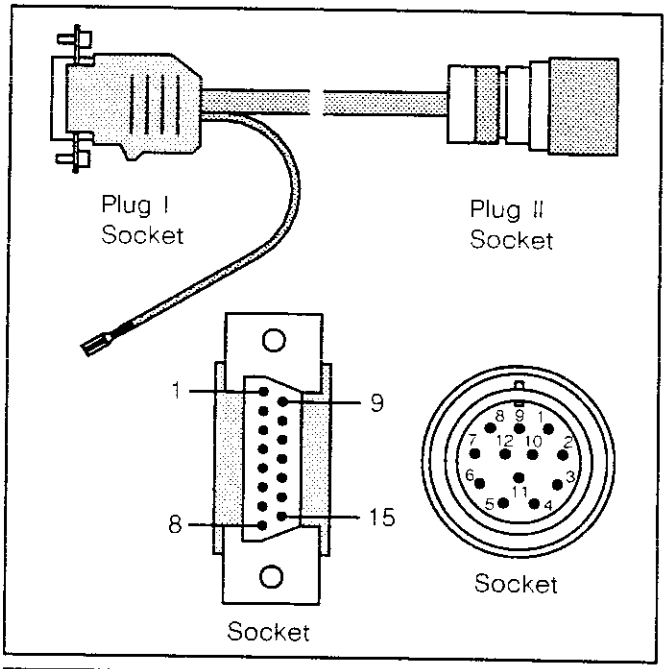
Do not insert or unplug the plugs with the voltage switched on.

The initiator input plug serves to connect the initiators for the 35 PO 90 and to supply the 35 PO 90 with the process voltage (Up) (for the supply of the operating unit, reserved input E.....). The connection of Up and 0 V (Up) is required in any case to operate the 35 PO 90.

If the 35 AK 40 system cable is to be connected to the 35 PO 90, it must be converted as follows:
- Plug connection PIN 1:
  Cover the cable with the pink colour as well.
- Plug connection PIN 8:
  Cover the cable with the grey colour.
- Plug connection PIN 9:
  Cover the cable with the blue colour.
- The jumper between the plugs PIN 6, 7 and 8 is maintained.
  -> Connection Up to cables with the grey and blue colours.
  -> Connection 0V (Up) to cables with the red and pink colours.

Description of the signals:
- See the function of the initiator signals, section 10.1.5.6.

Position encoder cable 35 AK 60 for the incremental encoder:

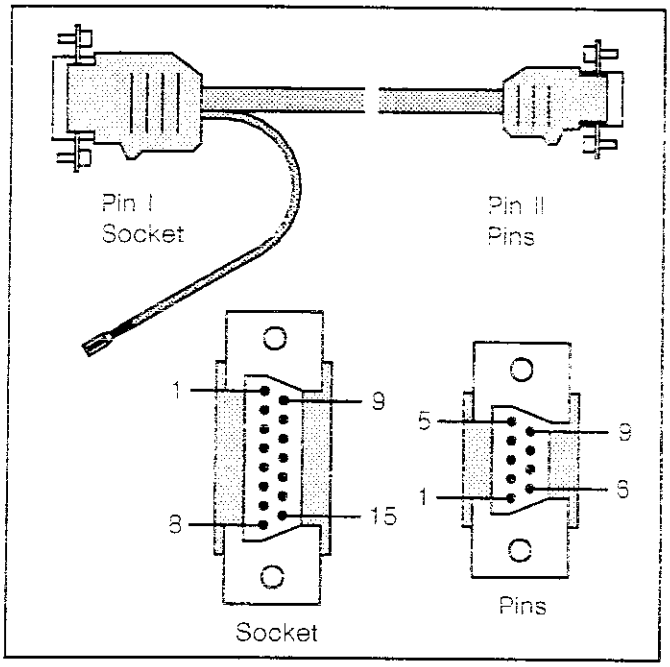


Plug II for the encoder	Plug I for 35 PO 90	Cable colour	Signal
	guided to the outside		Screen
5	8	pink	Track A
6	9	red-blue	Track /A
8	10	violet	Track B
1	11	grey-pink	Track /B
3	13	black	Zero track C
4	12	red	Zero track /C
	14	blue	Reserve
12	2	white	+5V/+15V/ext.*
2	7	grey	+5V/+15V/ext.*
10	3	brown	0 V*
11	4	green	0 V*
	5	yellow	0 V*

* Encoder supply, see settings, chapter 10.1.4.5

Do not insert or unplug the plugs with the voltage switched on.

Position encoder cable 35 AK 70 for AXODYN® inverter, construction DRH:



Pin II for AXODYN®	Pin I for 35 PO 90	Cable colour	Signal
4	guided to the outside		Screen
6	8	pink	Track A
1	9	red-blue	Track /A
7	10	violet	Track B
2	11	grey-pink	Track /B
8	13	black	Zero track C
3	12	red	Zero track /C

Do not insert or unplug the plugs with the voltage switched on.

Encoder interface DV3001:
The position encoder connection can be operated optionally with the buffer stage DV3001 (ABB driver technology).

The connection is carried out according to the following overview:

Plugs on the 35 PO 90	Plugs for the PE DV 3001	Signal
guided to the outside	4	Screen
6	6	Track A
9	1	Track /A
10	7	Track B
11	2	Track /B
13	8	Zero track C
12	3	Zero track /C
2	5	+5 V
4	9	0 V

Not in stock.

10.1.6.2 Earthing, wiring and screening concept

Compare the earthing and wiring concept for ABB Procontic T300 (volume 5, Configuration).

Structure and line guidance:

- A division into the power section and the control section is to be carried out when designing the switch cabinet.
- The 24V supply lines for the electronics and the interface cables (position encoder, operating unit, set value and initiator cables) may not be put into one cable channel together with switched lines, which supply inductive consumers (contactors, brakes, solenoid valves, motors, etc.) in order to keep the interference voltages as low as possible.
- All the contactss, brakes and solenoid valves are to be connected with interference suppressors (RC elements, free wheeling diodes etc.).
- A PE busbar is to be installed as close as possible to the units in order to achieve a good equipotential bonding between the separate components. The PE busbar should be installed, so that the earth lines (from all the units to the PE) are as short as possible (0.5 m - 1 m).
- The earth lines of the separate units should have a cross-section of 6 mm^2.

+24V electronic power supply unit and 0V busbar:

- A separate electronic power supply unit is to be provided for the 24 V supply (Up) of the 35 PO 90 and the 35 AB 50 as well as the PLC I/O modules. Consumers like contactors, brakes, solenoid valves, etc., may not be connected to this power supply unit.
- The 0 V point of the separate electronic power supply unit is guided to a 0 V busbar. The 0 V connections from the 35 PO 90, PLC I/O modules and other consumers but not from contactors, brakes or solenoid valves can be connected to the 24 V power supply. The 0 V busbar is connected to the PE busbar by means of a short line with a cross section of 6 mm^2.
- All the 0 V lines to the separate units should be as short as possible and have a cross section of at least 4 mm^2.
- The T300 0 V is connected to the 0 V busbar of the 24 V power supply by means of a short line with a cross section of 6 mm^2.
- The 0 V and + 24 V of the separate electronic mains unit are connected to the INI plug of the 35 PO 90 (see section 10.1.6.1, Initiator cable 35 AK 40).
- The initiators (limit positions) are supplied directly by the Up power supply unit and only the signal connection is connected to the 35 PO 90 (INI plug).

35 PO 90 with AXODYN® three-phase-current drive amplifiers of the DRH/DPH type:

The following earthing and wiring concept is also valid for other drive amplifiers.

A buffer stage with an optocoupler can be received as an option for the DRH/DPH drive amplifiers. It can be ordered under the code "encoder interface DV 3001" from the company responsibie for the drive amplifier.

Serial interface (V24):

The screen is connected on the 35 PO 90 and on the operator unit via PIN 1 of the respective plug.

Set value interface (Uw):

The screen is connected on one side only, on the DRH/DPH side to X3/5 (SW1(or X3/8 (SW2).

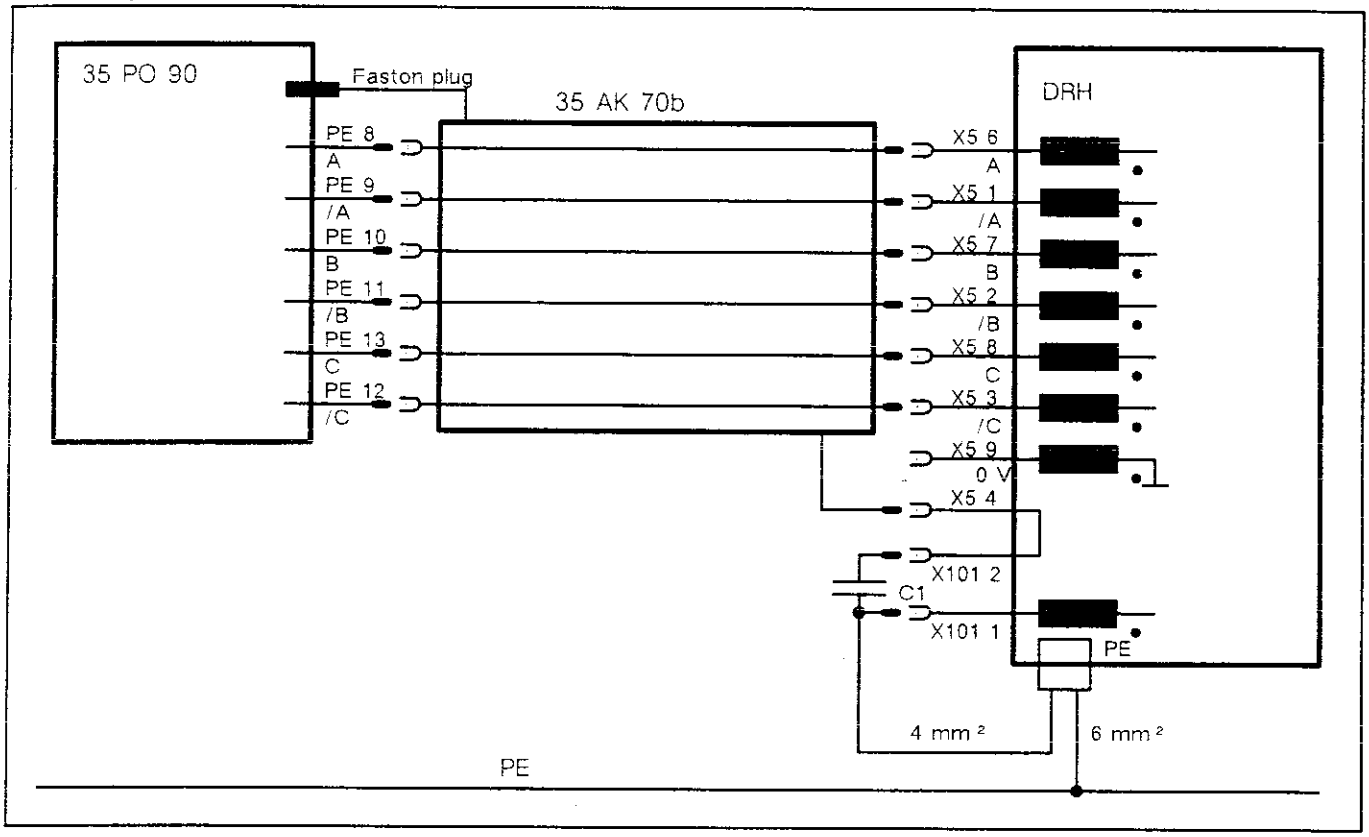
Position encoder interface (PE):

The screen is connected on the 35 PO 90 with the faston plug emerging from the plug connection of the 35 AK 70 on the faston tab attached directly above the PE plug.

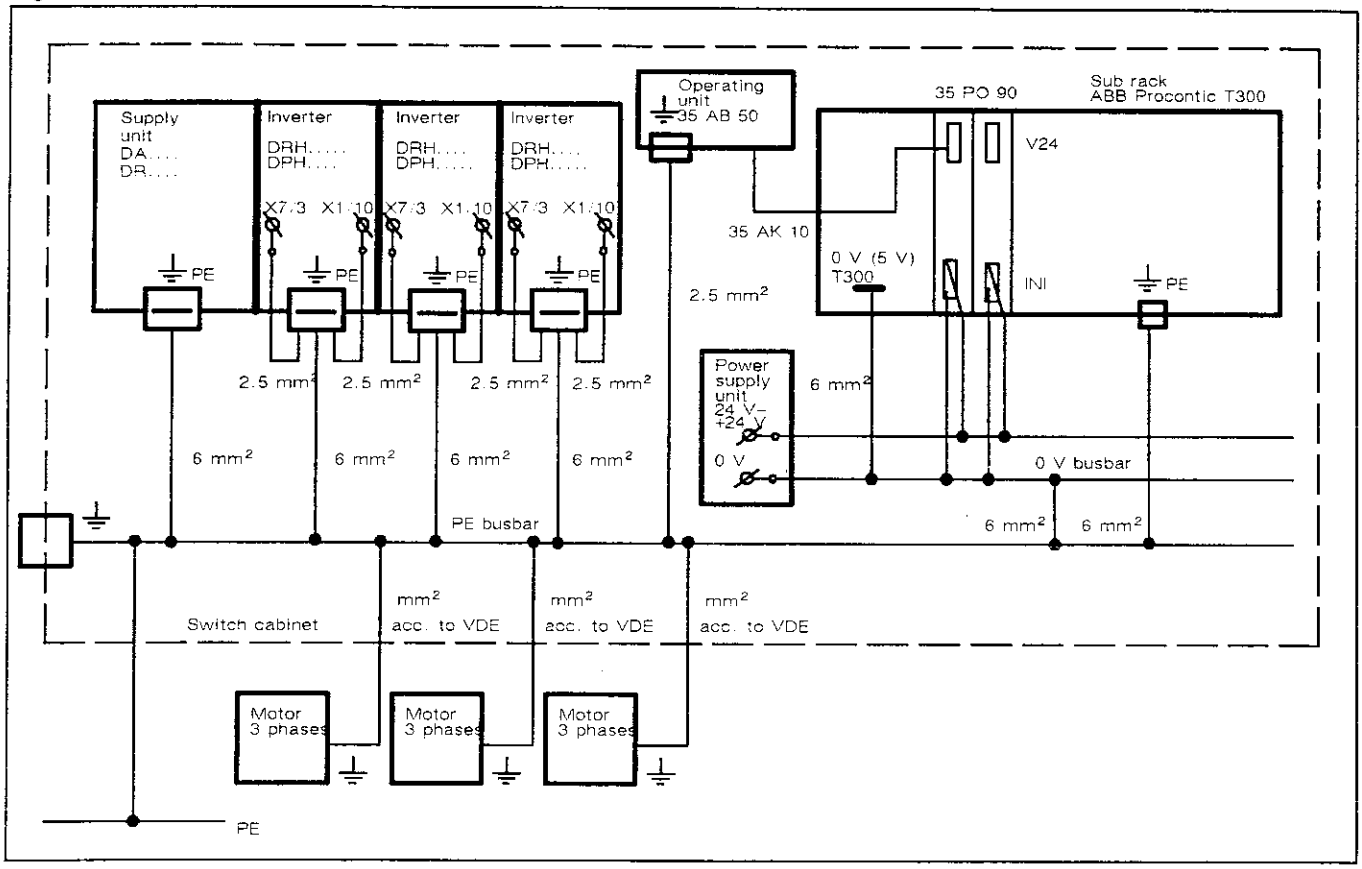
The screen is wired up on the DRH/DPH via a capacitor (C1 = 0,1 µF/MKT/250 V ABB type code: MKT XN 400005 P7) according to the following figure.

If the user is not working with a drive amplifier of the DRH type, the PE screen is to be connected on the 35 PO 90 only and insulated on the encoder.

Screening the PE interface:



Earthing and wiring concept for the 35 PO 90 with AXODYN® AC drive amplifiers of the DRH/DPH design:



10.1.6.3 Starting instructions

- The user should become familiar with the system components before switching on the device for the first time.
- Does the wiring of the system correspond to the recommended earthing and wiring concept?
- Starting and optimising the drive (see description of the drive amplifier).
- Setting up the 35 PO 90 (see section 10.1.4.5, Settings)
- Screw the 35 PO 90 units into the subrack before starting the device.
- Discharge the switch cabinet before touching the 35 PO 90 units (even when starting the device).
- **Note:**
  The front plugs of the 35 PO 90 may not be unplugged or inserted with the voltage supply switched on.
- The 35 PO 90 is programmed by the factory with a standard program. Starting the drive for the first time is possible with this program.
- Check whether the system cables are connected (observe section 10.1.6.1, System cables, and section 10.1.6.2, Earthing and wiring concept).
- Take the PLC out of service and set the drive amplifier enable to 0.
- Switch on the electronic power supply unit + 24V (UP1).
- Switch on the ABB Procontic T300 supply voltage: the LEDs "B", "+" and "Z" light up. The text "35 PO 90 READY" appears on the operating unit. Possible diagnosis errors with section 10.1.6.6.
- Check the initiator inputs with the operating unit (see section 10.1.5.5.3 and section 10.1.5.6) for their correct functioning (dampening the initiators manually).
- Set the drive amplifier enable to 1: the drive is in the position control (attention: the drive runs too high if the poles for the set value are confused).
- Approach the limit positions in the operating mode "manual control". The drive must stop with the approach of the limit position and the LED "E" must light up. Leave the limit positions by "manual control" in the opposite direction (selection with "+/- key").
- If the positive and negative drive directions are confused, the following alterations are necessary:
- Position encoder connection on the 35 PO 90:
  - Swap the connection of track A with track B
  - Swap the connection of track /A with track /B
- Set value output on the 35 PO 90:
  - Change the poles
- If only one of the two measures is carried out, the axis moves too fast. (**Attention:** only permitted with drive amplifiers with a differential input).
- Move to the reference point in the operating mode "move to reference point". The detection of the reference point is acknowledged with the LED "NP". If the 35 PO 90 does not find the reference point, although the reference point initiator is functioning correctly, the problem can lie with too short a reference cam.
  Remedy:
  Turn the pulse encoder, until the 35 PO 90 finds the position encoder zero track pulse, while the reference cam is approached.
- Determination and entry of the machine parameters (see sections: set types and set structure, machine data set):
  - P11 Transmission factor
  - P04 "Maximum drive speed" and if any measuring system is desired:
  - P17, P18 "Setting limits" (Uw is limited to ± 0.1 V by the factory)
  - P01 "Amplification factor" (Kp)
- Enter other machine parameters.
- Enter the user program with the operating unit or in the DNC transmission.
- Run the user program in the operating mode "key/AE"
- Control of the program flow with the PLC.

10.1.6.4 PC software 935 AM 50

The possibility of communicating with a (IBM compatible) PC via the serial interface of the 35 PO 90 exists with the 935 AM 50 PC software.

Possible SW functions:
The software consists of four programs, which can run on the operating system MS DOS.

- XCOPY Copying from and to the 35 PO 90
- XEDIT NC program editor
- XPRINT Printing out 35 PO 90 programs
- XHELP A short description of the listed programs

The prerequisite for the DNC mode is setting up the 35 PO 90 according to section 10.1.4.5, settings.

Serial interface to the 35 PO 90:
COM 1 is used as the serial interface to the 35 PO 90.

The subsettings are permanently set with the recall of the XCOPY command:

Transmission rate:	2400 baud
Word length:	8 bits
Stop bit:	1 bit
Parity:	even

Printer interface:
The logical system interface LPT1 is addressed to control a printer (standard-parallel interface under PC DOS or MS DOS).

If a printer is to be controlled with a serial interface, a deviation to a serial output port by means of a mode command is required.

Example: MODE LPT1: = COM1

This interface can be adapted by a mode command:
MODE COM1: (baud, parity, data bits, stop bits)

Example: MODE COM1: 9600, N, 8, 1

Description of the SW functions:
The follwing functions are implemented in XHELP:

1. XCOPY	Transferring files
2. XPRINT	Printing out files
3. XEDIT	Editing or altering files

XCOPY:
Recall:
XCOPY AXU(n) (drive) target file
(35 PO 90 –> PC transmission)
e.g., XCOPY AXU1 A:ABB1.AXU

XCOPY (drive) source file AXU(n)
(PC –> 35 PO 90 transmission)
e.g., XCOPY A:ABB1.AXU AXU1

Explanations:

Drive	e.g., C:, A:
Target file	Name of the file, to which the copying should take place, e.g., ABB1.AXU
Source file	Name of the file, from which the copying should take place, e.g., ABB1.AXU
AXU	35 PO 90
n	Number of the 35 PO 90 (1 to 6), but this is only when using the electronic reversing and interface logic; otherwise, the transmission of the parameter n is not carried out.

The maximum length of a file name amounts to 8 characters, full stop, 3 characters or figures.

XPRINT:
Recall:
XPRINT (drive) source file
(transferring the file to the printer)
e.g., XPRINT A:ABB.AXU

Explanations:
As for XCOPY

XEDIT:
Recall:
XEDIT (drive) source file
e.g., XEDIT A:ABB1.AXU

2 files are required in the XEDIT mode: XEDIT.COM and XEDIT.OVR.

Both must be located in the registered drive.

Operation:
The entry is constantly checked for its feasibility. The type and limit values are displayed in the status line. The set parameter to be processed is shown in a dark colour on the screen.

Value entry:
+/– sign, 0 to 9 and delete key

Comment entry:
All characters, which can be illustrated, as well as the delete key, DEL and INS

Cursor:
Keys left, right, up, down, home and end

Scrolling:
Page up, page down

The edit mode can be affected by the following keys:

SHIFT F1:	Leaving XEDIT, storing the file on a disk
SHIFT F2:	Leaving XEDIT, file not saved
SHIFT F3:	Saving the file
SHIFT F4:	Changing the file name

If a file, which is not saved, is entered with the recall of the EDIT mode, a standard file is displayed on the screen.

Special features when working with XEDIT:
- Entry 'MDS':
  - P01:
    Entry value with XEDIT: Kv = Kp-Faktor x 256
    Example: Kp = 2.00 => Kv = 2.00 x 256 = 512 (value to be entered).

- Entres in any measuring system:
  - If the "MDS" P11 ≠ 0 is programmed (entry in any measuring system), the entry of the position and speed set values must be carried out incrementally with XEDIT. The conversion into the desired measuring unit is then carried out by the 35 PO 90.

- Entry position values

  $POS_{METR} = 1/P11 \times POS_{INC}$

- Entry drive speed value:

  $FEED_{METR} = 12.5/P11 \times FEED_{INC}$

  $Vmax_{METR} = 12.5^{*}/P11 \times Vmax_{INC}$

* the factor 1/12.5 results due to the 35 PO 90 internal numerical representation.

10.1.6.5 Control of the 35 PO 90 with ABB Procontic T300 industrial computer

The control of the 35 PO 90 via the ABB Procontic T300 industrial computer is possible.

If the 35 PO 90 MPST bus interface is to be accessed by the PLC (block POKO) and by the industrial computer, the block enable of the PLC block POKO must be set to 0 before an industrial computer access to the 35 PO 90 MPST bus interface. The configuration of the block enable of the block POKO as a "super global value" in the PLC is possible.

10.1.6.6 LED diagnosis

The following errors are signalised by the LEDs on the front panel flashing. The errors cn only be acknowledged by switching off the ABB procontic T300 supply voltage or by a 35 PO 90 signal card reset:

LED 'B' flashes in 1 s cycle:
Binary input 'reserve' is not connected to +24 V or the 24 V power supply voltage is still switched off when the T300 power supply voltage is switched on. → Connect input 'reserve' to +24 V (see initiator cable) or switch on the 24 V power supply voltage UP1 before switching on the T300 power supply voltage.

LED 'B', 'E', and '+' flash in a 0.1 s cycle:
The 35 PO 90 internal software watchdog (supervision program) has been addressed.

LED 'B', 'E', '+' and '–' flash in a 0.1-s cycle:
The MPST bus signal/PFD has displayed a voltage failure.

LED 'B', 'E', '+', '–' and 'Z' flash in a 0.1 s cycle:
The 35 PO 90 internal stack supervision routine has been addressed.

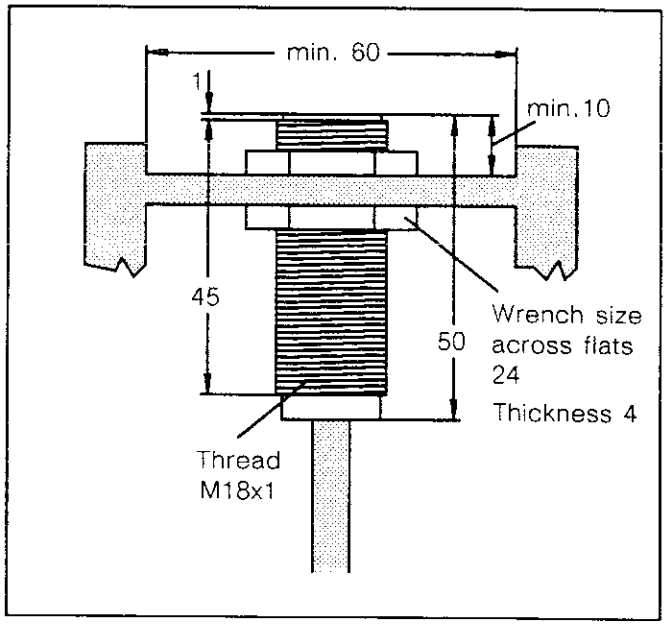
10.1.6.7 Extension of the user program segments in the RAM by re-assembling the processor printed board.

Re-assembly:
If the RAM block 6264 (8k x 8) assembled by the factory is replaced by a RAM block 43256 (32k x 8) and the assembly of the resistors R11 and R12 is adapted (see table below), 11 further user program segments are available in the RAM of the 35 PO 90 for the user. Changing the 35 PO 90 firmware is not necessary.

Resistor	Status	Meaning
R11	not assembled *	A17 = 8k x 8 RAM
R11	assembled	A17 = 32k x 8 RAM
R12	assembled *	A17 = 8k x 8 RAM
R12	not assembled	A17 = 32k x 8 RAM

* Factory assembly

10.1.6.8 Assembly of the initiators:



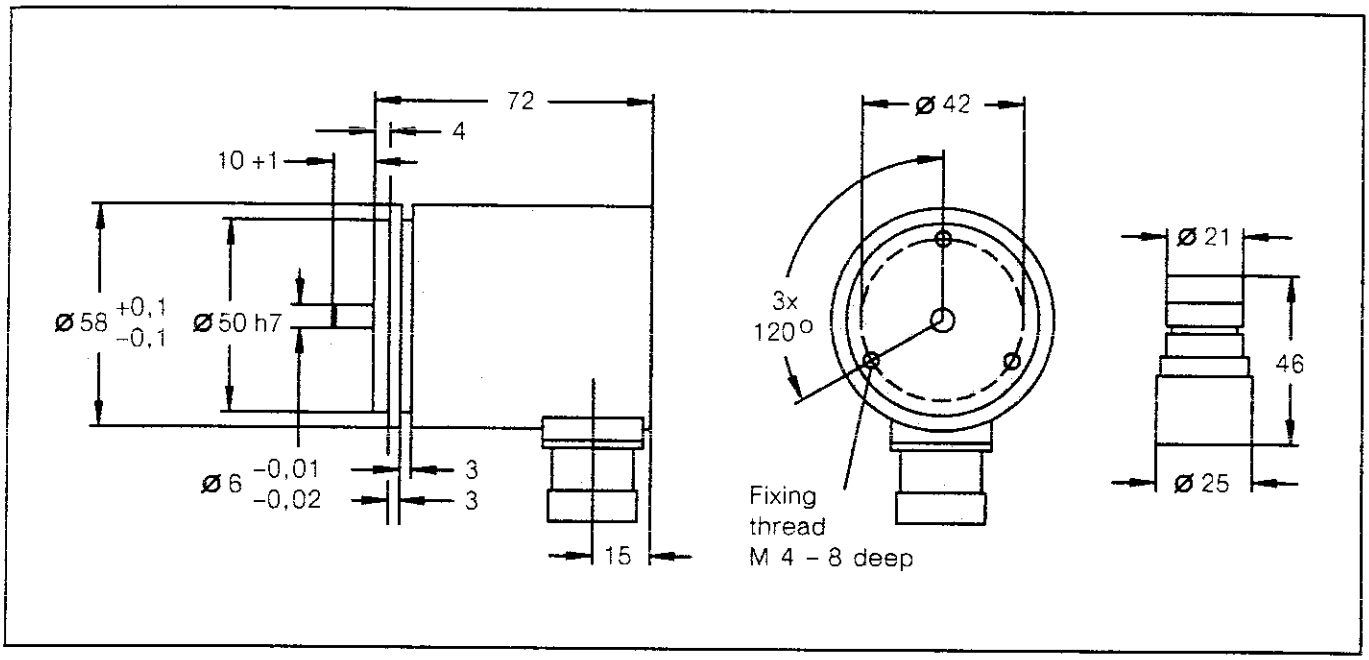
10.1.6.9 Operating with the 35PO90 and 35US50

It is necessary to switch on the 35 US 50 approx. 30 seconds after the ABB Procontic T300, as the latter takes some seconds (power-on reset), before it becomes accessible (including the 35 PO 90) after the power is switched on.

When it is switched on, the 35 US 50 autmatically detects the number of the 35 PO 90 units connected.

However, if the connection of the 35 US 50 is effected via the PLC program, the 35 US 50 can only work while the PLC program is in operation (it cannot work when the program is stopped or in the remote mode).

10.1.6.10 Incremental position encoder



Technical data

Power supply voltage	+ 5 V ± 5 %
Current consumption	max. 220 mA (without load)
Total power dissipation	max. 1.1 W
Order numbers	
- Position sensor 500 incr./revolution	GJV3075101R1
- Position sensor 1000 incr./revolution	GJV3075101R2

Mechanical data

Dimensions	see figure above
Weight	approx. 390 g (according to type)
Motor starting torque (at 25 °C)	
- without shaft seal	max. 0.007 Nm
- with shaft seal	max. 0.035 Nm
max. permissible speed	6000 rev/min (without shaft seal) 3000 rev/min (with shaft seal)
Bearing lifetime	10^9 revolutions
Shaft load capability	118 N (radial), 98 N (axial)

Environmental conditions

Temperature	
- operation	0 °C to + 70 °C
- storage	- 25 °C to + 80 °C
Humidity	max. 98 % relative humidity
Degree of protection (according to DIN 40050,page 1)	IP 64
Shock (standard value)	20 g, 11 ms
Vibration (standard value)	10 g, 5...2000 Hz

Materials

Base	aluminium, passivated in chromic acid
Housing	aluminium, black anodized
Shaft	non-magnetic stainless steel
Bearing	ABEC 5
Light source	GaAs infra-red LED

Handling instructions for incremental encoders

Connection of the encoder shaft can be carried out via a custom specified metal bellow coupling.

If the encoder is to be driven by means of a gear-wheel or roller, care must be taken that the gear-wheel is mounted onto the shaft stub with Ø 6 mm -0,01 / -0,02 mm. No backlash should be present (e.g. faulty gripping of gear-wheels) when changing the direction of rotation.

Under no circumstances should the permissible axial or radial shaft loads be exceeded (see Technical Data).

Caution! Do not engage or disengage any connectors while equipment is under power!

First of all do not

All this involves the loss of warranty.

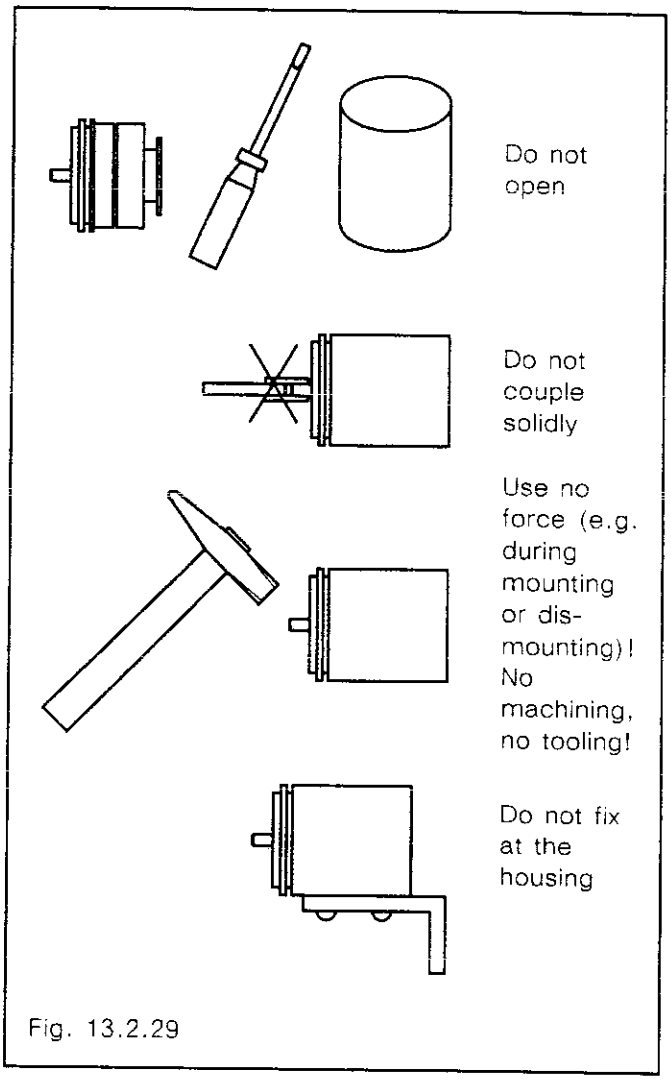


Fig. 13.2.29

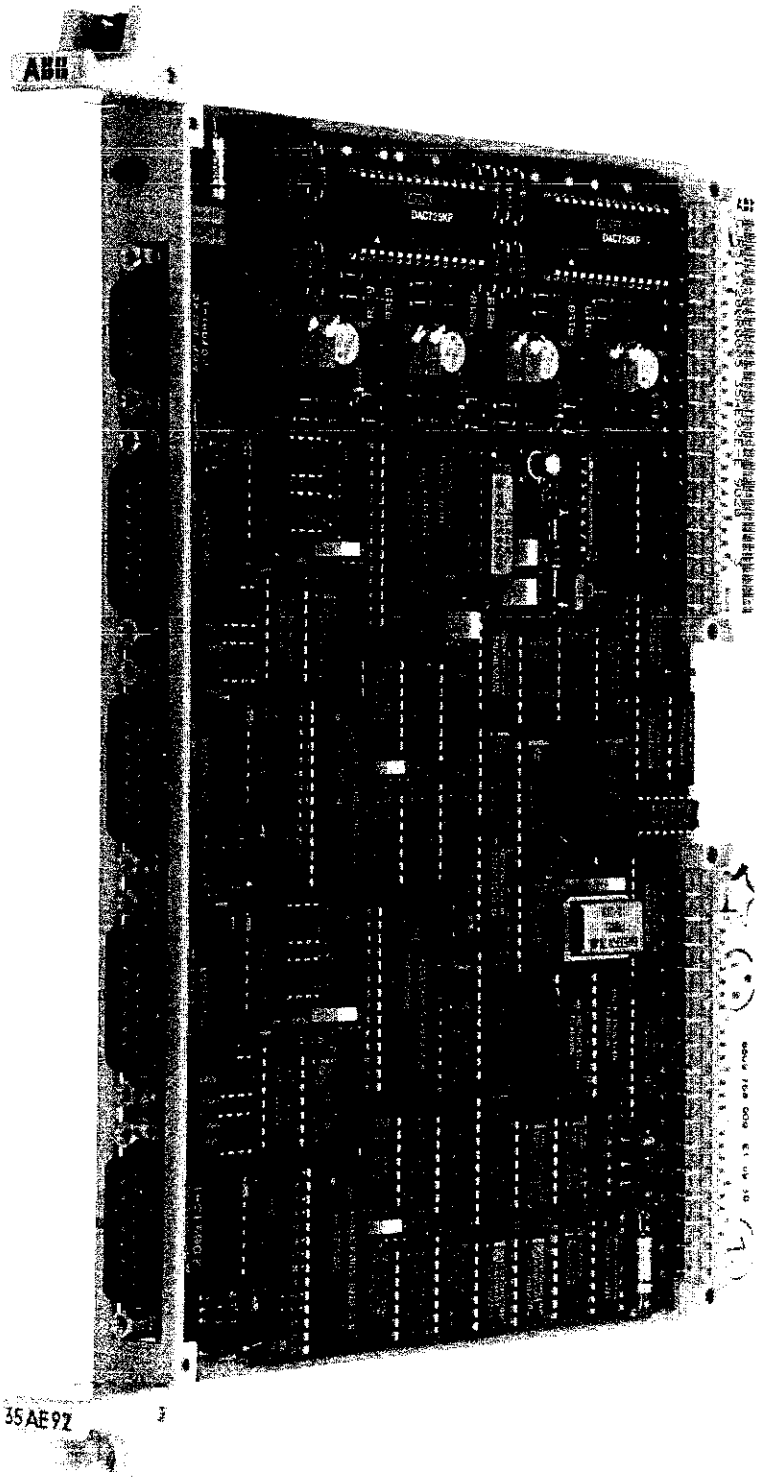
Incremental sensors/cable lengths

Beside the incremental sensors (+ 5 V power supply voltage) available from ABB, + 15 V sensors can also be connected. The supply voltage of the incremental sensor is set via X5 (see chapter 13.2.4.3, Settings).

Cable length of the position sensor cable:

	Sensor supply via 07 PO 60	Sensor supply externally
Sensor with + 5 V supply	max 20 m	max 20 m
Sensor with +15 V supply	max 20 m	max 20 m

10.2 Axis card 35 AE 92 R4, R5



90 05 17

10.2.1 Technical data

Axes for rubric R4	2
rubric R5	4
Encoder	Incremental 5 V/15 V with a differential output RS 422
U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+ 15 V ± 5 %
U_{B3} positive supply voltage	− 15 V ± 5 %
I_{B1} supply current to U_{B1}, rubric R4	1 A ± 20 % plus I_{X3} + I_{X4}
I_{B1} supply current to U_{B1}, rubric R5	1.4 A ± 20 % plus I_{X3} ... I_{X6}
I_{B2} supply current to U_{B2}, rubric R4	0.06 A ± 20 % plus I_{X3} + I_{X4} +I_{X7}
I_{B2} supply current to U_{B2}, rubric R5	0.10 A ± 20 % plus I_{X3} ... I_{X7}
I_{B3} supply current to U_{B3}, rubric R4	0.06 A ± 20 % plus I_{X7}
I_{B3} supply current to U_{B3}, rubric R5	0.10 A ± 20 % plus I_{X7}

I_{X3} ... I_{X6} is the supply current taken from the plugs X3, X4, X5 and X6 to supply the external auxilliary logics and encoder lamps.

I_{X7} is the output current of the analogue amplifier taken from the plug X7.

Supply currents for the external logics at X3 ... X6:	
I_{tot} (U_5) = I_I + I_5	Imax. 0.5 A/axis
I_{tot} (U_{15}) = I_{15}	Imax. 0.3 A / axis (note the capacity of the ABB Procontic T300 power supply unit)
Line length for external logics or path encoder:	
For I_{tot} = 0.3 A and A = 0.5 mm²	typically 10 m
Total power loss rubric R4	5.8 W
Total power loss rubric R5	10 W
Input values for path encoder signals:	
Input switch	according to RS 422
Common-mode rejection	max. + 25 V
Differential input voltage	max. 7 V with 5 V encoders/max. 16 V with 15 V encoders
Differential input high threshold	max. + 0.2 V
Differential input low threshold	max. − 0.2 V
Line terminator RC element (5 V or 15 V)	R typically 300 Ω or 820 Ω C typically 330 pF
Input current, static	≤ 20 mA
dynamic	≤ 40 mA
Flank clearance (U_{a1} − U_{a2} with $f_{inp.}$ = 1 MHz)	250 ns
Input frequency U_{a1}, U_{a2}	≤ 1 MHz
Pulse width U_{a0}	≥ 5 µs
Input frequency U_{a0}	≤ 20 kHz
Watchdog for reading the actual values:	
Time delay	typically 20 ms
Adjustable (assembly position 1001)	0.7 ... 150 ms
Touch probe input:	
Signal level: 0 Signal	0 ... 1.2 V
1 Signal	2.4 ... 30 V
Input current	≤ 2 mA
Delay tv	400 ns
Exe interference signal $\overline{Uas}$:	
Signal level	TTL
Input current	≤ 0.5 mA
Delay tv	typically 50 µs

Output data (non-floating):	
For digital value 7FFFH (+ FS)	+ 10 V
For digital value 0000H (0)	0 V
For digital value 0FFFFH (- 1)	- 1 LSB
For digital value 8000H (- FS)	- 10 V
Arithmetical resolution (1LSB)	0.305 mV
Monotony	14 bits
Output amplifier delay for the output signal change from +FS to -FS	< 200 µs
Loading resistor	> 5 kΩ
Output inductivity, bifilar reactor	typically 140 µH
Effective inductivity	typically 1.5 µH
Zero point error:	
With a factory balance	< 17 mV
With a balance in the system	< 5 mV
Zero point drift in the permitted temperature range	< 10 mV
Ouput voltage error:	
With a factory balancing	< 17 mV
With a balancing in the system	< 5 mV
Output voltage drift in the Permitted temperature range	< 15 mV
Symmetry and linearity error	< 4 mV
Symmetry and linearity drift in the permitted temperature range	< 2 mV
Offset voltage, setting range	typically ± 15 mV
Output voltage, setting range	typically ± 25 mV
Ambient values:	
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	1 pitch
Weight, rubric R4	1.0 kg
rubric R5	1.0 kg
Order number: rubric R4	GJR5137200 R4 (for 2 axes)
rubric R5	GJR5137200 R5 (for 4 axes)

Note: The unit of rubric 5 is shown in the photograph on the first page.

10.2.2 Description

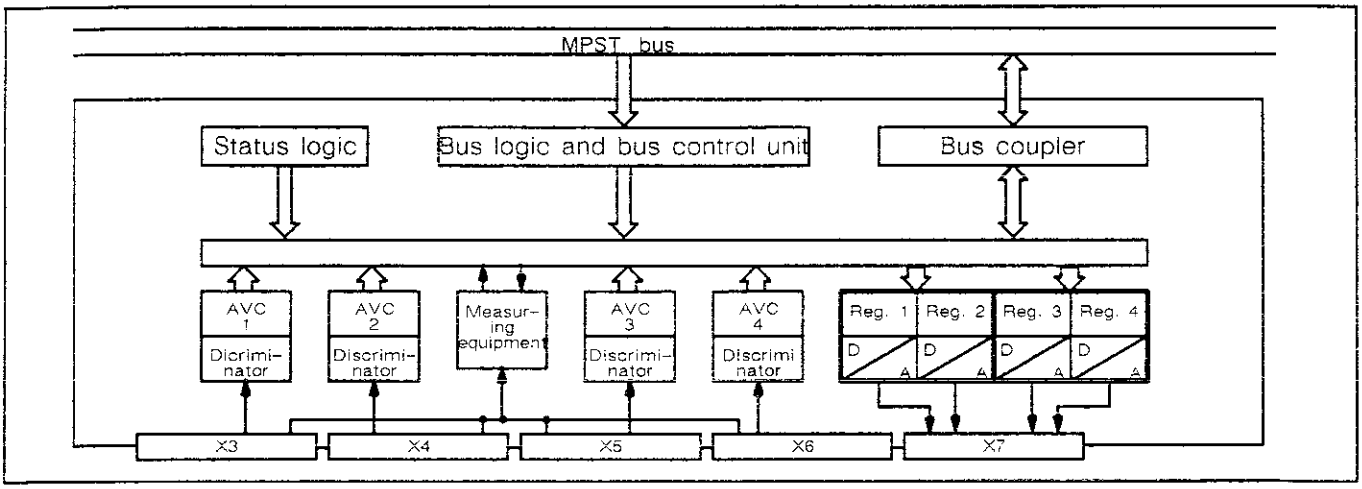
The axis card 35 AE 92 R4 and R5 is a passive subscriber on the MPST bus. rubric 4 is designed for 2 axes, rubric 5 for 4 axes. The axis card mainly executes the following functions:

Reception and evaluation of the path encoder signals

- Path encoders, which supply square-wave pulse rows shifted in their phase by 90°, can be connected.
- Creation of path pulses in three phases and which are added in a 16 bit forwards/backwards counter with an overflow, without carry, in the direction discriminator.
- The actual value counter can be read by the MPST bus. Its level is not deleted during the reading procedure.
- Reception of the encoder zero pulses and deletion of the actual value counters for the reference point movement, if the zero mark is reached.
- Deletion of the actual value counter with reset.

Reception and output of the speed set values

- Saving for 16 bit speed set values in registers, which can be written by the MPST bus.
- Conversion of the digital set value into an analogue voltage and output to the drive amplifier.
- Setting the KV factor with the software.
- Deletion of the set value with reset.



AVC = actual value counter

Fig. 10.2-1 Block diagram of the axis card 35 AE 92 R5

Measuring operating mode

- Possibility to connect a "touch probe". This creates a trigger pulse, which maintains the current counter level of all axes on the unit.
- Software creation of the touch trigger pulse for the simultaneous position determination of all 4 axes.

Diagnosis

- It can be read in one of the status bytes assigned to the respective axis, whether there is an encoder malfunction or an encoder line break or whether the "watchdog" has been addressed.
- Optical display "watchdog not addressed" by the LED H1.

Interfaces

- A 15-polar plug (X3 ... X6) is available on the front of the units to connect the path encoder, its supply (lamp and logic) and as a "touch probe" input.
- The 9-polar plug connector X7 serves to connect the drive amplifier (non-floating).

Supervision

- Supervision of the actual value prompting by the MPST bus. If an adjustable time reference is not observed, the "watchdog" is addressed. It deletes the set values of all axes and is stored depending on the operating mode. It also controls the optical display H1 (watchdog active = LED (light emitting diode) H1 goes out) and sets a status bit. The message can be latched or not.

10.2.3 Mechanical structure

Unit in the double-size in the Eurocard format, 160 x 233, 4 mm, 1 pitch.

Displays:
H1 operating display, watchdog is not addressed

Plug connectors:

X1, X2	32-polar bus interface according to DIN 41 612, part 2 design C
X3, X4, X5, X6	Encoder interface, plug connector AMP HDP 20, 15-polar
X7	Analogue interface, plug connector AMP HDP 20

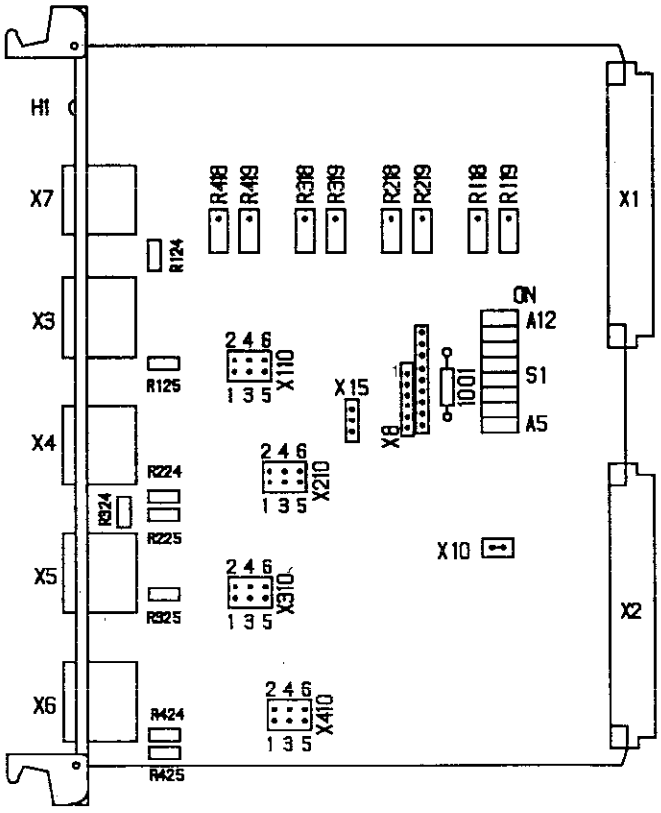


Fig. 10.2-2 Component side (top view).

Non-drawn pins are measuring points, which may not be connected.

R124 and R125 or R224 and R225 or R324 and R325 or R424 and R425 are highly set 470 Ω resistors to adapt the encoder to the respective axis. These resistors are to be interrupted or removed when using encoders with an output voltage of 8 V ... 15 V.

10.2.4 Plug assignment

10.2.4.1 MPST bus interface, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	U B3	– 15 V voltage	X1. 6c	U B2	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	–	–	X1.24c	–	–
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	–	–	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

10.2.4.2 Front plugs

Encoder interface for axis 1 (plug X3):

PIN	Signal name	Meaning
X3.1	Ua1	Encoder pulse 0°
X3.2	$\overline{Ua1}$	Encoder pulse 180°
X3.3	Ua2	Encoder pulse 90°
X3.4	$\overline{Ua2}$	Encoder pulse 270°
X3.5	Ua0	Zero pulse 0°
X3.6	$\overline{Ua0}$	Zero pulse 180°
X3.7	0 V	Ground lamp
X3.8	UL +	Lamp supply level + 5 V
X3.9	Uas*	Exe interference signal
X3.10	U15	Logic supply level + 15 V
X3.11	U5	Logic supply level + 5 V
X3.12	0 V	0 V logic
X3.13	0 V	0 V logic
X3.14	UTT	Trigger touch probe
X3.15	–	Screen

Encoder interface for axis 3 (plug X5):

PIN	Signal name	Meaning
X5.1	Ua1	Encoder impulse 0°
X5.2	$\overline{Ua1}$	Encoder impulse 180°
X5.3	Ua2	Encoder impulse 90°
X5.4	$\overline{Ua2}$	Encoder impulse 270°
X5.5	Ua0	Zero pulse 0°
X5.6	$\overline{Ua0}$	Zero pulse 180°
X5.7	0 V	Ground lamp
X5.8	UL +	Lamp supply level + 5 V
X5.9	Uas*	Exe interference signal
X5.10	U15	Logic supply level + 15 V
X5.11	U5	Logic supply level + 5 V
X5.12	0 V	0 V logic
X5.13	0 V	0 V logic
X5.14	UTT	Trigger touch probe
X5.15	–	Screen

Analog interface (plug X7):

PIN	Signal name	Meaning
X7.1	Ua1	Analog voltage for axis I
X7.2	0V1	0 V analog axis I
X7.3	Ua2	Analog voltage for axis II
X7.4	0V2	0 V analog axis II
X7.5	Ua3	Analog voltage for axis III
X7.6	0V3	0 V analog axis III
X7.7	Ua4	Analog voltage for axis IV
X7.8	0V4	0 V analog axis IV
X7.9	–	Screen

Encoder interface for axis 2 (plug X4):

PIN	Signal name	Meaning
X4.1	Ua1	Encoder pulse 0°
X4.2	$\overline{Ua1}$	Encoder pulse 180°
X4.3	Ua2	Encoder pulse 90°
X4.4	$\overline{Ua2}$	Encoder pulse 270°
X4.5	Ua0	Zero pulse 0°
X4.6	$\overline{Ua0}$	Zero pulse 180°
X4.7	0 V	Ground lamp
X4.8	UL +	Lamp supply level + 5 V
X4.9	Uas*	Exe interference level
X4.10	U15	Logic supply level + 15 V
X4.11	U5	Logic supply level + 5 V
X4.12	0 V	0 V logic
X4.13	0 V	0 V logic
X4.14	UTT	Trigger touch probe
X4.15	–	Screen

Encoder interface for axis 4 (plug X6):

PIN	Signal name	Meaning
X6.1	Ua1	Encoder pulse 0°
X6.2	$\overline{Ua1}$	Encoder pulse 180°
X6.3	Ua2	Encoder pulse 90°
X6.4	$\overline{Ua2}$	Encoder pulse 270°
X6.5	Ua0	Zero pulse 0°
X6.6	$\overline{Ua0}$	Zero pulse 180°
X6.7	0 V	Ground lamp
X6.8	UL +	Lamp supply level + 5 V
X6.9	Uas*	Exe interference level
X6.10	U15	Logic supply level + 15 V
X6.11	U5	Logic supply level + 5 V
X6.12	0 V	0 V logic
X6.13	0 V	0 V logic
X6.14	UTT	Trigger touch probe
X6.15	–	Screen

* If the Exe interference signal is not used, the corresponding input of the affected axis is to be switched to + 5 V.

10.2.5 Unit addresses on the MPST bus

10.2.5.1 Address division

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	0
MPST code of the upper, passive address area (perm. wired up)			Unit address for S1 on the axis card 35 AE 92 can be set (See also 10.2.10.1)								Axis address		Selection of the operating mode		

10.2.5.2 Address overview

Axis	Operating mode	Access	Address	Data
1	Status	R/W	XX**0H	D07...D00
	Actual value	Read	XX**2H	D15...D00
	Set value	Write	XX**4H	D15...D00
	Measuring value	R/W	XX**6H	D15...D00
2	Status	R/W	XX**8H	D07...D00
	Actual value	Read	XX**AH	D15...D00
	Set value	Write	XX**CH	D15...D00
	Measuring value	R/W	XX**EH	D15...D00
3	Status	R/W	XX *0H	D07...D00
	Actual value	Read	XX *2H	D15...D00
	Set value	Write	XX *4H	D15...D00
	Measuring value	R/W	XX *6H	D15...D00
4	Status	R/W	XX *8H	D07...D00
	Actual value	Read	XX *AH	D15...D00
	Set value	Write	XX *CH	D15...D00
	Measuring value	R/W	XX *EH	D15...D00

** Bit4 of address low byte must be set to 0.

* Bit 4 of address low byte must be set 1.

10.2.5.3 Assignment and function of the address bits A0 ... A4

Axis addresses		
Address bit	A04	A03
Axis 1	0	0
Axis 2	0	1
Axis 3	1	0
Axis 4	1	1

Operating modes selection			
Address bit	A02	A01	A00
Status	0	0	0
Actual value	0	1	0
Set value	1	0	0
Measuring value	1	1	0

10.2.6 Status byte

The separate bits of the status byte have the following meaning:

Bit	Function	active	write	read
D00	Reference point active	1	X	
D01	Reference point reached	1		X
D02	Touch probe activation	1	X	
D03	Measuring result ready	1		X
D04	Encoder malfunction	1		X
D05	Encoder line break Ua1	1		X
D06	Encoder line break Ua2	1		X
D07	Watchdog addressed	1		X

The status bits D0 and D2 can not be read.

10.2.7 Settings

10.2.7.1 Setting the unit address

DIL switch **S1**:

Example for address E500

This unit fills the address area of E500 to E51E. The next unit would then receive the address E520.

10.2.7.2 Watchdog functions

Jumper zone **X8**:

Without jumpers The watchdog is only displayed, in the status byte (bit D7) and optically with the light emitting diode.

Jumper 2–3 Watchdog deletes the set value register. The watchdog is re-activated by reading the actual value and the set value register released.

Jumper 5–6 The watchdog interrupt is saved and the set value deleted, if jumper 2–3 are inserted as well. A status bit to remove the storage function must first be written for the release (e.g., by activating the reference point movement). The actual value must then be read cyclically again, so that the watchdog remains active.

10.2.7.3 Setting the address time of the watchdog

t (ms) = 0.15 x R (kOhm)

Assembly position **1001**: R min. 4.7 kOhm
(Tolerance: ± 20 %) R max. 1 MOhm

10.2.7.4 Activating the touch trigger

Jumper zone **X15**:

Jumper 1–2	Touch trigger	Activation by 1/0 edge
Jumper 2–3	Touch trigger	Activation by 0/1 edge

10.2.7.5 Operating mode setting of the direction discriminators

Jumper zone **X110**: for axis 1
Jumper zone **X210**: for axis 2
Jumper zone **X310**: for axis 3
Jumper zone **X410**: for axis 4

Method of counting the jumper zones	2 4 6 1 3 5
Four-fold evaluation: (Jumpers 2–4)	o—o o o o o
Double evaluation of Ua1: (Jumpers 3–5)	o o o o o—o
Single evaluation of Ua1: (Jumpers 2–4, 3–5)	o—o o o o—o
Counter application:	o o o o o o

Jumper **X10**: The oscillator jumper must always be inserted.

10.2.7.6 Path encoder interface for Ua1, Ua2 and Ua0

The input switch of the interface corresponds to RS 422 and is realised with the blocks SN 75 173/26 LS 34. The flank clearance t_F of the encoder amounts to 250 ns with an input frequency of 1 MHz.

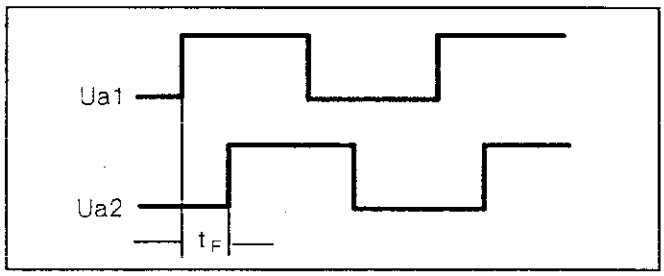


Fig. 10.2-3 Flank clearance t_F

10.2.7.7 Accuracy

Move to reference point

Actual value counter level with the zero pulse 0 ± 1 incr.

Reference point correction

The actual value counter in the individual axes is set to a basic value between ± 1 increment depending on the level of the signals Ua1 and Ua2 with a reset. The deletion of the actual value counters with the reference point movement occurs via the reset input. The position of the reference pulse Ua0 depends on the encoder used.

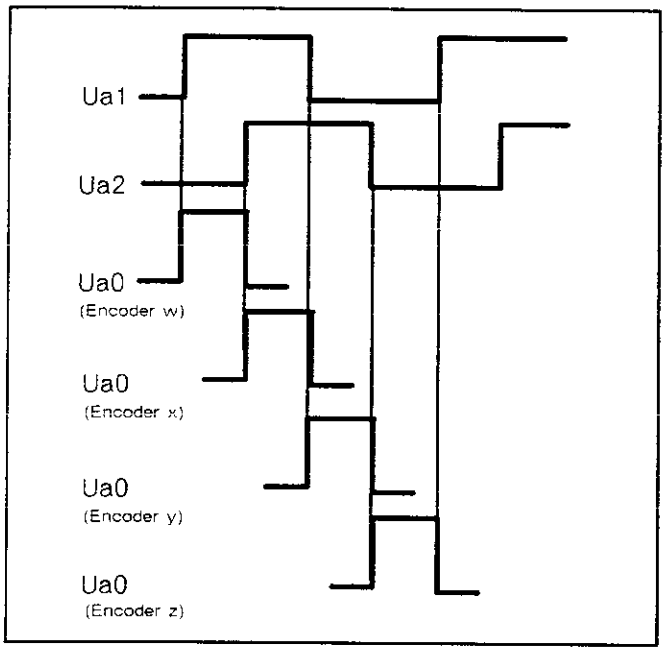


Fig. 10.2-4 Possible position of the reference pulse Ua0 (depending on the encoder)

Actual value counter level	– 1 incr.	0	+ 1 incr.	0
Encoder	w	x	y	z

Measuring accuracy:

The input delay of the UTT input through to the activation of the trigger pulse amounts to max. 400 ns and causes an error with the trigger activation depending on the drive speed.

Measuring error: max.1 increment

10.2.8 Application instructions

For the principle program examples, see chapters 10.2.8.8 and 10.2.8.9.

10.2.8.1 Balancing the analogue unit

The advantage of the balance of the analogue unit in the system is that the zero point error, which is caused by the tolerance of the supply voltages, is no longer necessary.

The balancing is carried out, so that the output voltage on the potentiometers

R119 for axis 1 R219 for axis 2
R319 for axis 3 R419 for axis 4

is set to 0 V (±0,1 mV) with the set value 0. If the potentiometer turns to the right, this causes an enlargement of the output voltage.

The gain balancing with +FS is required after a balance. The balancing is carried out, so that the output voltage at the potentiometers

R118 for axis 1 R218 for axis 2
R318 for axis 3 R418 for axis 4

is set to + 10 V (± 1 mV) with the set value 7FFFH. If the potentiometer turns to the right, this causes an enlargement of the output voltage. At least a 4 1/2-digit voltmeter is to be used for the balancing. The symmetry with – FS (set value = 8000H) is to be checked afterwards. The difference between the amounts of +FS and –FS must amount to $\leq$ 2 mV. The difference can be set to 1 mV when using a 5 1/2-digit voltmeter. The balancing should be carried out with a connected load. The potentiometers are to be secured with fuse laqueur after the balancing has taken place.

The jumper X8/2-3 is to be disconnected for the balancing, so that the set value register is not reset, when the watchdog is addressed.

10.2.8.2 Card initialisation

a) The actual value counters of all the active axes must be read to initialise the direction discriminators.
b) If the watchdog is set to "saving" (jumper X8/5-6), a status byte must be written to activate the watchdog (this generally happens automatically with the reference point movement, which is necessary after switching on the supply voltage).
c) The watchdog is addressed each time the actual value of an axis is read.
d) A measuring value must be read to reset the measuring value logic.
e) The corresponding measuring values must be read to reset the measuring value register.

10.2.8.3 Measuring value function

Measuring movement activation

A measuring movement is activated, when the data bit D2 for a cycle is set to 1 in the status register of any function.

Touch trigger initialisation

All the actual value registers are blocked, when the touch trigger is reached, with a measuring movement. A release of the actual value register of an axis is carried out by reading the respective measuring value register. The measuring value can only be read out from the address for the actual value reading, while the measuring value of an axis was not read but without achieving a release of the actual value register. The corresponding status bit D3 of the axis is reset, when the measuring value is read. The measuring value registers of the non-relevant axes must also be read after a measuring movement in order to achieve the release for the actual value reading.

The measuring value logic can only be re-activated after a completed measuring movement, if at least one measuring value was read out. The contents of the measuring value registers, which have not been read out, are not altered with this new measuring movement.

Reading the measuring value does not reset the watchdog.

For the programming example for the measuring movement, see chapter 10.2.8.8.

Measuring movement reset

An already activated measuring movement can be deactivated by the software without initiating the touch trigger. This can be realised by reading any measuring value on the card, before the touch trigger pulse is emitted. A new measuring movement can then be started by setting D2 at a later point in time.

10.2.8.4 Switching on the touch probe

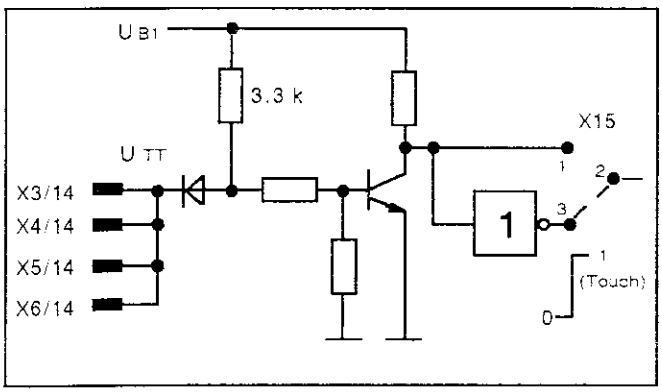


Fig. 10.2-5 Switch extract

Jumper X15	UTT signal	Touch
2 – 3	0 → 1	1 / 0
1 – 2	1 → 0	1 / 0

The signal level is decisive for activating the touch trigger. If the trigger is initiated immediately after its activation, either the incorrect initialisation characteristic is set for X 15 or the trigger signal is already active.

10.2.8.5 Exe interference signal

If the Exe interference signal is not used, the corresponding input $\overline{Uas}$ (Pin 9) of the affected access is to be bridged with + 5 V (Pin 8 or pin 11) in the HD plug.

10.2.8.6 Adapting the path encoder input to the 15 V encoders

To highly set resistors R = 470 Ω must be interrupted or removed per connected access (incremental encoder), if actual value encoders with 15 V outputs are used.

These include the following:

Axis 1	Axis 2	Axis 3	Axis 4
R124 R125	R224 R225	R324 R325	R424 R425

10.2.8.7 Counter application

Each functional unit can be used as a counter, if the jumpers are assigned according to 10.2.7.5. Switching the counter pulses is carried out via Ua1 (RS422). Ua2 (90°, Pin 3) must be switched with 470 Ω according to + 5 V (Pin 8 or Pin 11) and Ua2 (270°, Pin 4) according to 0 V (Pins 7, 12, 13 or pin 15) in the HD plug.

The reading out procedure is carried out via the function "reading the actual value". The counter contents are deleted, when the counter is read.

The connection of Ua2 (90°) and Ua2 (270°) causes the counter release. A signal change to Ua2 (90°), e.g., open input or input for 0 V, stops the counter. It emerges from the stop mode only with the correct connection of Ua2 and reset. A reset of the counting block can also be created via Ua0 (move to reference point).

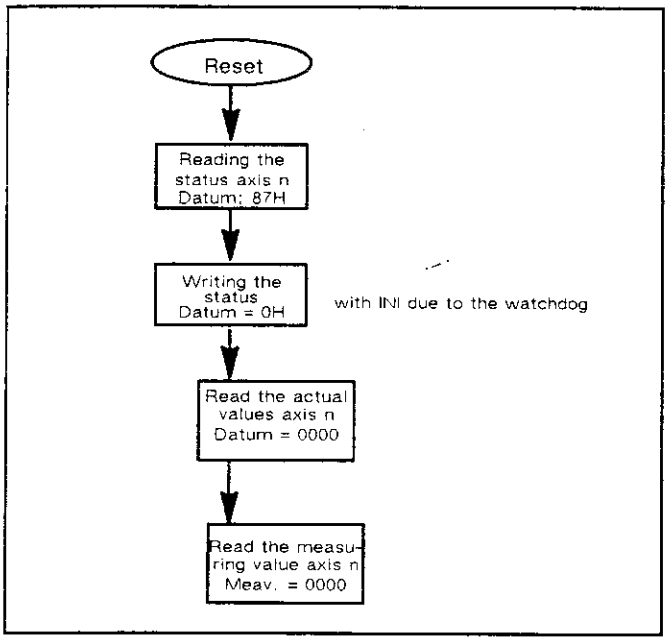
10.2.8.8 Flow diagrams

Principle examples for sequences. The flow diagrams were written in stages, i.e., the watchdog has been addressed.

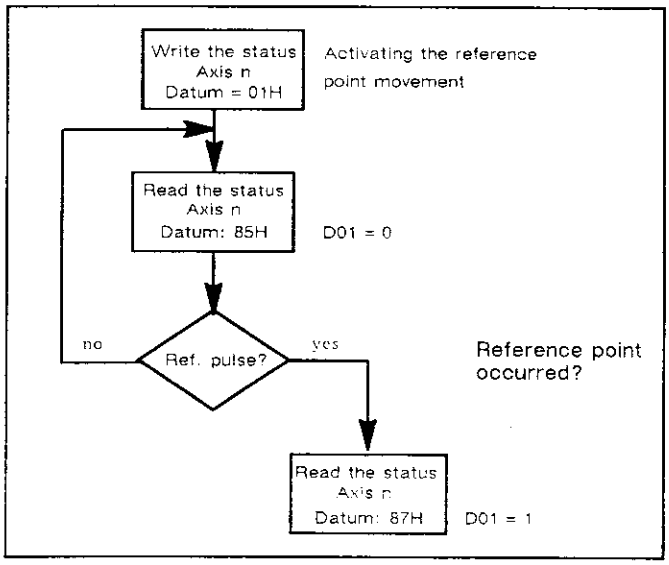
Abbreviations:

Actv.:	Actual value
Meav.:	Measuring value
D03:	Data bit 3
n:	as required (1...4)

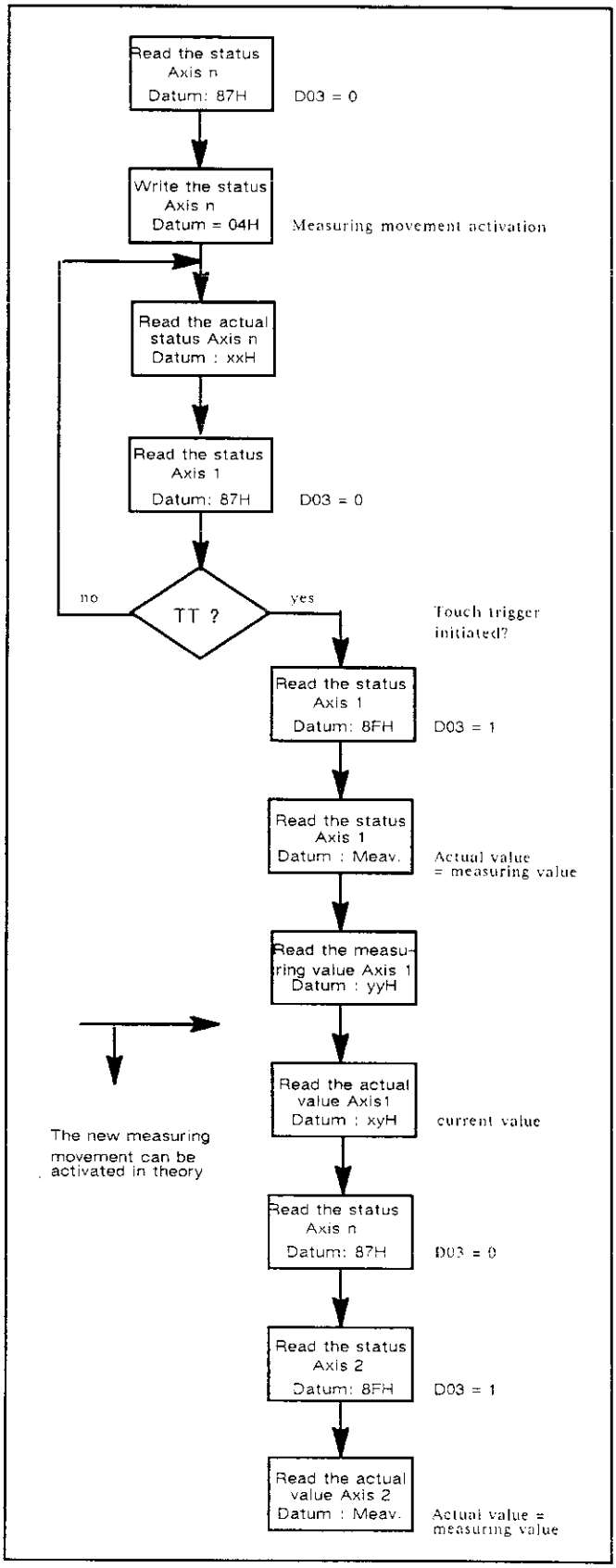
Reset/Initialisation



Move to reference point

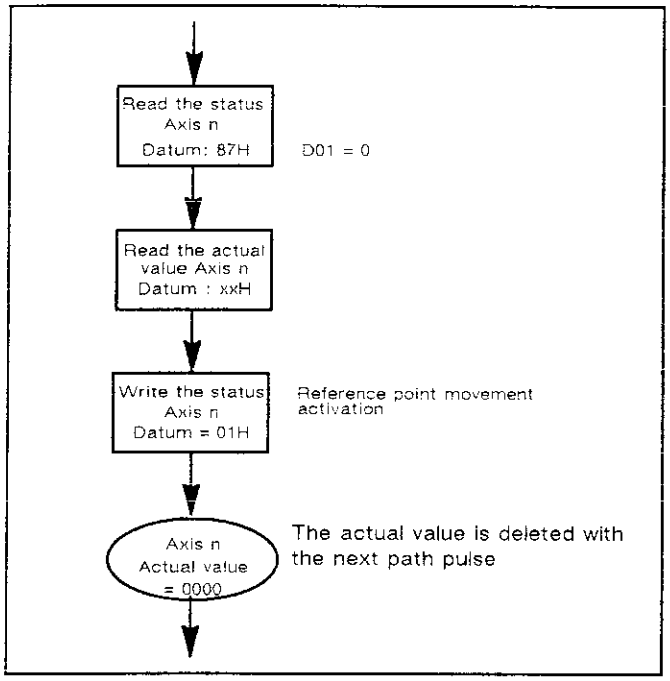


Measuring movement

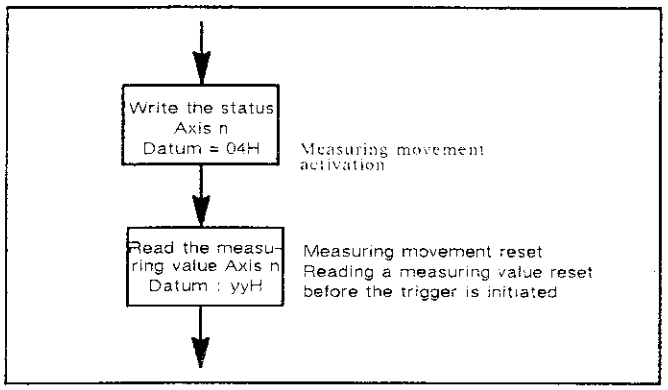


-Move to reference point immediately
-Deleting the actual value counter (cyclically)
-Direction discriminator reset

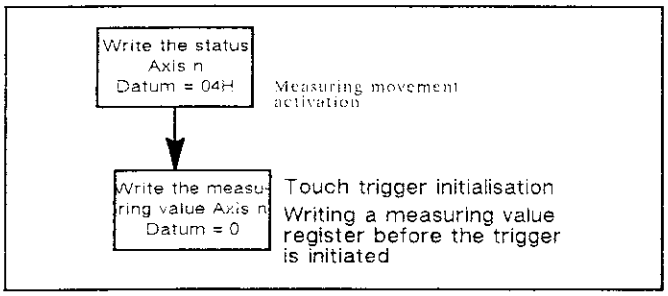
The Uao are to be connected with the inputs either from track A or track B to realise these applications. The limit frequency of Uao is to be observed with these applications!



Measuring movement deletion



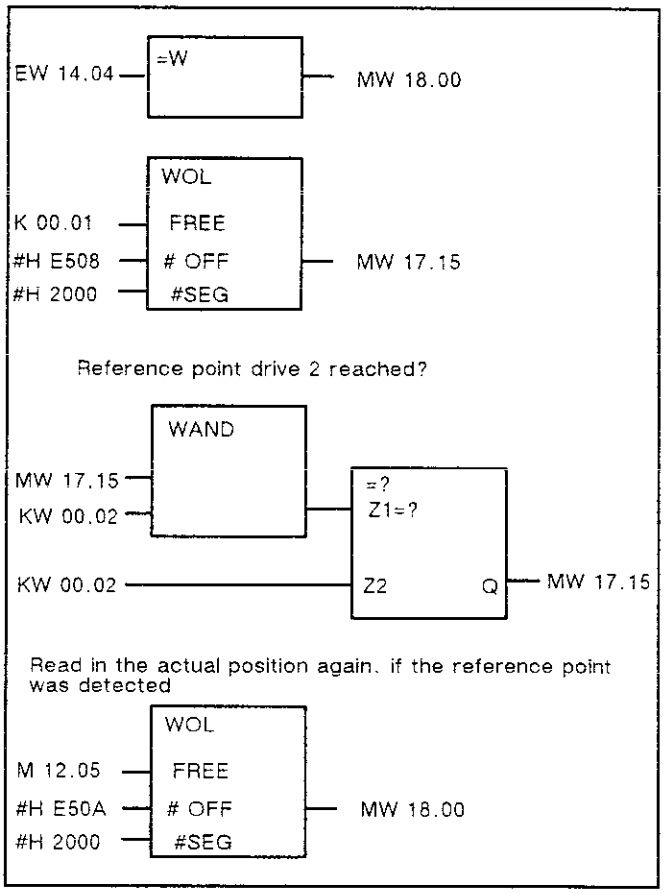
Touch Trigger by the software



10.2.8.9 Program extract 907 PC 31

Move to reference point

The actual value is to be read again after reaching the reference point and the old value deleted, so that plausibility or following errors do not occur after the move to the reference point due to the deleted actual value counter.



Variable:

EW	14.04	IPOS2_ON
K	00.01	TRUE
KW	00.02	TWO
M	12.05	REFSIGNAL2
MW	17.15	STATUS2
MW	18.00	RCTPOS2

10.2.8.10 Switch variants with path encoder interfaces

The path encoder interface is designed in accordance with RS422. The possibility exists of connecting other drivers with negligible switch measures in the cable plug as well. However, the transfer to another type of connection always brings certain limitations. The function of the line break supervision is ensured only. The maximum input frequency is reduced with some applications from 1 MHz to 250 kHz.

Adaptation of the path encoder tracks Ua1 and Ua2

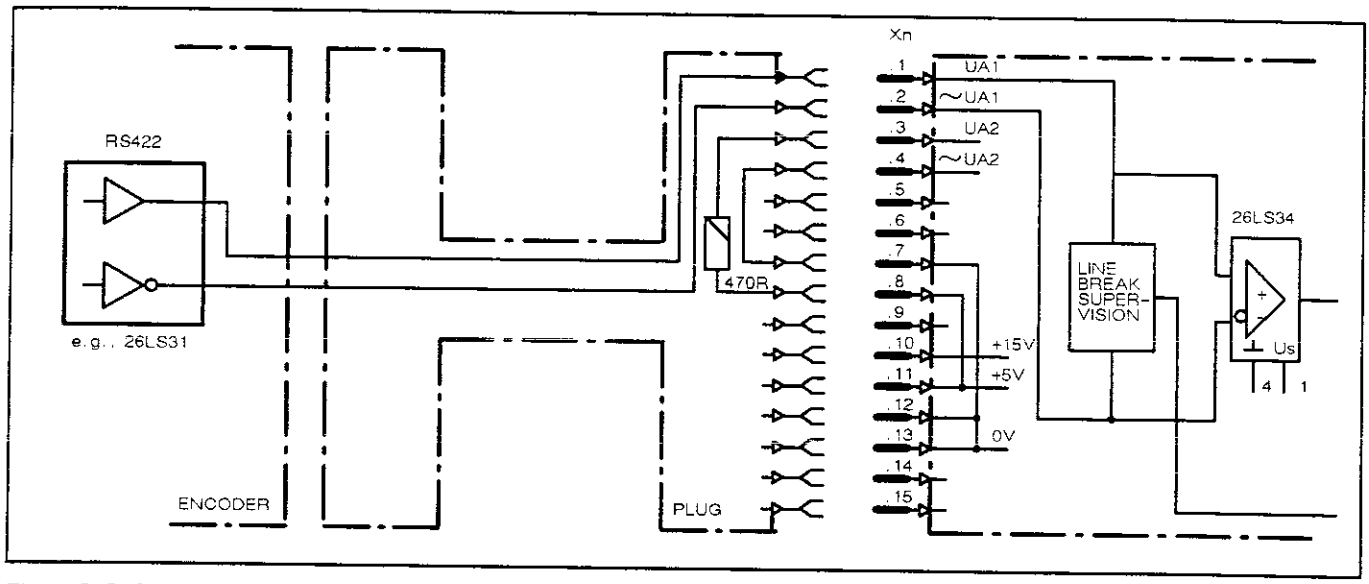


Fig. 10.2-6: Application of fast counters - no limits

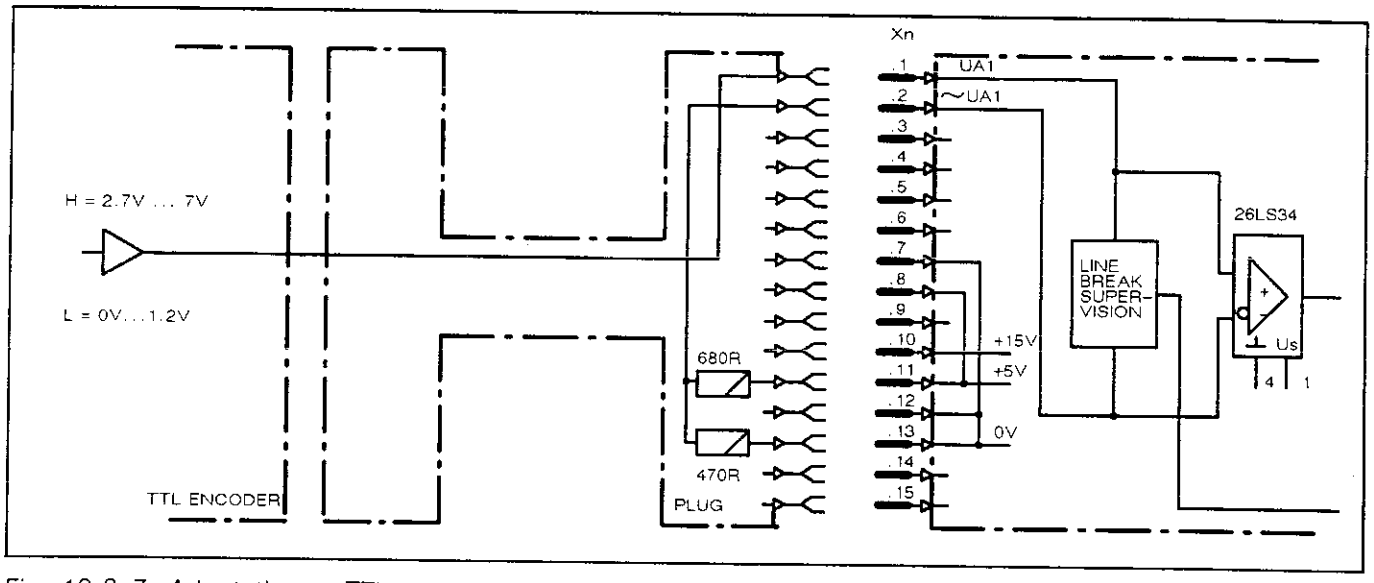


Fig. 10.2-7: Adaptation to TTL output - f $\leq$ 250 kHz, typical line supervision.

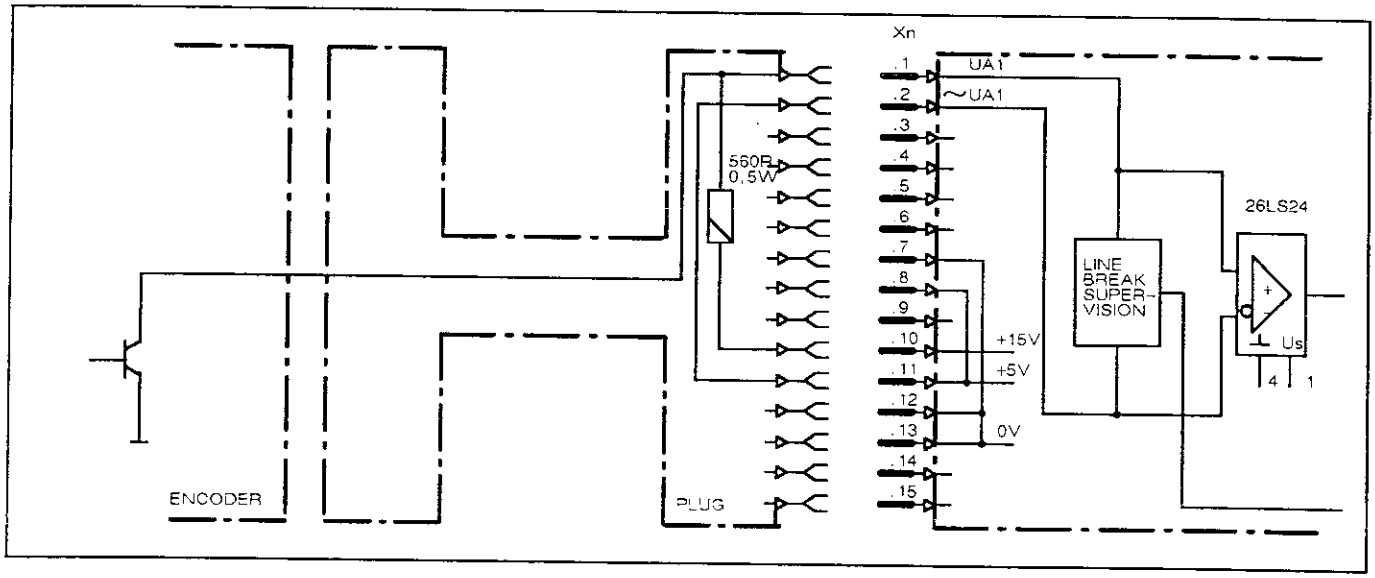


Fig. 10.2-8: Adaptation to open-collector - f $\leq$ 250 kHz, typical line supervision.

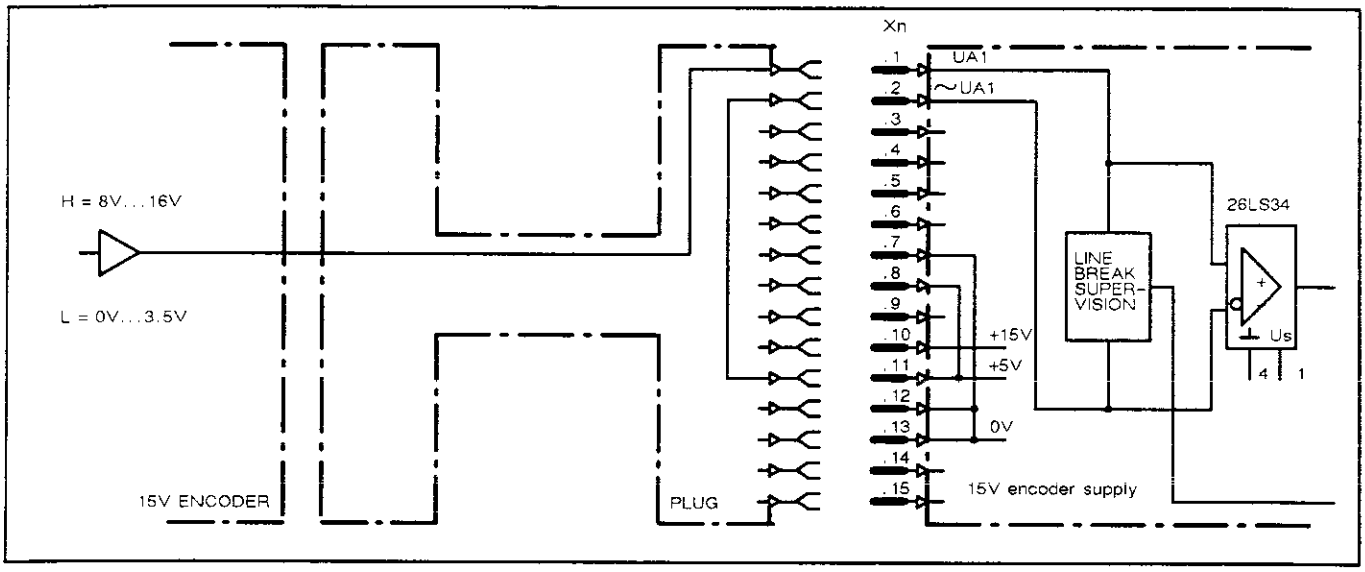


Fig. 10.2-9: 15 V output – f $\leq$ 250 kHz, typical line supervision. Set the encoder supply to 15V

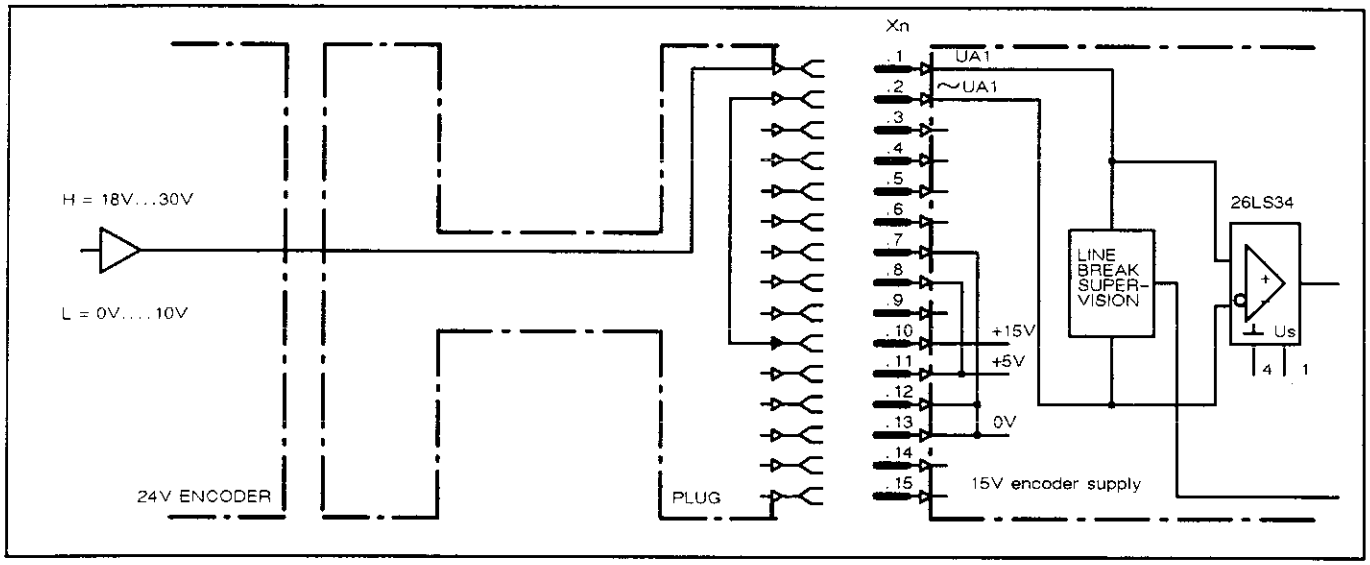


Fig. 2-10: 24 V output – f $\leq$ 250 kHz, typical line supervision. Set the encoder supply to 15V

Adapatation of the zero track Uao

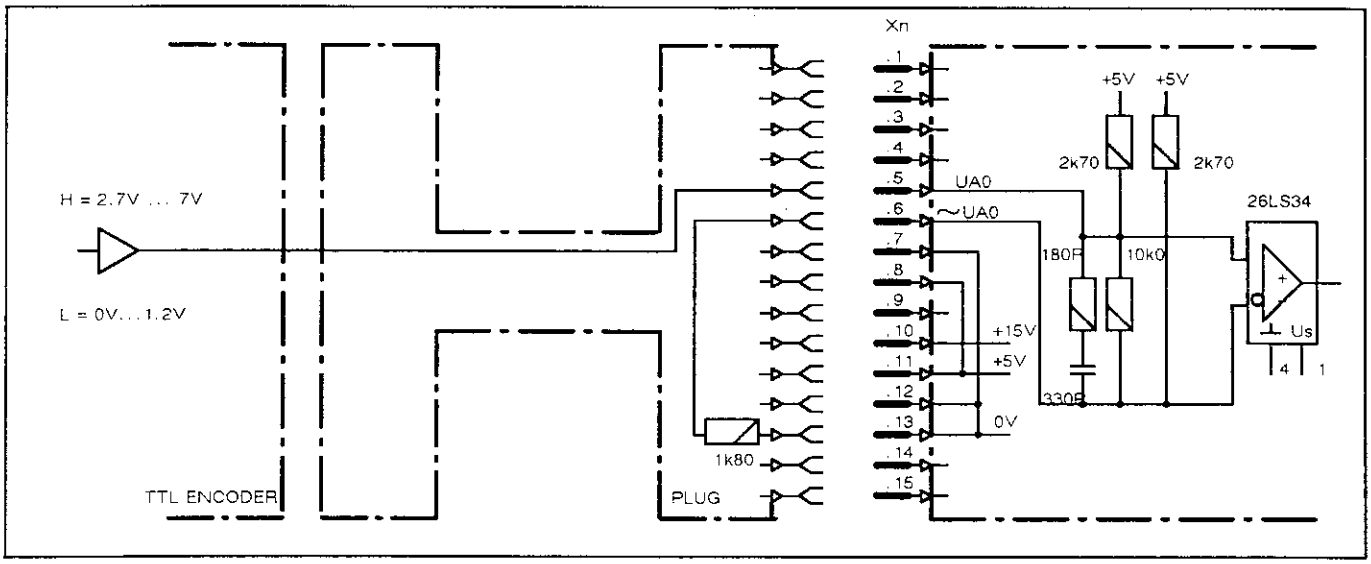


Fig. 10.2-11: Adaptation to TTL output – frequency f according to data sheet

Proceed as for fig. 10.2-8 when using an open collector output, whereby Uao does not have to be connected

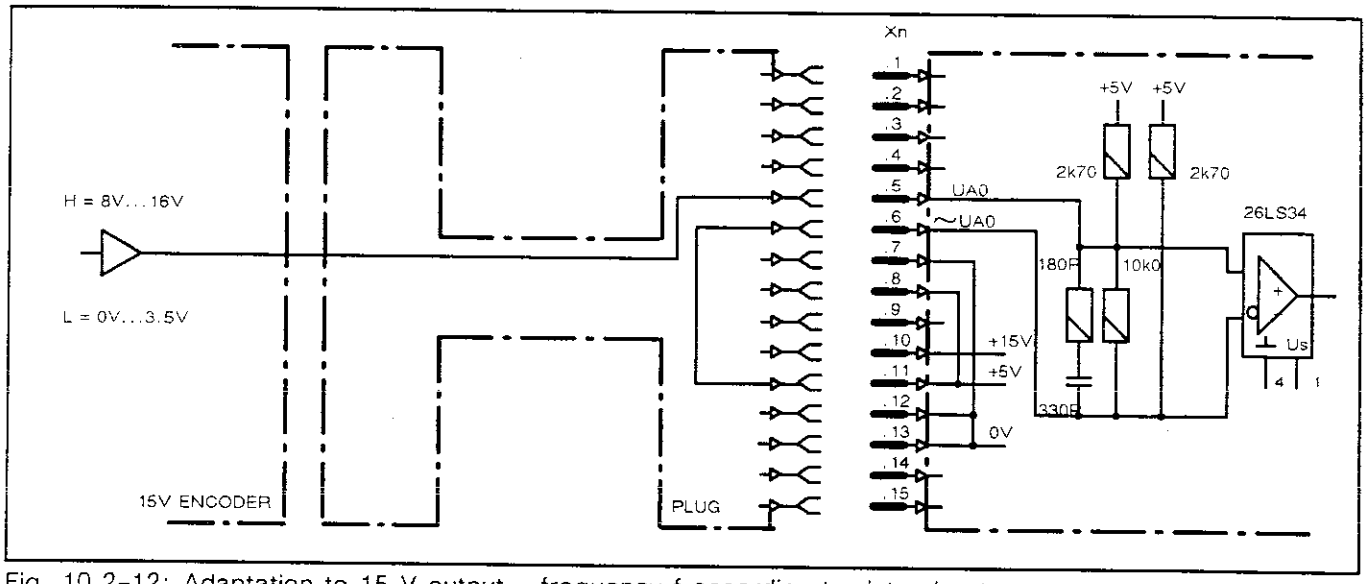


Fig. 10.2-12: Adaptation to 15 V output - frequency f according to data sheet

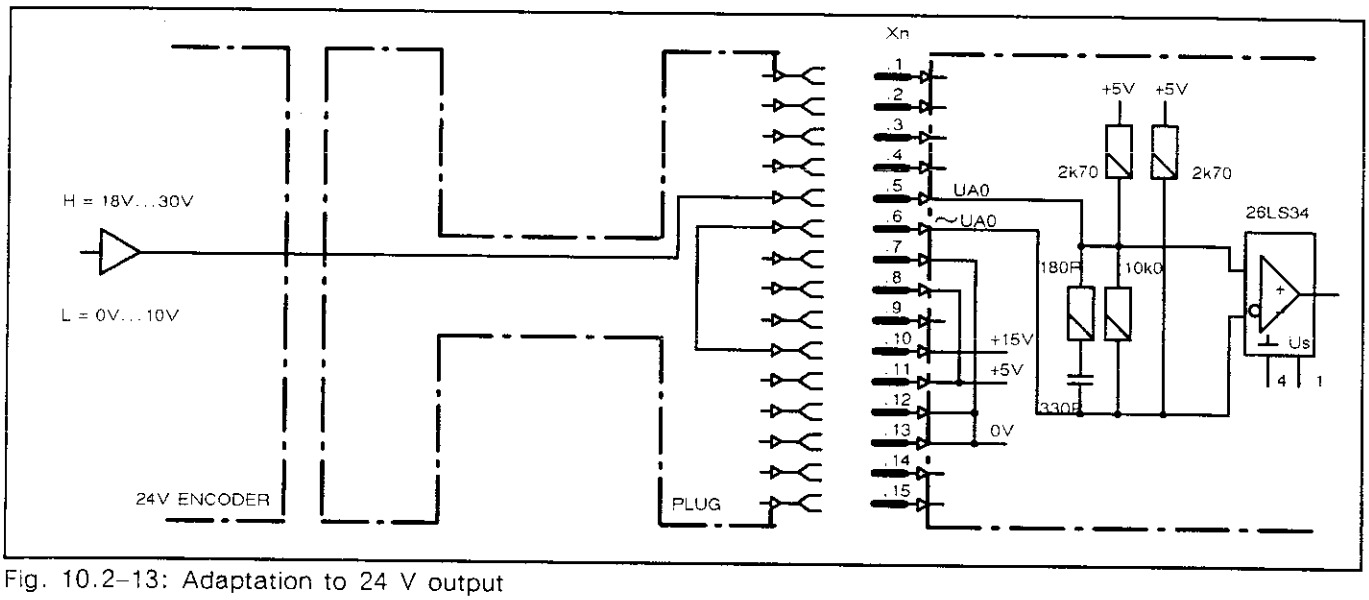


Fig. 10.2-13: Adaptation to 24 V output

Illustration of the RS422 interface

Fig. 10.2-14 ... 16:
Illustration of an RS422 interface to increase the immunity to interference. No limits for Fig. 10.2-14 and Fig. 10.2-15. F $\leq$ 250 kHz for fig. 10.2-15.

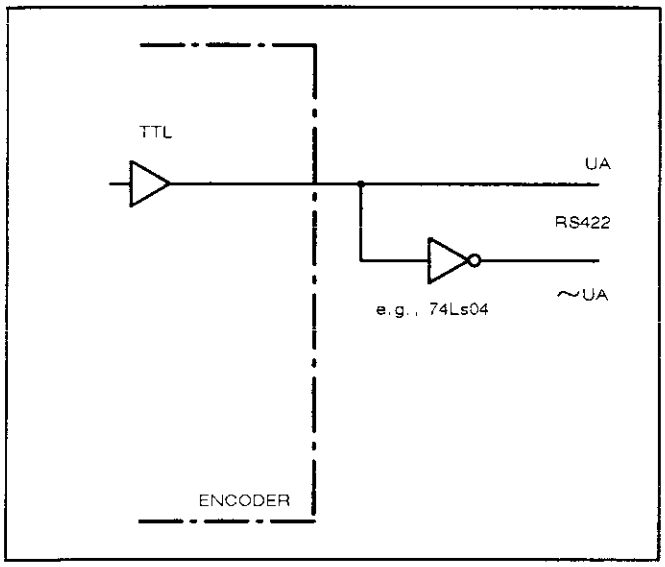


Fig. 10.2-14: TTL - RS422 conversion

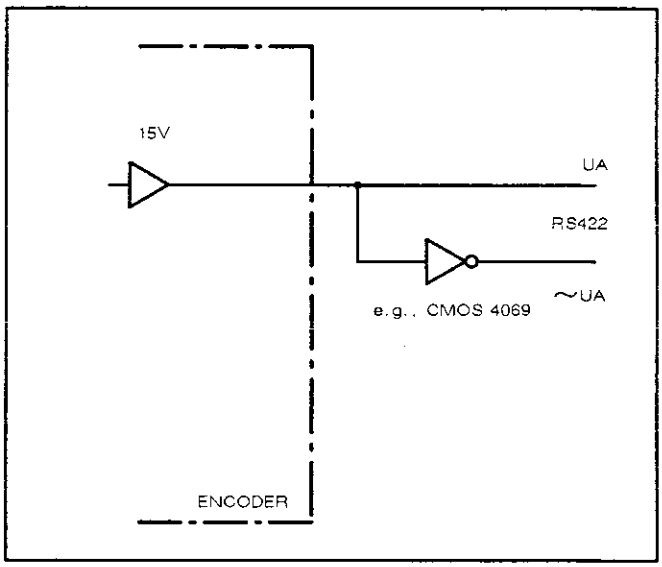


Fig. 10.2-15: 15 V logic - RS422 conversion

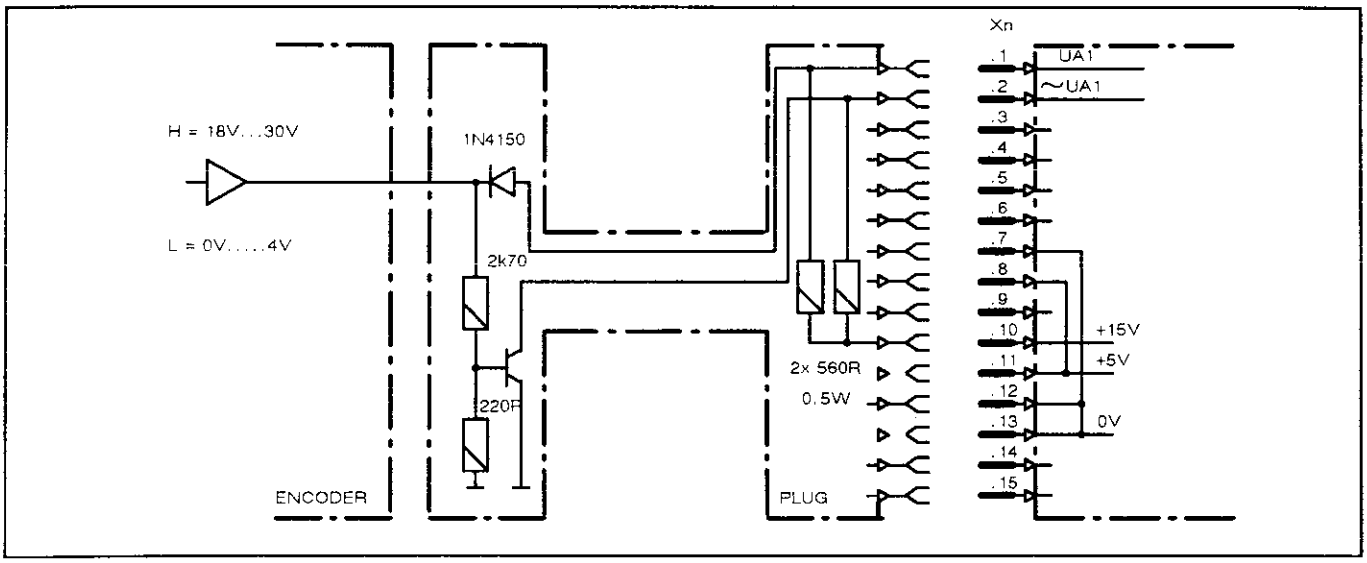


Fig. 10.2-16: 24 V logic - RS422 conversion

10.2.8.11 Differences between rubric 1,2 and rubric 4,5

The table is valid for the rubrics 1 and 2 starting from the alteration index "c".

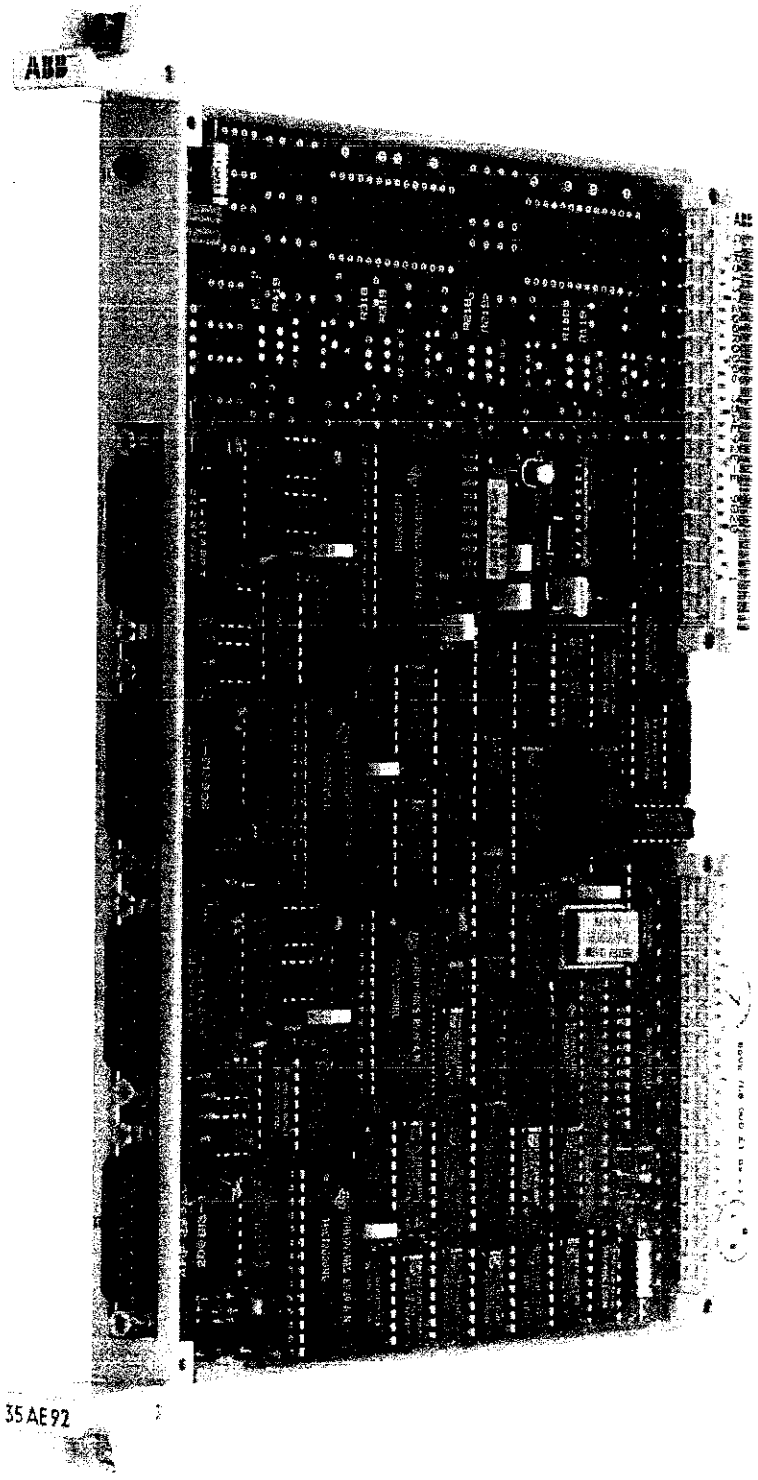
Comment	rubric 1/2	rubric 4/5
IB2	0.1 A/0,15 A	0.06 A/0.1 A
IB3	0.1 A/0,15 A	0.06 A/0.1 A
Pulse width U_{a0} *1	5 µs	5 µs
Input frequency U_{a0} *1	20 kHz	20 kHz
D/A converter IC/axis	1 item	0.5 item
Zero point error (factory balancing)	< 10 mV	< 17 mV
Output voltage error (factory balancing)	< 10 mV	< 17 mV
Output voltage drift	< 15 mV	< 15 mV
Symmetry and linearity drift	< 4 mV	< 2 mV
Encoder switchover	no *2	yes *3
EMC improvement		yes

*1 Differences to the alteration indexes "a" and "b" can be requested from ABB.

*2 Adapting to an incremental encoder with a 15 V output level can only be carried out via an application.

*3 The encoder switchover is carried out in accordance with the data sheet by interrupting certain resistors.

10.3 Incremental input 35 AE 92 R6



90 05 16

10.3.1 Technical data

Axes	4
Encoder	Incremental 5 V/15 V with differential output RS 422
U_{B1} positive supply voltage	+ 5 V ± 5 %
I_{B1} supply current to U_{B1}	1.0 A ± 20 % plus I_{X3} ... I_{X6}
I_{X3} ... I_{X6} is the supply current taken from the plugs X3, X4, X5 and X6 to supply the external auxilliary logics and encoder lamps.	
Supply currents for the external logics for X3 ... X6:	
I_{tot} (U5) = I_I + I_5	Imax. 0.5 A/axis
I_{tot} (U15) = I_{15}	Imax. 0.3 A/axis (note the capacity of the ABB Procontic T300 power supply unit in the subrack)
Line length for external logics or path encoder:	
For I_{tot} = 0.3 A and A = 0.5 mm²	typically 10 m
Total power loss	5 W
Input values for path encoder signals:	
Input switch	according to RS 422
Common-mode rejection	max. + 25 V
Differential input voltage	max. 7 V with 5 V encoders/ 16 V with 15 V encoders
Differential input high threshold	max. + 0.2 V
Differential input low threshold	max. – 0.2 V
Line terminator RC element (5 V / 15 V)	R typically 300 Ω or 820 Ω C typically 330 pF
Input current, static	≤ 20 mA
dynamic	≤ 40 mA
Flank clearance (U_{a1} – U_{a2} with $f_{Inp.}$ = 1 MHz)	250 ns
Input frequency U_{a1}, U_{a2}	≤ 1 MHz
Pulse width U_{a0}	≥ 5 µs
Input frequency U_{a0}	≤ 20 kHz
Watchdog for reading the actual values:	
Time delay	typically 20 ms
Adjustable (assembly position 1001)	0.7 ... 150 ms
Touch probe input:	
Signal level: 0-signal	0 ... 1.2 V
1-signal	2.4 ... 30 V
Input current	≤ 2 mA
Delay tv	400 ns
Exe interference signal $\overline{U_{as}}$:	
Signal level	TTL
Input current	≤ 0.5 mA
Delay tv	typically 50 µs
Ambient values:	
Ambient temperature	0 °C ... + 55 °C
Storage temperature	– 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Dimensions	1 pitch
Weight	1.0 kg
Order number:	GJR5137200R6

10.3.2 Description

The 35 AE 92 R6 incremental input is a passive subscriber on the MPST bus and designed for 4 incremental decodes. The incremental input mainly executes the following functions:

Reception and evaluation of the path encoder signals

- Path encoders, which supply square-wave pulse rows shifted in their phase by 90°, can be connected.
- Creation of path pulses in three phases and which are added in a 16 bit for-/backwards counter with overflow,without carry (0...0FFFFH...0...0FFFFH), in the direction discriminator.
- The actual value counter can be read by the MPST bus. Its level is not deleted during the reading procedure.
- Reception of the encoder zero pulses and deletion of the actual value counters for the reference pont movement, if the zero marks are reached.
- Deletion of the actual value counter with reset.

Measuring operating mode

- Possibility to connect a "touch probe". This creates a trigger pulse, which maintains the current counter level of all axes on the unit.
- Software creation of the touch trigger pulse for the simultaneous position determination of all 4 axes.

Diagnosis

- It can be read in one of the status bytes assigned to the respective axis, whether there is an encoder malfunction or an encoder line break or whether the "watchdog" has been addressed.
- Optical display "watchdog not addressed" by the LED H1.

Interfaces

- A 15-polar plug (X3 ... X6) is available on the front of the units to connect the path encoder, its supply (lamp and logic) and as a "touch probe" input.

Supervision

- Supervision of the actual value prompting by the MPST bus. If an adjustable time reference is not observed, the "watchdog" is addressed. It deletes the set values of all axes and is stored depending on the operating mode. It also controls the optical display H1 (watchdog active = LED (light emitting diode) H1 goes out) and sets a status bit. The message can be set to be saved or not.

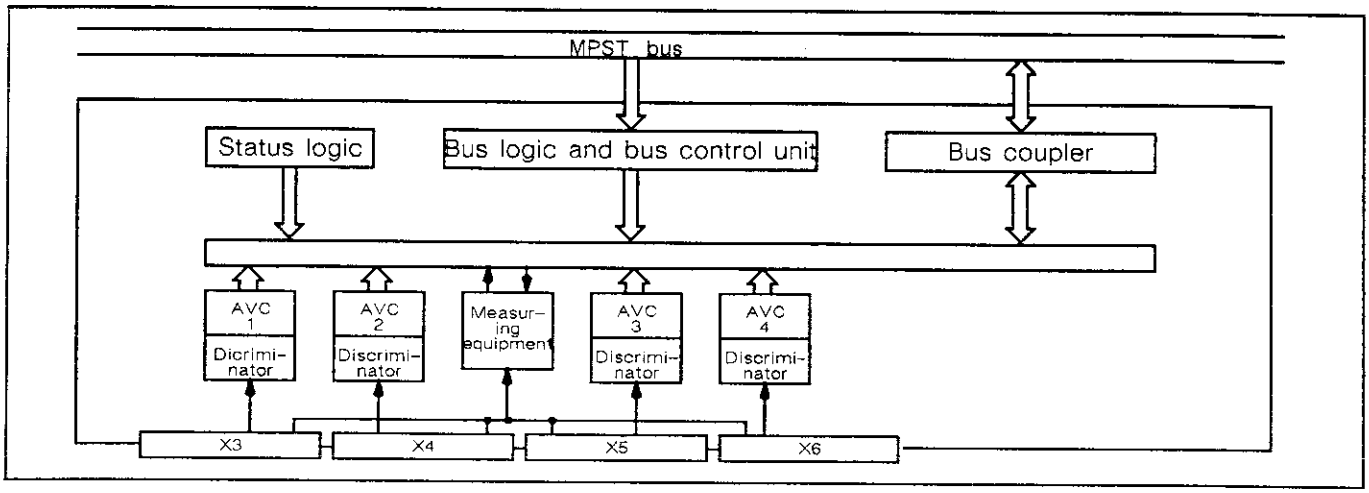


Fig. 10.3-1 Block diagram of the axis card 35 AE 92 R6

10.3.3 Mechanical structure

Unit in the double-size Eurocard format, 160 x 233.4 mm, 1 pitch.

Displays:
H1 operating display, watchdog is not addressed

Plug connectors:

X1, X2	32-polar bus interface according to DIN 41 612, part 2 design C
X3, X4, X5, X6	Encoder interface, plug connector AMP HDP 20, 15-polar

R124 and R125 or R224 and R225 or R324 and R325 or R424 and R425 are highly set 470 Ω resistors to adapt the encoder to the respective axis. These resistors are to be interrupted or removed when using encoders with an output voltage of 8 V ... 15 V.

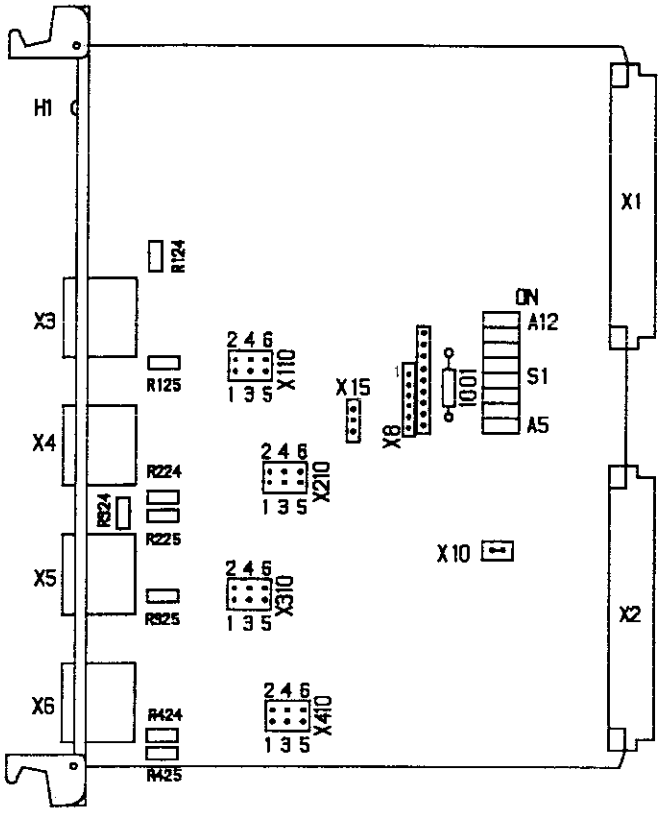


Bild 10.3-2 Component side (top view).

10.3.4 Plug assignment

10.3.4.1 MPST bus interface, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U_{B1}	5 V voltage	X1. 2c	U_{B1}	5 V voltage
X1. 4a	U_{B1}	5 V voltage	X1. 4c	U_{B1}	5 V voltage
X1. 6a	U_{B3}	- 15 V voltage	X1. 6c	U_{B2}	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	–	–	X1.24c	–	–
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{BOV}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	–	–	X2.22c	$\overline{RS}$	Reset
X2.24a	$\overline{W}$	Write	X2.24c	$\overline{R}$	Read
X2.26a	$\overline{I/O}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

10.3.4.2 Front plugs

Encoder interface for axis 1 (plug X3):

PIN	Signal name	Meaning
X3.1	Ua1	Encoder pulse 0°
X3.2	$\overline{Ua1}$	Encoder pulse 180°
X3.3	Ua2	Encoder pulse 90°
X3.4	$\overline{Ua2}$	Encoder pulse 270°
X3.5	Ua0	Zero pulse 0°
X3.6	$\overline{Ua0}$	Zero pulse 180°
X3.7	0 V	Ground lamp
X3.8	UL +	Lamp supply level + 5 V
X3.9	$\overline{Uas}$*	Exe interference signal
X3.10	U15	Logic supply level + 15 V
X3.11	U5	Logic supply level + 5 V
X3.12	0 V	0 V logic
X3.13	0 V	0 V logic
X3.14	UTT	Trigger touch probe
X3.15	–	Screen

Encoder interface for axis 3 (plug X5):

PIN	Signal name	Meaning
X5.1	Ua1	Encoder impulse 0°
X5.2	$\overline{Ua1}$	Encoder impulse 180°
X5.3	Ua2	Encoder impulse 90°
X5.4	$\overline{Ua2}$	Encoder impulse 270°
X5.5	Ua0	Zero pulse 0°
X5.6	$\overline{Ua0}$	Zero pulse 180°
X5.7	0 V	Ground lamp
X5.8	UL +	Lamp supply level + 5 V
X5.9	$\overline{Uas}$*	Exe interference signal
X5.10	U15	Logic supply level + 15 V
X5.11	U5	Logic supply level + 5 V
X5.12	0 V	0 V logic
X5.13	0 V	0 V logic
X5.14	UTT	Trigger touch probe
X5.15	–	Screen

Encoder interface for axis 2 (plug X4):

PIN	Signal name	Meaning
X4.1	Ua1	Encoder pulse 0°
X4.2	$\overline{Ua1}$	Encoder pulse 180°
X4.3	Ua2	Encoder pulse 90°
X4.4	$\overline{Ua2}$	Encoder pulse 270°
X4.5	Ua0	Zero pulse 0°
X4.6	$\overline{Ua0}$	Zero pulse 180°
X4.7	0 V	Ground lamp
X4.8	UL +	Lamp supply level + 5 V
X4.9	$\overline{Uas}$*	Exe interference level
X4.10	U15	Logic supply level + 15 V
X4.11	U5	Logic supply level + 5 V
X4.12	0 V	0 V logic
X4.13	0 V	0 V logic
X4.14	UTT	Trigger touch probe
X4.15	–	Screen

Encoder interface for axis 4 (plug X6):

PIN	Signal name	Meaning
X6.1	Ua1	Encoder impulse 0°
X6.2	$\overline{Ua1}$	Encoder impulse 180°
X6.3	Ua2	Encoder impulse 90°
X6.4	$\overline{Ua2}$	Encoder impulse 270°
X6.5	Ua0	Zero pulse 0°
X6.6	$\overline{Ua0}$	Zero pulse 180°
X6.7	0 V	Ground lamp
X6.8	UL +	Lamp supply level + 5 V
X6.9	$\overline{Uas}$*	Exe interference signal
X6.10	U15	Logic supply level + 15 V
X6.11	U5	Logic supply level + 5 V
X6.12	0 V	0 V logic
X6.13	0 V	0 V logic
X6.14	UTT	Trigger-Touch-Probe
X6.15	–	Sreen

* If the Exe interference signal is not used, the corresponding input of the affected axis is to be switched to + 5 V.

10.3.5 Unit addresses on the MPST bus

10.3.5.1 Address division

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	0
MPST code of the upper, passive address area (perm. wired up)			Unit address for S1 on the axis card 35 AE 92 can be set (See also 10.3.7.1)								Axis selection		Selection of the operating mode		

10.3.5.2 Address overview

No.	Operating mode	Access	Address	Data
1	Status	R/W	XX**0H	D07...D00
	Actual value	Read	XX**2H	D15...D00
	Set value	Write	XX**4H	D15...D00
	Measuring value	R/W	XX**6H	D15...D00
2	Status	R/W	XX**8H	D07...D00
	Actual value	Read	XX**AH	D15...D00
	Set value	Write	XX**CH	D15...D00
	Measuring value	R/W	XX**EH	D15...D00
3	Status	R/W	XX *0H	D07...D00
	Actual value	Read	XX *2H	D15...D00
	Set value	Write	XX *4H	D15...D00
	Measuring value	R/W	XX *6H	D15...D00
4	Status	R/W	XX *8H	D07...D00
	Actual value	Read	XX *AH	D15...D00
	Set value	Write	XX *CH	D15...D00
	Measuring value	R/W	XX *EH	D15...D00

** Bit4 of address low byte must be set to 0.
* Bit 4 of address low byte must be set 1.

10.3.5.3 Assignment and function of the address bits A0 ... A4

Axis addresses		
Address bit	A04	A03
Axis 1	0	0
Axis 2	0	1
Axis 3	1	0
Axis 4	1	1

Operating modes selection			
Address bit	A02	A01	A00
Status	0	0	0
Actual value	0	1	0
Set value	1	0	0
Measuring value	1	1	0

10.3.6 Status byte

The separate bits of the status byte have the following meaning:

Bit	Function	active	write	read
D00	Reference point active	1	X	
D01	Reference point reached	1		X
D02	Touch probe activation	1	X	
D03	Measuring result ready	1		X
D04	Encoder malfunction	1		X
D05	Encoder line break Ua1	1		X
D06	Encoder line break Ua2	1		X
D07	Watchdog addressed	1		X

The status bits D0 and D2 cannot be read.

10.3.7 Settings

10.3.7.1 Setting the unit address

DIL switch **S1**:

Example for address E500

This unit fills the address area of E500 to E51E. The next unit would then receive the address E520.

10.3.7.2 Watchdog functions

Jumper zone **X8**:

Without jumpers The watchdog is only displayed, in the status byte (bit D7) and optically with the light emitting diode H1.
Jumpers 2–3 No function.
Jumpers 5–6 The watchdog interrupt is saved. A status bit to remove the storage function must first be written for the release (e.g., by activating the reference point movement). The actual value must then be read cyclically again, so that the watchdog remains active.

10.3.7.3 Setting the address time of the watchdog

t (ms) = 0.15 x R (kOhm)

Assembly position **1001**: R min. 4.7 kOhm
(Toleranz: ± 20 %) R max. 1 MOhm

10.3.7.4 Activating the touch trigger

Jumper zone **X15**:

Jumpers 1–2	Touch trigger	Activation by 1/0 edge
Jumpers 2–3	Touch trigger	Activation by 0/1 edge

10.3.7.5 Operating mode setting of the direction discriminators

Jumper zone **X110**: for axis 1
Jumper zone **X210**: for axis 2
Jumper zone **X310**: for axis 3
Jumper zone **X410**: for axis 4

Method of counting the jumper zones	2 4 6 1 3 5
Four-fold evaluation: (Jumpers 2–4)	o—o o o o o
Double evaluation of Ua1: (Jumpers 3–5)	o o o o o—o
Single evaluation of Ua1: (Jumpers 2–4, 3–5)	o—o o o o—o
Counter application:	o o o o o o

Jumper **X10**: The oscillator jumper must always be inserted.

10.3.7.6 Path encoder interface for Ua1, Ua2 and Ua0

The input switch of the interface corresponds to RS 422 and is realised with the blocks SN 75 173/26 LS 34. The flank clearance t_F of the encoder amounts to 250 ns with an input frequency of 1 MHz.

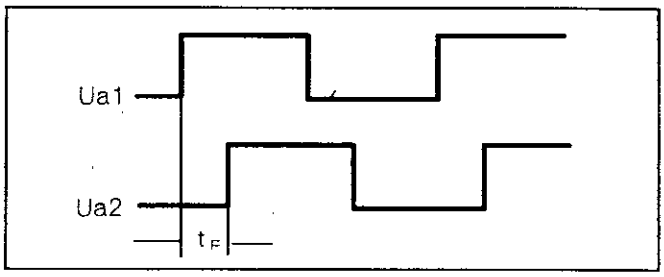


Fig. 10.3–3 Flank clearance t_F

10.3.7.7 Accuracy

Move to reference point

Actual value counter level with the zero pulse 0 ± 1 incr.

Reference point correction

The actual value counter in the individual axes is set to a basic value between ± 1 increment depending on the level of the signals Ua1 and Ua2 with a reset. The deletion of the actual value counters with the reference point movement occurs via the reset input. The position of the reference pulse Ua0 depends on the encoder used.

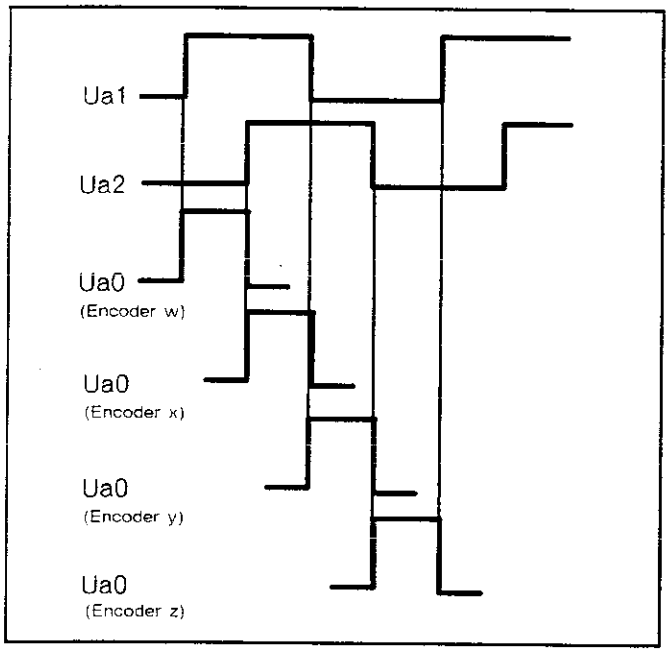


Fig. 10.3-4 Possible position of the reference pulse Ua0 (depending on the encoder)

Actual value counter level	– 1 incr.	0	+ 1 incr.	0
Encoder	w	x	y	z

Measuring accuracy:

The input delay of the UTT input through to the activation of the trigger pulse amounts to max. 400 ns and causes an error with the trigger activation depending on the jog speed.

Measuring error: max.1 increment

10.3.8 Application instructions

For the principle program examples, see chapters 10.3.8.7 and 10.3.8.8.

10.3.8.1 Card initialisation

a) The actual value counters of all the active axes must be read to initialise the direction discriminators.
b) If the watchdog is set to "saving" (jumper X8/5–6), a status byte must be written to activate the watchdog (this generally happens automatically with the reference point movement, which is necessary after switching on the supply voltage).
c) The watchdog is addressed each time the actual value of an axis is read.
d) A measuring value must be read to reset the measuring value logic.
e) The corresponding measuring values must be read to reset the measuring value register.

10.3.8.2 Measuring value function

Measuring movement activation

A measuring movement is activated by the data bit D2 for a cycle being written in the status register of any function with 1.

Touch trigger initialisation

All the actual value registers are blocked, when the touch trigger is reached, with a measuring movement. A release of the actual value register of an axis is carried out by reading the respective measuring value register. The measuring value can only be read out from the address for the actual value reading, while the measuring value of an axis was not read but without achieving a release of the actual value register. The corresponding status bit D3 of the axis is reset, when the measuring value is read. The measuring value registers of the non–relevant axes must also be read after a measuring movement in order to achieve the release for the actual value reading.

The measuring value logic can only be reactivated after a completed measuring movement, if at least one measuring value was read out. The contents of the measuring value registers, which have not been read out, are not altered with this new measuring movement.

Reading the measuring value does not reset the watchdog.

For the programming example for the measuring movement, see chapter 10.3.8.7.

Measuring movement reset

An already activated measuring movement can be deactivated by the software without initialising the touch trigger. This can be realised by reading any measuring value on the card, before the touch trigger pulse is emitted. A new measuring movement can then be started by setting D2 at a later point in time.

10.3.8.3 Switching on the touch probe

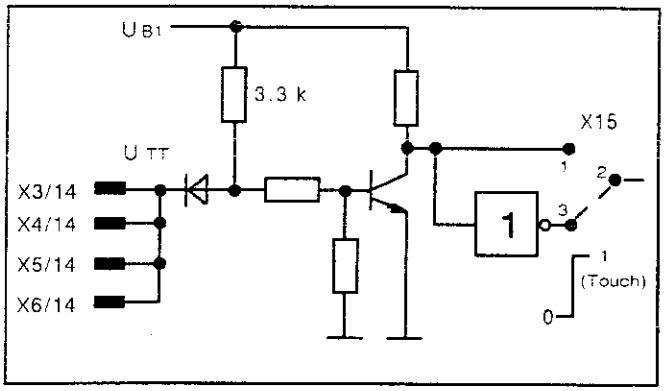


Fig. 10.3-5 Switch extract

Jumper X15	UTT signal	Touch
2 – 3	0 → 1	1 / 0
1 – 2	1 → 0	1 / 0

The signal level is decisive for activating the touch trigger. If the trigger is initialised immediately after its activation, either the incorrect initialisation characteristic is set for X 15 or the trigger signal is already active.

10.3.8.4 Exe interference signal

If the Exe interference signal is not used, the corresponding input $\overline{Uas}$ (Pin 9) of the affected access is to be bridged with + 5 V (Pin 8 or pin 11) in the HD plug.

10.3.8.5 Adapting the path encoder input to the 15 V encoders

To highly set resistors R = 470 Ω must be interrupted or removed per connected access (incremental encoder), if actual value encoders with 15 V outputs are used.

These include the following:

Axis 1	Axis 2	Axis 3	Axis 4
R124 R125	R224 R225	R324 R325	R424 R425

10.3.8.6 Counter application

Each functional unit can be used as a counter, if the jumpers are assigned according to 10.3.7.5. Switching the counter pulses is carried out via Ua1 (RS422). Ua2 (90°, Pin 3) must be switched with 470 Ω according to + 5 V (Pin 8 or Pin 11) and Ua2 (270°, Pin 4) according to 0 V (Pins 7, 12, 13 or pin 15) in the HD plug.

The reading out procedure is carried out via the function "reading the actual value". The counter contents are deleted, when the counter is read.

The connection of Ua2 (90°) and Ua2 (270°) causes the counter release. A signal change to Ua2 (90°), e.g., open input or input for 0 V, stops the counter. It emerges from the stop mode only with the correct connection of Ua2 and reset. A reset of the counting block can also be created via Ua0 (move to reference point).

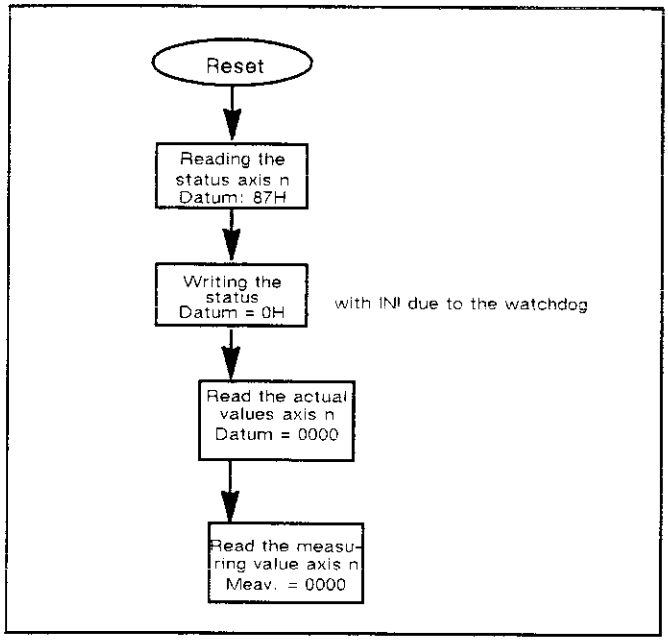
10.3.8.8 Flow diagrams

Principle examples for sequences. The flow diagrams were written in stages, i.e., the watchdog has been addressed.

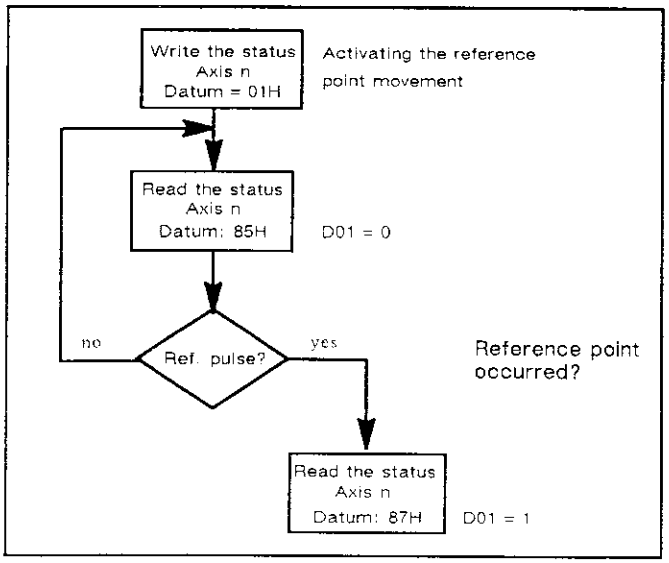
Abbreviations:

Actv.:	Actual value
Meav.:	Measuring value
D03:	Data bit 3
n:	as required (1...4)

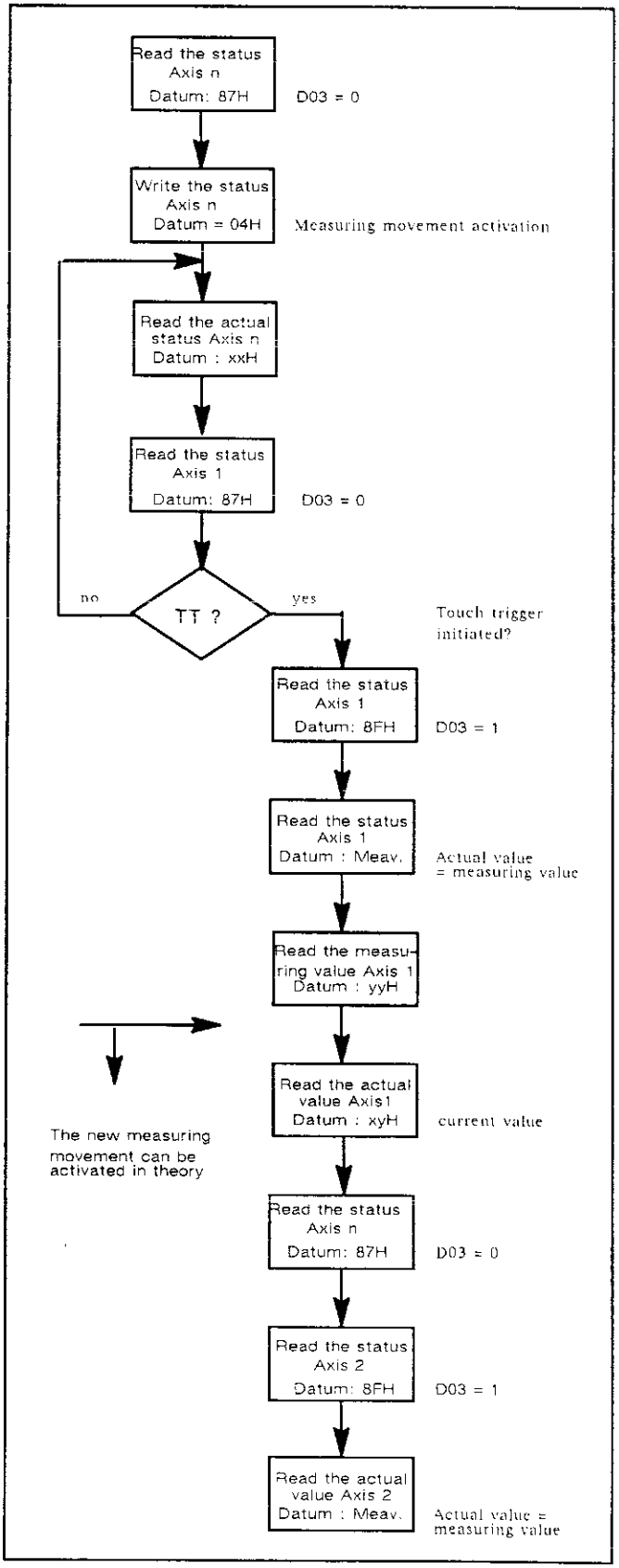
Reset/Initialisation



Move to reference point

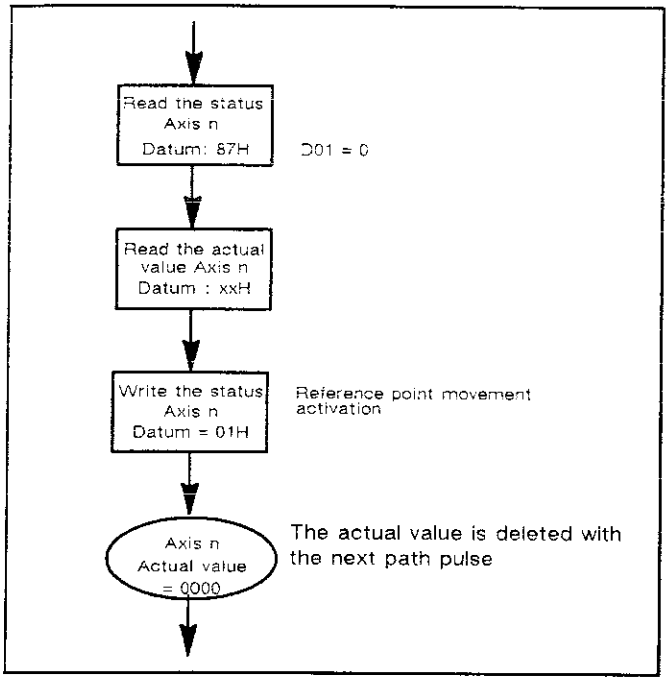


Measuring movement

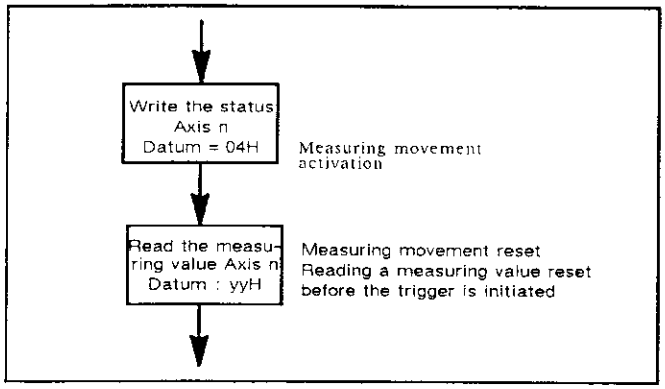


-Move to reference point immediately
-Deleting the actual value counter (cyclically)
-Direction discriminator reset

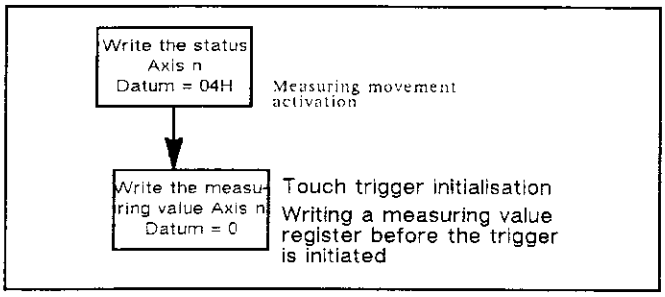
The Uao are to be connected with the inputs either from track A or track B to realise these applications. The limit frequency of Uao is to be observed with these applications!



Measuring movement deletion



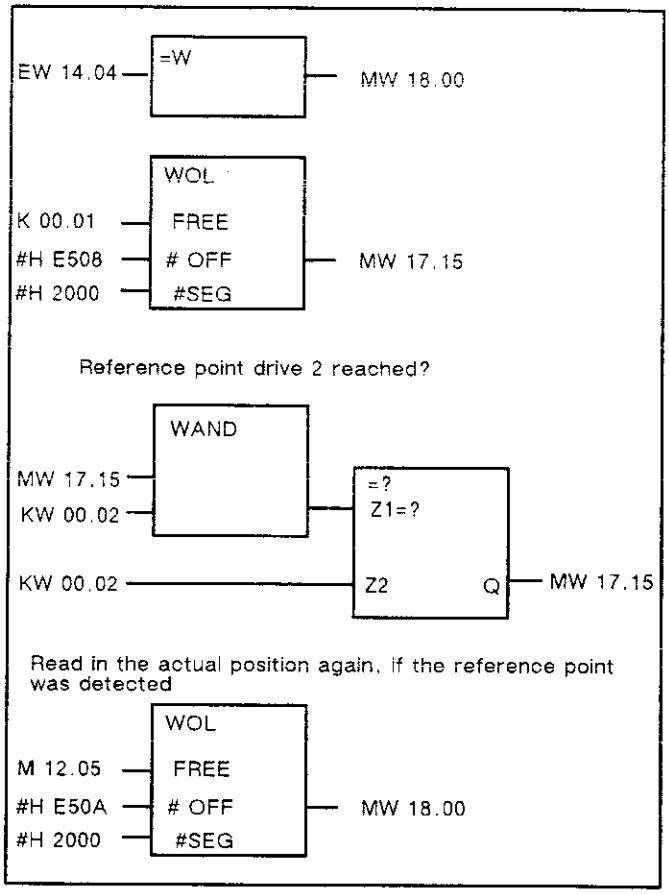
Touch Trigger by the software



10.3.8.9 Program extract 907 PC 31

Move to reference point

The actual value is to be read again after reaching the reference point and the old value deleted, so that plausibility or following errors do not occur after the move to the reference point due to the deleted actual value counter.



Variable:

EW	14.04	IPOS2_ON
K	00.01	TRUE
KW	00.02	TWO
M	12.05	REFSIGNAL2
MW	17.15	STATUS2
MW	18.00	RCTPOS2

10.3.8.10 Switch variants with path encoder interfaces

The path encoder interface is designed in accordance with RS422. The possibility exists of connecting other drivers with negligible switch measures in the cable plug as well. However, the transfer to another type of connection always brings certain limitations. The function of the line break supervision is ensured only. The maximum input frequency is reduced with some applications from 1 MHz to 250 kHz.

Adaptation of the path encoder tracks Ua1 and Ua2

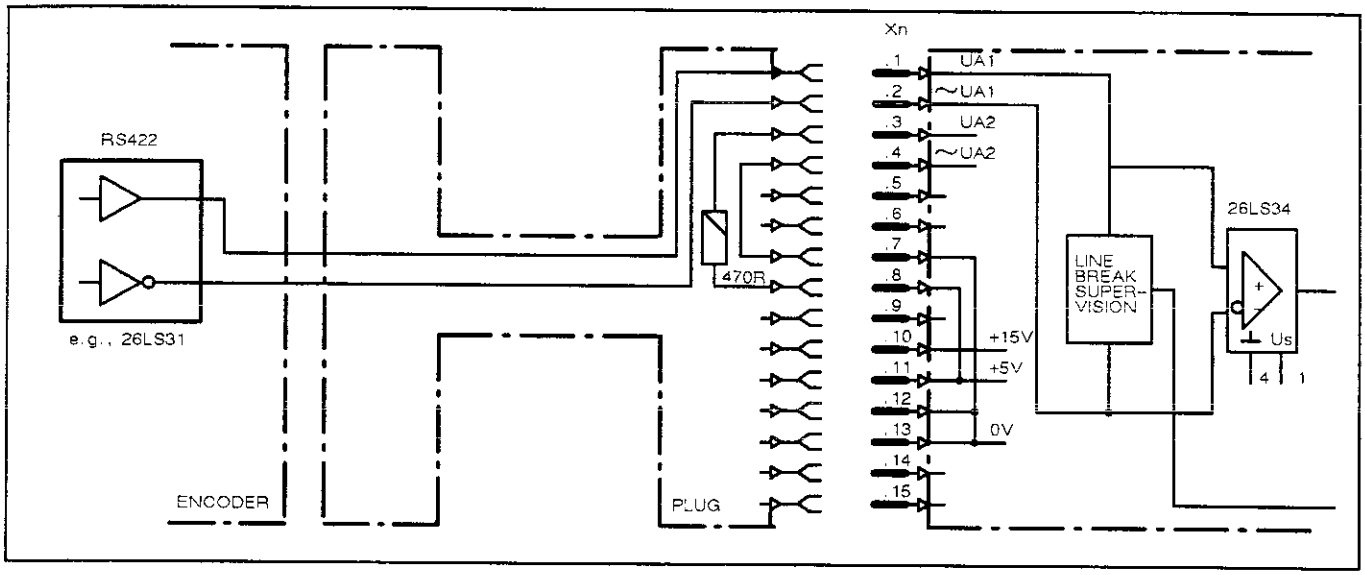


Fig. 10.3-6: Application of fast counters - no limits

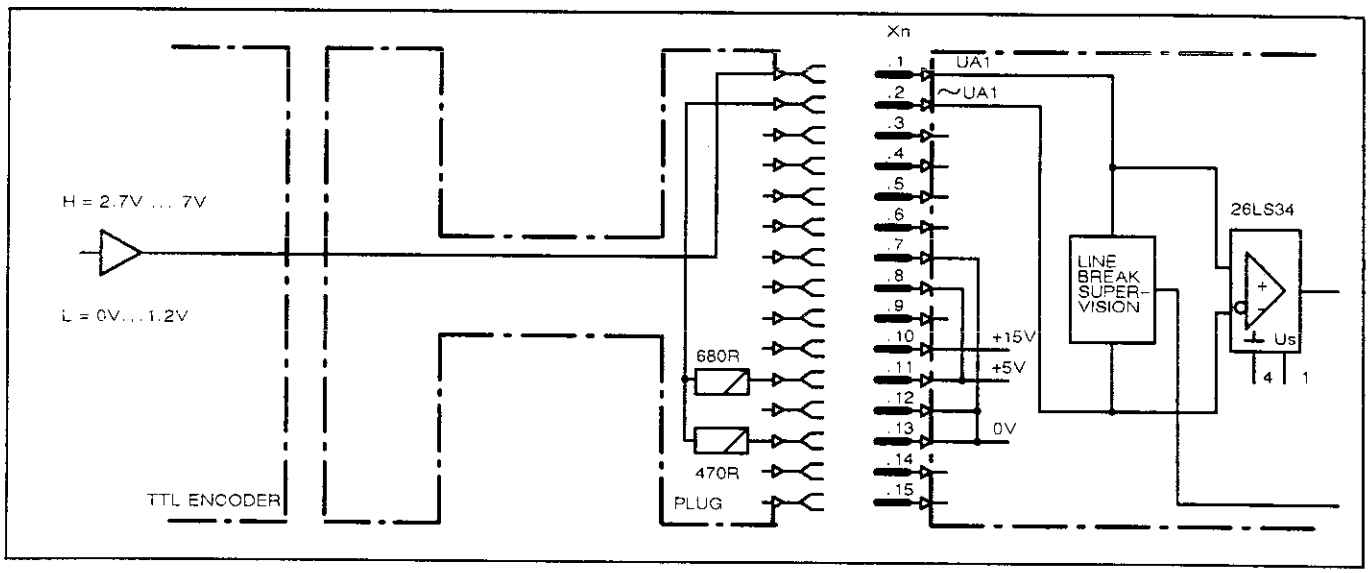


Fig. 10.3-7: Adaptation to TTL output - f $\leq$ 250 kHz, typical line supervision.

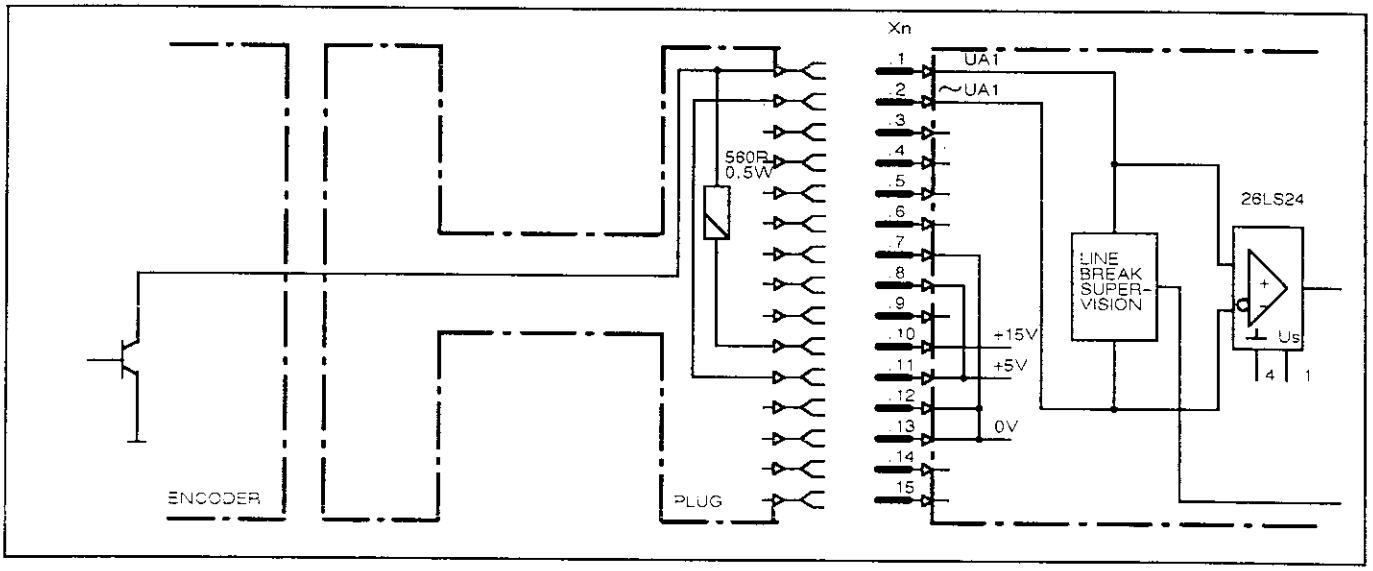


Fig. 10.3-8: Adaptation to open-collector - f $\leq$ 250 kHz, typical line supervision.

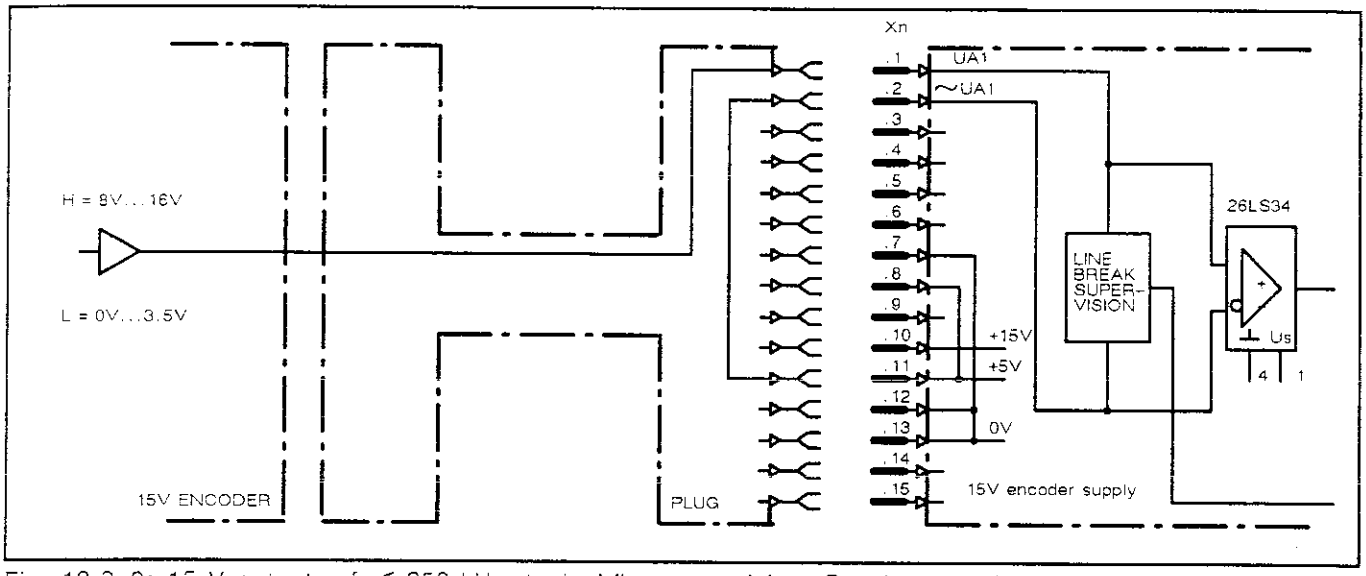


Fig. 10.3-9: 15 V output – f $\leq$ 250 kHz, typical line supervision. Set the encoder supply to 15V

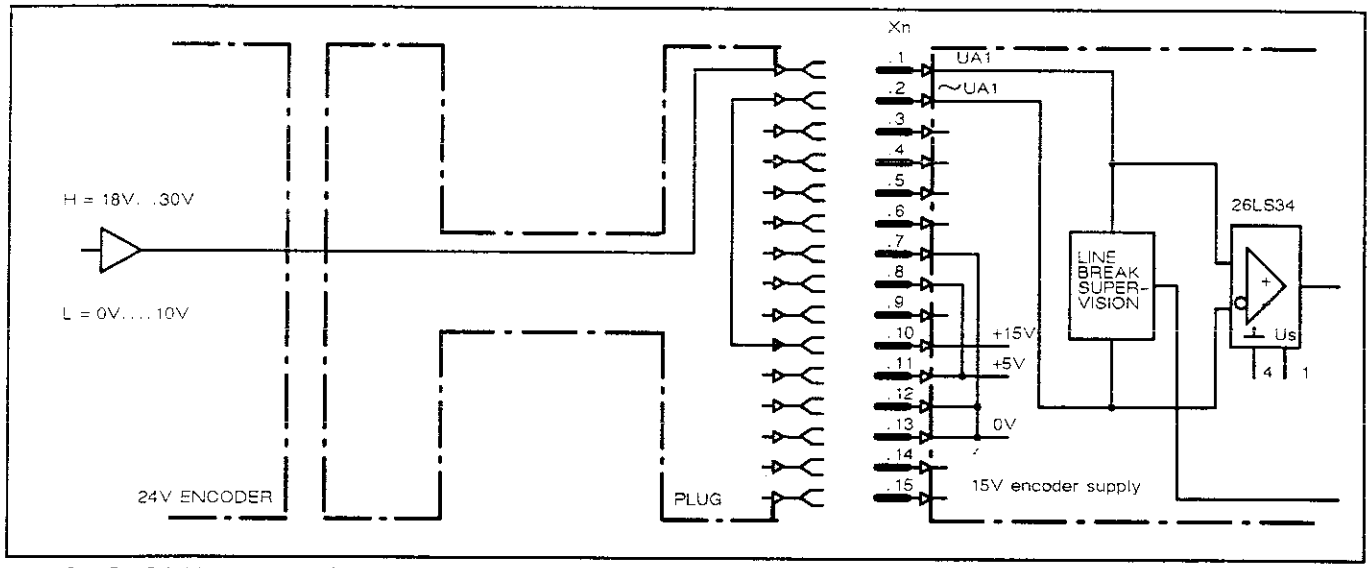


Fig. 2-10: 24 V output – f $\leq$ 250 kHz, typical line supervision. Set the encoder supply to 15V

Adapatation of the zero track Uao

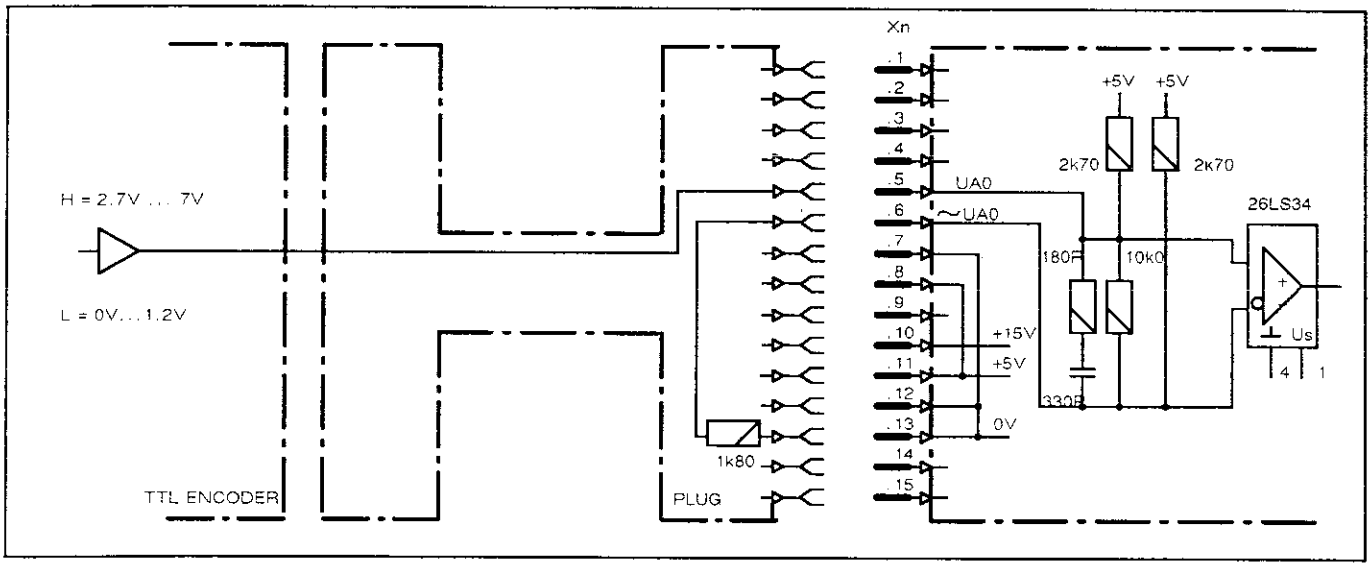


Fig. 10.3-11: Adaptation to TTL output – frequency f according to data sheet

Proceed as for Fig. 10.3-8 when using an open collector output, whereby $\overline{Uao}$ does not have to be connected

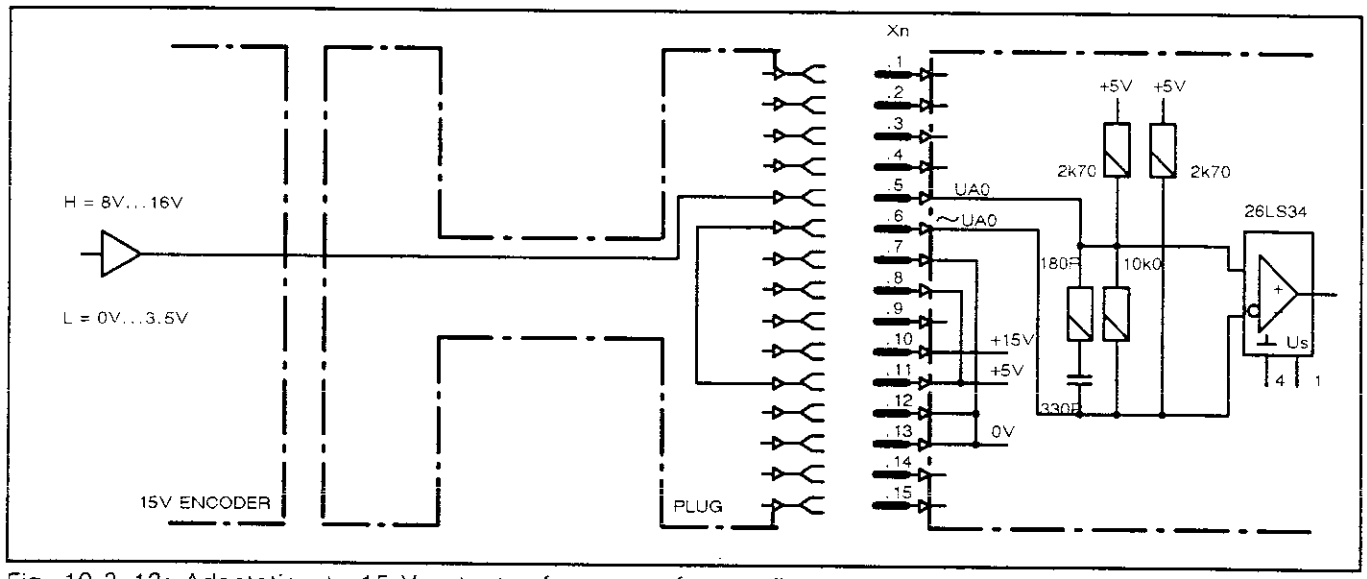


Fig. 10.3-12: Adaptation to 15 V output – frequency f according to data sheet

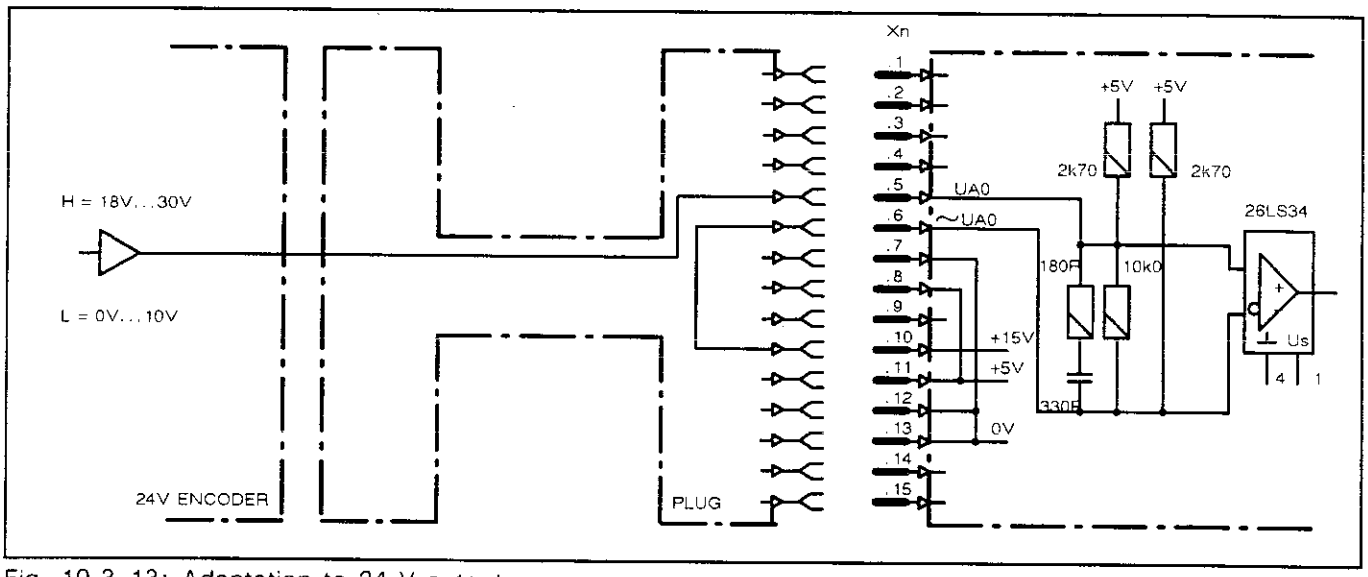


Fig. 10.3-13: Adaptation to 24 V output

Illustration of the RS422 interface

Fig. 10.3-14 ... 16:
Illustration of an RS422 interface to increase the immunity to interference. No limits for Fig. 10.3-14 and Fig. 10.3-15. F $\leq$ 250 kHz for Fig. 10.3-15.

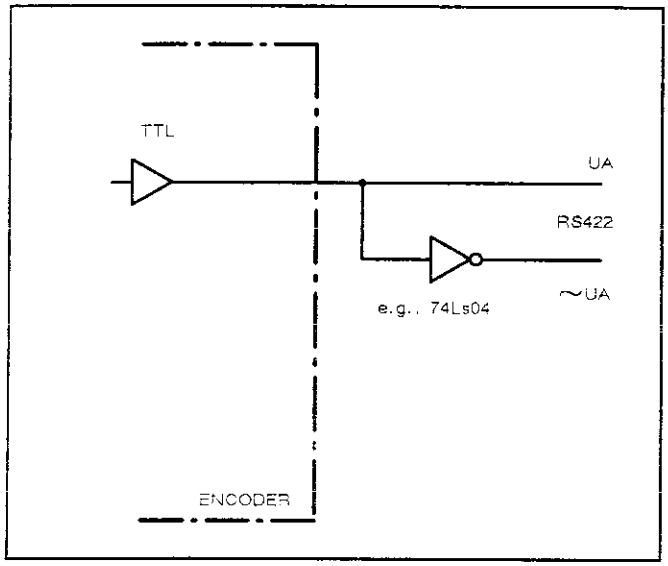


Fig. 10.3-14: TTL - RS422 conversion

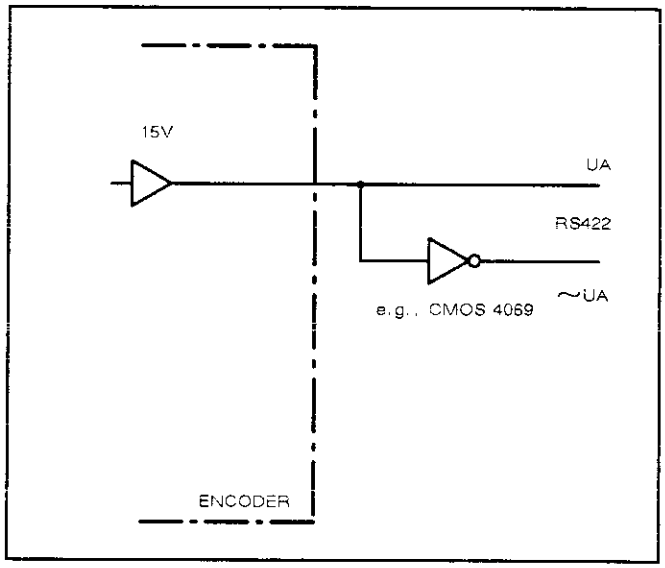


Fig. 10.3-15: 15 V logic - RS422 conversion

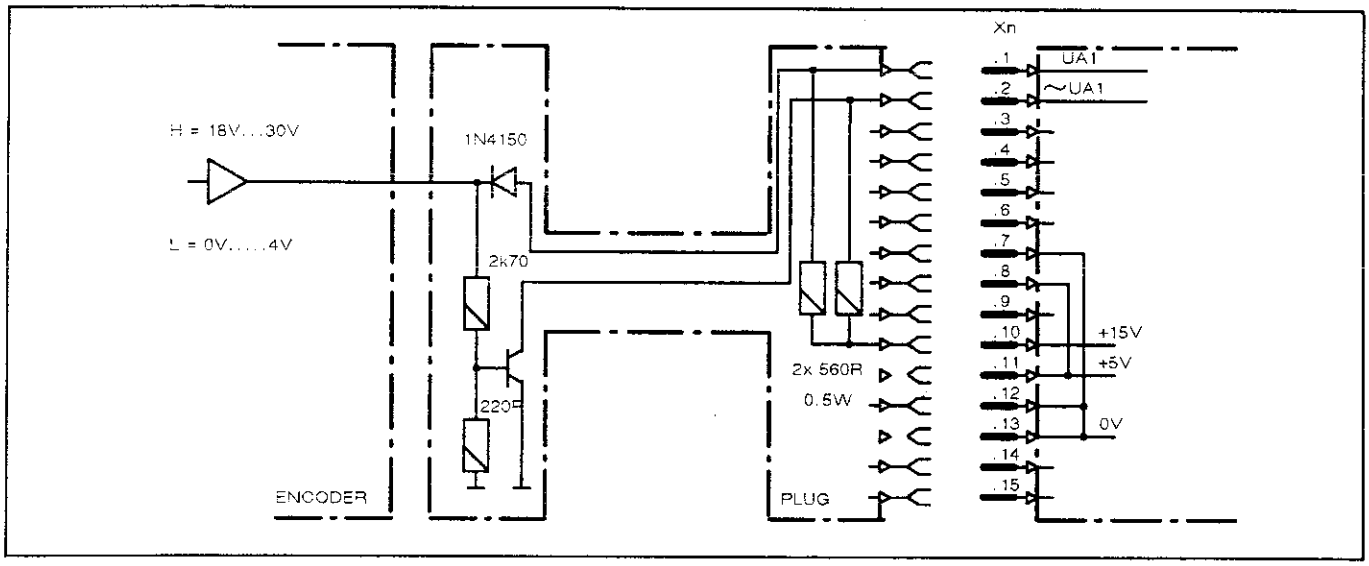


Fig. 10.3-16: 24 V logic - RS422 conversion

11 IR central units

35 IR 93 R101: Industrial computer *in preparation.*

11.1 *in preparation*

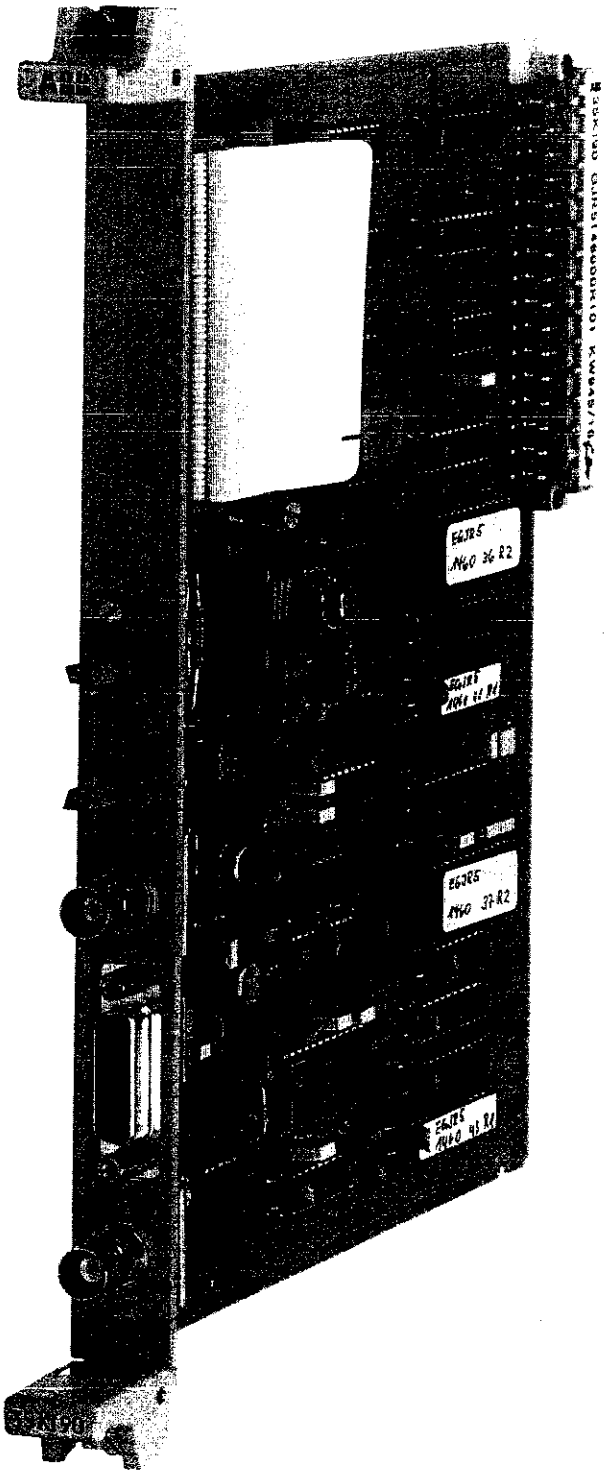
12 Opto-electrical measuring and sensor system, OMS-F

35 KI 90: Camera interface.
35 IV 90 R101: Iconic processor.

12.1 Camera interface 35 KI 90 ..... 12.1- 1
12.1.1 Technical data 12.1- 2
12.1.2 Description 12.1- 3

12.2 Iconic processor 35 IV 90 R101 ..... 12.2- 1
12.2.1 Technical data 12.2- 2
12.2.2 Description 12.2- 3

12.1 Camera interface 35 KI 90



90 07 07

12.1.1 Technical data

Supply voltages	
Supply voltage U_{B1}	+ 5 V ± 5%
Supply voltage U_{B2}	+ 15 V ± 5%
Supply voltage U_{B3}	- 15 V ± 5%
Supply currents (without camera, without monitor)	
I_{B1} for U_{B1}	typically 0.9 A, max. 1.5 A
I_{B2} for U_{B2}	typically 30 mA, max. 50 mA
I_{B3} for U_{B3}	typically 40 mA, max. 60 mA
Ambient values	
Ambient temperature	0 ... 55 °C
Storage temperature	- 25 ... + 75 °C
Humidity rating	F
Mechanical stress	VDE 160 when installed
Input values	
Local bus	TTL signals
Synchronising bus	TTL signals
Camera input	BNC socket or D 15 female connector
Plug-and-socket connection	BNC socket / 75 Ohm
Input resistance	75 Ohm
Input signal	BAS signal , max. 1.1 Vss
Standard	CCIR (Europe)
Output values	
Local bus	TTL signals
Current supply for the camera	TTL signals
Camera synchronisation	+ 12 V ± 1 V, max. 500 mA
Camera synchronisation	TTL signals
Monitor output	
Plug-and-socket connection	BNC socket / 75 Ohm
Output resistance	75 Ohm
Output resistance	Positive BAS signal, max. 1.1 V_{SS}
Standard	CCIR (Europa)
Dimensions	1 pitch
Weight	0.35 kg

Order number

35 KI 90 R101 for 8 MHz	GJR5146000R101
35 KI 90 R202 for 10 MHz	GJR5146000R202
35 KI 90 R111 for 8 MHz	GJR5146000R111
35 KI 90 R212 for 10 MHz	GJR5146000R212

12.1.2 Description

The 35 KI 90 camera interface forms a basic unit in the ABB Procontic T300 system together with the 35 IV 90 iconic processor. It includes the interfaces to the CCD surface camera, to a black/white image monitor, to a local bus (video and control bus) and to a synchronising bus. The control of the camera interface is carried out by the iconic processor 35 IP 90 via the local bus. The camera interface can be operated as a master or a slave unit by reprogramming the plug-in jumpers. A master camera interface can synchronise several slave camera interfaces via the synchronising bus.

The camera interface 35 KI 90 mainly has the following tasks:

- Creation of the synchronising signals (video generator)
- Control (synchronisation) of a camera
- Control (synchronisation) of a monitor
- Creation of a binary image
- Creation of a digital image with grey shades
- Synchronisation of a slave camera interface

A detailed functional description of the video sensor, OMS-F (camera interface + iconic processor) can be ordered under the order number GATS131510R2001.

Note: Differences between the rubrics R101, R202, R111 and R212

Rubric R101:
- 16 MHz quartz
- without a C synchronisation signal on plug X5

Rubric R202:
- 20 MHz quartz
- without a C synchronisation signal on plug X5

Rubric R111:
- 16 MHz quartz
- with a C synchronisation signal on plug X5

Rubric R212:
- 20 MHz quartz
- with a C synchronisation signal on plug X5

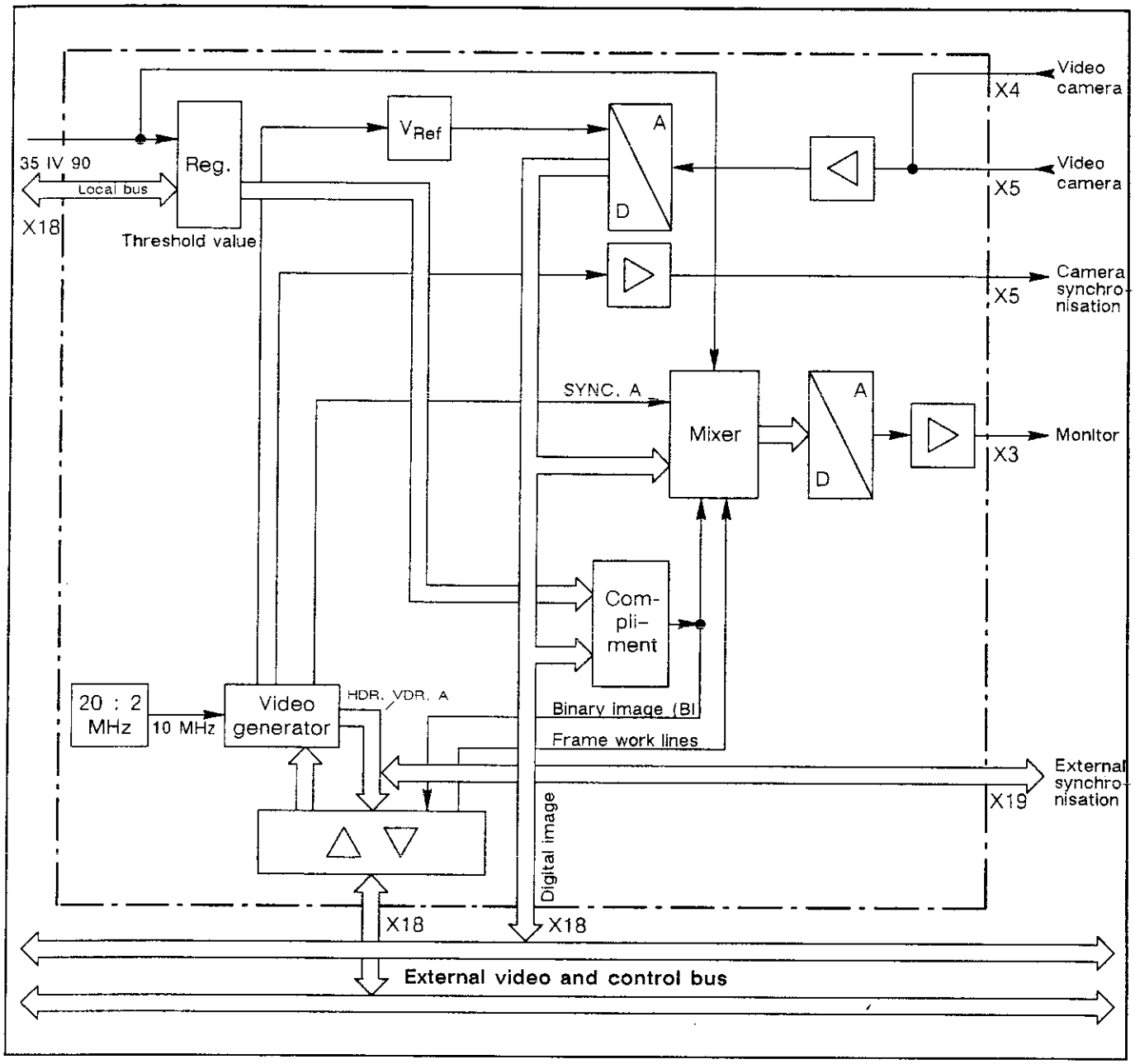
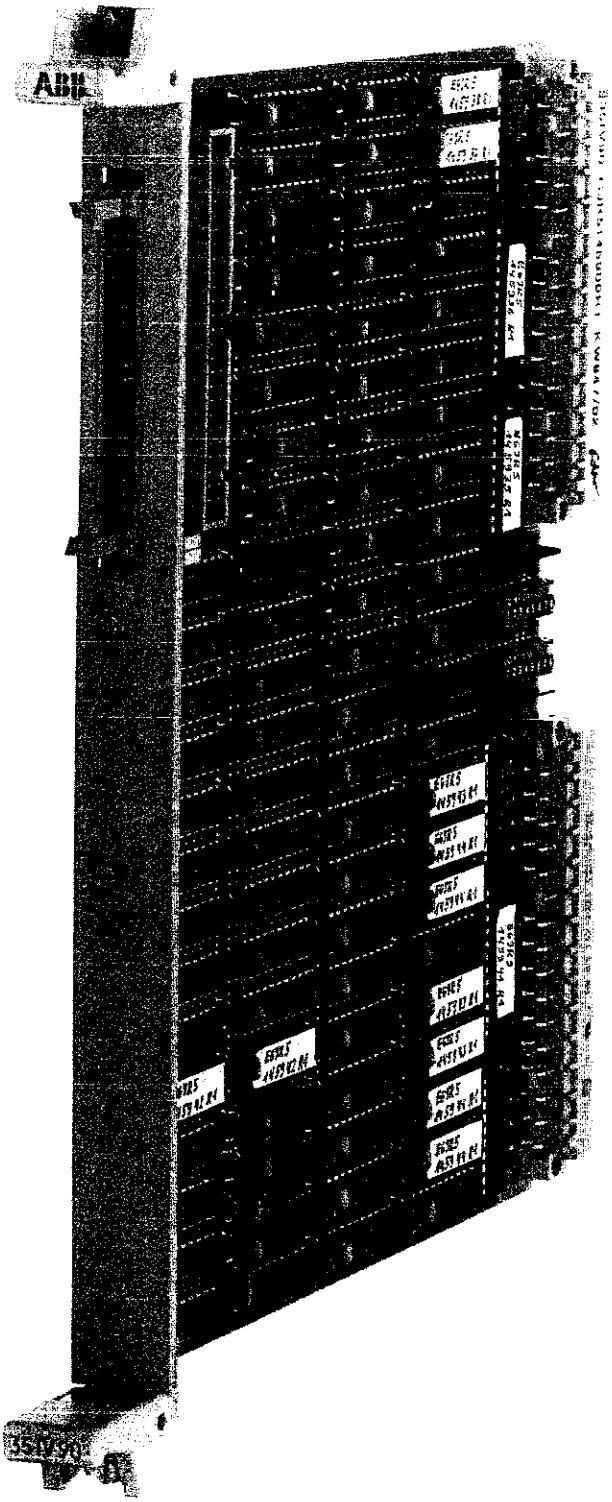


Fig. 12.1-1: Block diagram of the 35 KI 90 R212 camera interface.

12.2 Iconic processor 35 IV 90 R101



90 07 09

12.2.1 Technical data

Supply voltages	
Supply voltage U_{B1}	+ 5 V ± 5%
Supply voltage U_{B2}	+ 15 V ± 5%
Supply voltage U_{B3}	− 15 V ± 5%
Supply currents (without 35 KI 90)	
I_{B1} for U_{B1}	typically 2.9 A, max. 3.5 A
Ambient values	
Ambient temperature	0 ... 55 °C
Storage temperature	− 25 ... + 75 °C
Humidity rating	F
Mechanical stress	VDE 160 when installed
Input values	
Local bus (X 30)	TTL signals
Video bus (X 40)	TTL signals
Output values	
Local bus (X 30)	TTL signals
Video bus (X 40)	TTL signals
Dimensions	1 pitch
Weight	0.4 kg
Order number for	
35 IV 90 R1	GJR5145900R1

12.2.2 Description

As an intelligent input unit the 35 IV 90 iconic processor prepares the image data of the 35 KI 90 camera interface fast using its hardware. A central unit on the MPST bus controls the iconic processor. It includes the interfaces to the 35 KI 90 camera interface (local bus) and to other 35 IV 90 iconic processors (video and control bus).

The 35 IV 90 iconic processor mainly has the following tasks:

- Control of the 35 KI 90 camera interface
- Control of other iconic processors (slaves)
- Control of a possible image memory
- Evaluation of the digital image data
- Creation of 8 independently adjustable windows
- Creation of 8 window frame lines
- Surface contents determination within 8 independently adjustable windows
- Histogram compilation (compiling the rate of frequency of the grey shades) via 128 neutral steps
- Determining the moment of plain area in the X direction (Mx) or in the Y direction (My)
- Making the evaluated data available for the central unit. They are accessed via the MPST bus.

A detailed functional description of the video sensor, OMS-F (camera interface + iconic processor), can be ordered under the order number GATS131510R2001.

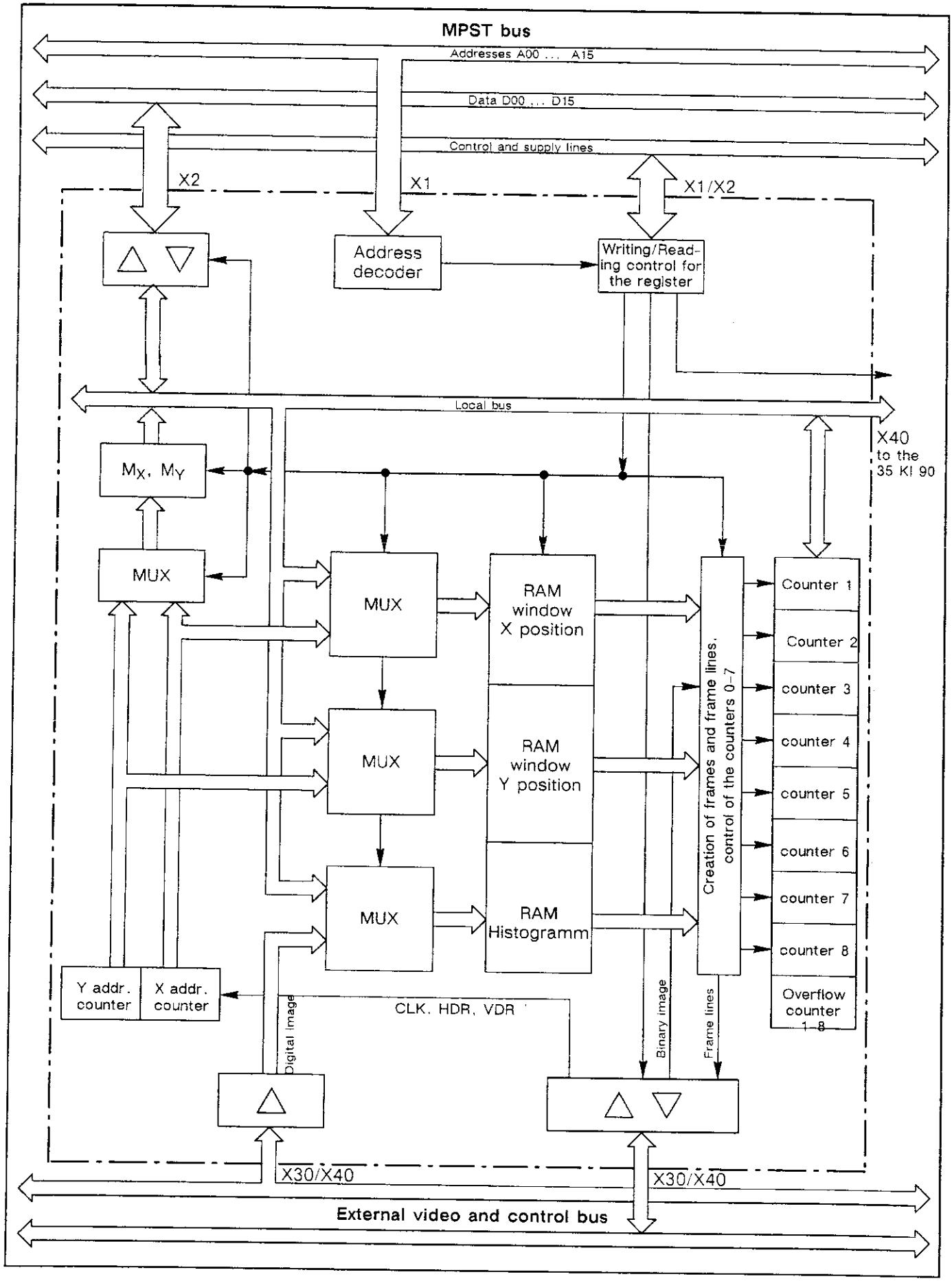


Bild 12.2-1: Block diagram of the iconic processors 35 IV 90

13 Binary input units

35 EB 90 R1:	Binary input unit,	24 V DC,	non-floating,	64-fold.
35 SK 90:	Flat system cable.			
07 EM 61 R1:	Input module,	24 V DC,	isolated,	8-fold.
35 EB 91 R1:	Binary input unit,	24 V DC,	non-floating,	32-fold.
35 EB 91 R2:	Binary input unit,	48 V DC,	non-floating,	32-fold.
35 EB 92 R1:	Binary input unit,	24 V DC,	isolated,	32-fold.
35 EB 92 R2:	Binary input unit,	48 V DC,	isolated,	32-fold.

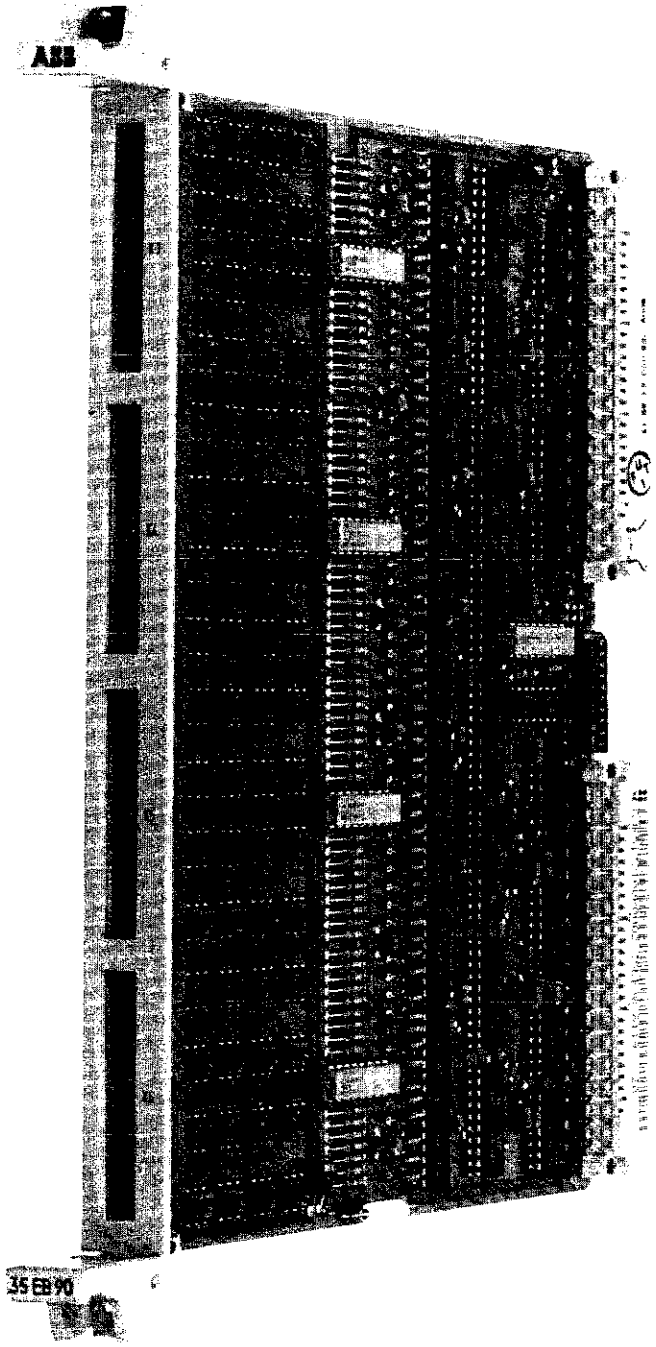
13.1 Binary input unit 35 EB 90 R1 ..... 13.1- 1
13.1.1 Technical data 13.1- 2
13.1.2 Description 13.1- 2
13.1.3 Mechanical structure 13.1- 2
13.1.4 Settings 13.1- 3

13.2 Cabels and input modules 13.2- 1
13.2.1 Flat system cable 35 SK 90 R* 13.2- 1
13.2.2 Input module 07 EM 61 R1 ... 13.2- 1

13.3 Binary input unit 35 EB 91 R1 and R2 ..... 13.3- 1
13.3.1 Technical data 13.3- 2
13.3.2 Description 13.3- 2
13.3.3 Unit addresses 13.3- 3
13.3.3.1 Address setting 13.3- 3
13.3.3.2 Address division 13.3- 3
13.3.3.3 Assembly positions 13.3- 3
13.3.4 Mechanical structure 13.3- 4
13.3.5 Pin assignment 13.3- 5
13.3.5.1 MPST bus interface, plug X1, X2 ..... 13.3- 5
13.3.5.2 Front plug X3 ..... 13.3- 6

13.4 Binary input unit 35 EB 92 R1 and R2 ..... 13.4- 1
13.4.1 Technical data 13.4- 2
13.4.2 Description 13.4- 3
13.4.3 Unit addresses 13.4- 3
13.4.3.1 Address settings 13.4- 3
13.4.3.2 Address division 13.4- 4
13.4.3.3 Interrupt vector setting 13.4- 4
13.4.3.4 Setting the interrupt signal edge detection (polarity) 13.4- 4
13.4.3.5 Assembly positions 13.4- 4
13.4.4 Mechanical structure 13.4- 4
13.4.5 Pin assignment 13.4- 5
13.4.5.1 MPST bus interface, plug X1, X2 ..... 13.4- 5
13.4.5.2 Front plug X3 ..... 13.4- 6

13.1 Binary input unit 35 EB 90 R2



90 01 84

13.1.1 Technical data

Supply voltage	5 V ± 5 % (TTL)
Current input	≤ 400 mA
Signal level of all control signals, data and address signals	TTL
Max. permitted current through optocoupler LED	30 mA
Cut-in delay	typically 8 ms
Test voltage	2 $kV_{eff.}$
Permitted temperature range	0 ... 55 °C

13.1.2 Description

The input unit 35 EB 90 is the interface for binary signals between the process and the control.

There are 64 input channels which are galvanically isolated via optocouplers (plugs X3 ... X6, available on a card. They are divided into groups of 16 inputs each and are connected via 34-polar connectors with standard ribbon cables with two poles to the input modules 07 EM 61 (overview 1).

The input unit is a passive subscriber on the MPST bus.

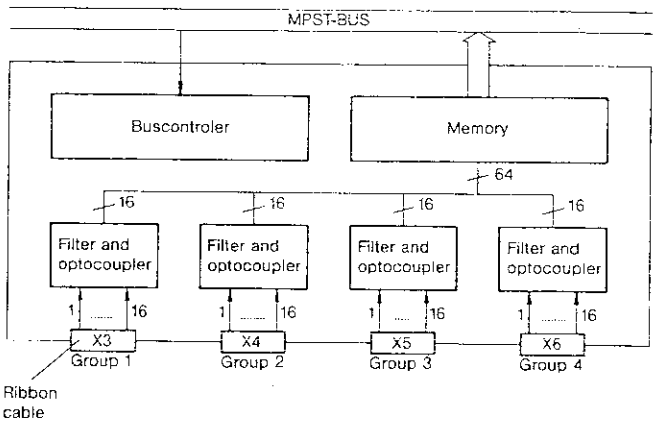


Fig. 13.1-1 Block diagram

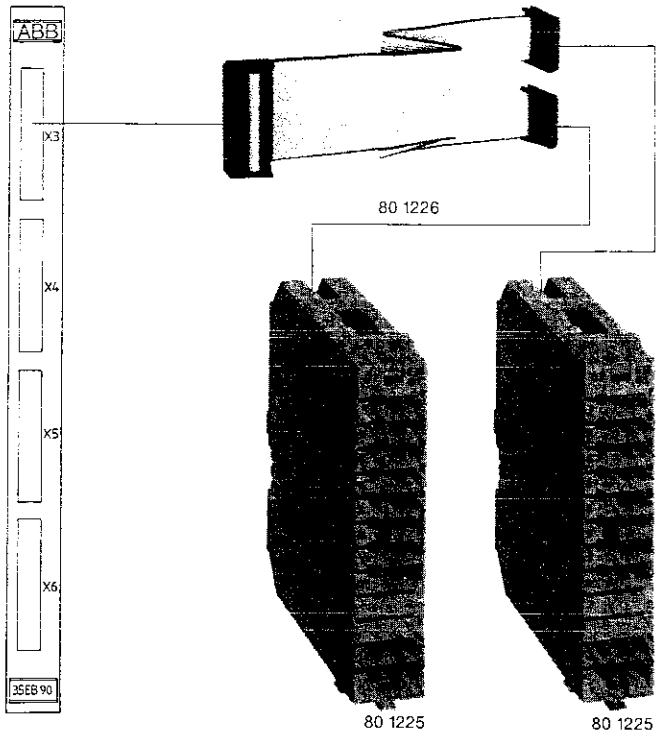
13.1.3 Mechanical structure

Mechanical dimensions according to DIN 41 494, part 2	233.4 x 160 mm H x W
Width of the front panel	4 R = 20.32 mm
Connecting elements on the rear according to DIN 41 612, part 2, design C	2 x 32-polar blade strips
Connecting elements on the front	4 x 34 -polar mine connector, Quickie type
Dimensions	1 pitch
Weight	0.5 kg
Order number	GJR5132100R2

For the pin assignment 35 EB 90, see overview 3

Overview 1

Connection of the 07 EM 61 input module with the 35 SK 90 system cable for the 35 EB 90 input unit



Input unit Channel 8–15 Channel 0–7

When installing the system cables and using input modules from other companies, attention is to be paid to the fact that the mine connector must always be connected to the cathodes of the optocoupler on the right-hand contact row (seen from the front panel). Anodes on the left-hand side.

13.1.4 Settings

The input unit can be read in bytes as well as in words. A prerequisite for switching through the data from the inputs to the data bus:

1. $\overline{R} = 0$
2. $\overline{I/O} = 0$
3. A13, A14, A15 = 1

The setting of the unit address is carried out with a 10-polar DIL switch (overview 2). The position OFF of the switch is detected by the system as logically 1, position ON as logically 0.

The data are prompted in words (WO = 1) or in bytes (WO = 0) via the data lines A0, A1, A2 and WO.

Table for "WO" = 0 (Byte prompting)

A00	A01	A02	A03 ... A12	A13	A14	A15	Signals on Berg plugs
0	0	0	x ... x	1	1	1	X3 low byte
1	0	0	x ... x	1	1	1	X3 high byte
0	1	0	x ... x	1	1	1	X4 low byte
1	1	0	x ... x	1	1	1	X4 high byte
0	0	1	x ... x	1	1	1	X5 low byte
1	0	1	x ... x	1	1	1	X5 high byte
0	1	1	x ... x	1	1	1	X6 low byte
1	1	1	x ... x	1	1	1	X6 high byte

Table for "WO" = 1 (Word prompting):

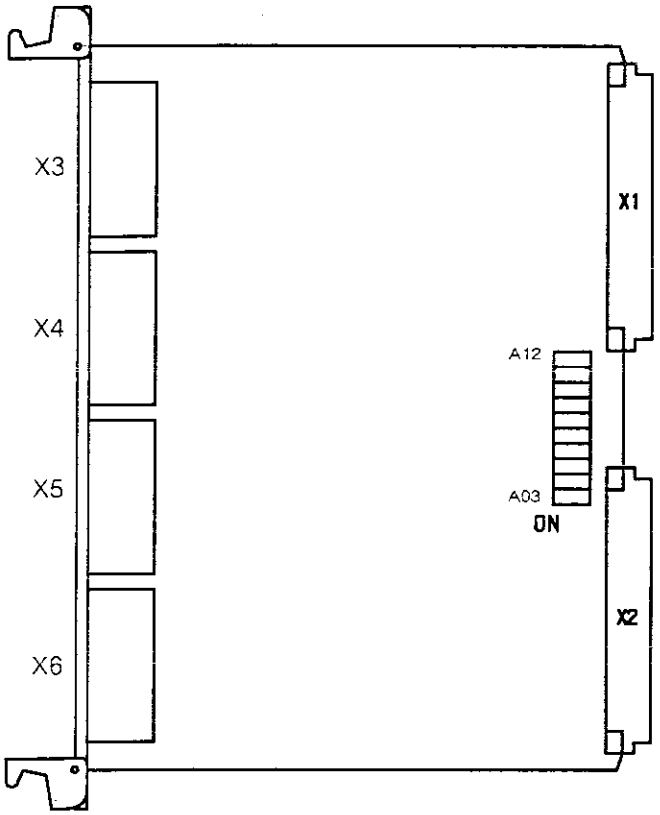
A00	A01	A02	A03 ... A12	A13	A14	A15	Signals on Berg plug
0	0	0	x ... x	1	1	1	X3
0	1	0	x ... x	1	1	1	X4
0	0	1	x ... x	1	1	1	X5
0	1	1	x ... x	1	1	1	X6

x for A3 to A12 means either 1 or 0.

A03 ... A12 Setting of the unit address

Overview 2

Mechanical structure 35 EB 90



X1 MPST bus
X2 MPST bus
} 32-polar MPST bus interface according to DIN 41 612, part 2, design C

X3 Output cable Channels 0–15
X4 Output cable Channels 16–31
X5 Output cable Channels 32–47
X6 Output cable Channels 48–63
} 34-polar plug connectors system cable 35 SK 90

Fig. 13.1-2 Component side (top view)

Overview 3

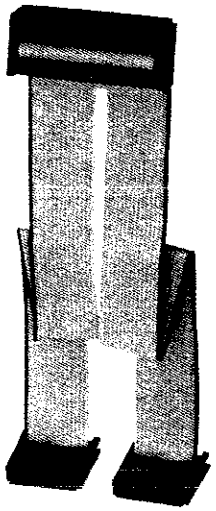
Plug assignment of the 35 EB 90

Plug	Channel	Pin	Plug	Channel	Pin
X3	0	33–34	X4	16	33–34
	1	31–32		17	31–32
	2	29–30		18	29–30
	3	27–28		19	27–28
	4	25–26		20	25–26
	5	23–24		21	23–24
	6	21–22		22	21–22
	7	19–20		23	19–20
	8	15–16		24	15–16
	9	13–14		25	13–14
	10	11–12		26	11–12
	11	9–10		27	9–10
	12	7– 8		28	7– 8
	13	5– 6		29	5– 6
	14	3– 4		30	3– 4
	15	1– 2		31	1– 2

Plug	Channel	Pin	Plug	Channel	Pin
X5	32	33–34	X6	48	33–34
	33	31–32		49	31–32
	34	29–30		50	29–30
	35	27–28		51	27–28
	36	25–26		52	25–26
	37	23–24		53	23–24
	38	21–22		54	21–22
	39	19–20		55	19–20
	40	15–16		56	15–16
	41	13–14		57	13–14
	42	11–12		58	11–12
	43	9–10		59	9–10
	44	7– 8		60	7– 8
	45	5– 6		61	5– 6
	46	3– 4		62	3– 4
	47	1– 2		63	1– 2

13.2 Cables and input modules

13.2.1 Flat system cable 35 SK 90 R*



80 12 26

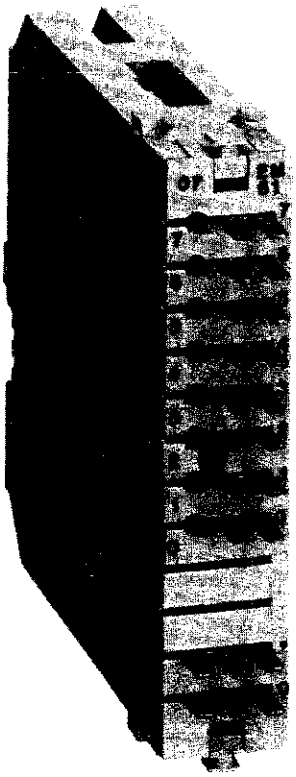
The 35 SK 90 system cable connects the 34-polar plus connectors of the ABB Procontic T300 in-/output unit with the 16-polar plug connectors of in-/output modules (1 or 2).

Examples: 35 EB 90 07 EM 61

The following lengths are supplied as standard:

Cable length	Type	Order number
0.5 m	35 SK 90 R1	GJR5135000R1
1.0 m	35 SK 90 R2	GJR5135000R2
1.5 m	**35 SK 90 R3**	**GJR5135000R3** (Preference)
2.0 m	35 SK 90 R4	GJR5135000R4
2.5 m	35 SK 90 R5	GJR5135000R5

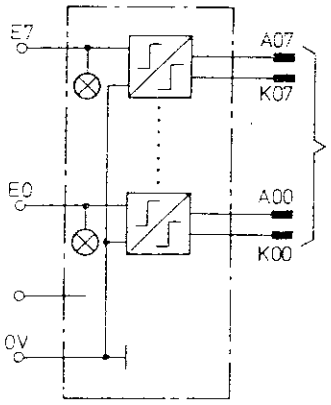
13.2.2 Input module 07 EM 61 R1 8 input channels 24 V DC with LED



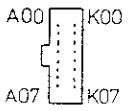
80 12 25

Technical data

Permitted ambient temperature	-20 °C ... +55 °C
Input signal level U_E for E0...E7	
with 0-signal	-31.2 ...+5 V DC
with 1-signal	+14 ... +31.2 V DC
Input current I_E with U_E = 24 V DC	approx. 10 mA per channel
Signalization of the input signal	1 yellow LED each
Dimensions	1 SIGMA®-tronic pitch
Weight	110 g
Order number	GJR5210800R1



Block diagram



Plug connector for the flat system cable

The input module 07 EM 61 serves to adapt the signals coming from the process for the ABB Procontic T300 control. It is used to increase the contact safety for mechanical encoders, to terminate a long input line with low ohms and therefore to improve the interference and destruction resistance, for example.

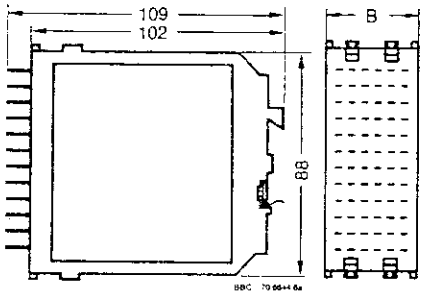
The module includes 8 independent input channels. The 1-signal for the respective input channel is displayed by a yellow light-emitting diode.

The switch is located in a plastic casing, which is put on a top-hat-rail of 35 mm in accordance with DIN 46 277, page 3.

The process signals are input from the front via flat plugs of 2.8 x 0.8 mm in accordance with DIN 46 244, which are in two parts and connected to each other.

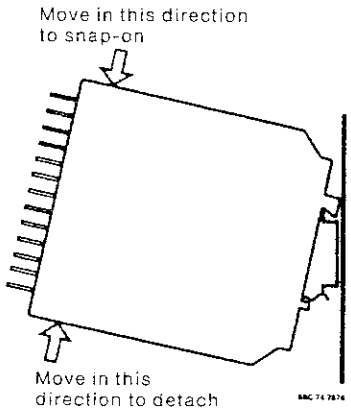
The output signals are guided to the ABB Procontic T300 control via a system cable 35 SK 90 or 35 SK 92 from above via a 16-polar plug connector.

The module does not require any current supply; the flat plugs + and 0 only serve to hand on the supply voltage to other ABB Procontic T300 components, e.g., output switch stages. The zero potential of the process signals is, however, required, as it is connected to the flat plug 0.



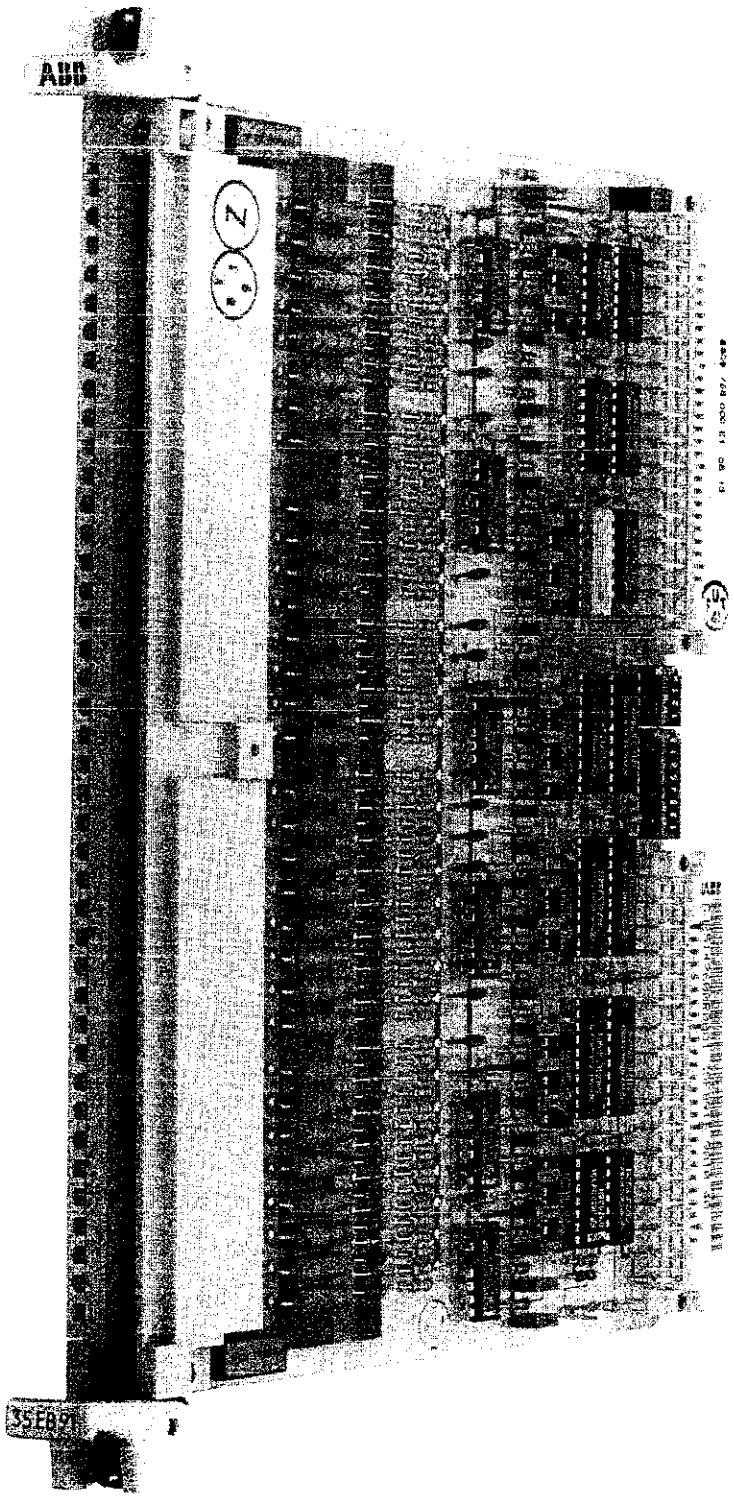
Module type	Meas. B
07 EM 61	20
07 LM 61	20
07 TM 61	40
07 RM 61	40
07 AM 62	40

Mounting measurements



Notes for mounting

13.3 Binary input unit 35 EB 91 R1 and R2



90 01 71

13.3.1 Technical data

Supply voltage U_{B1}	+ 5 V ± 5%
Current input I_{B1}	typically < 0.35 A
Power loss	8 W
Channels per unit	32
Input voltage U_{P1}. Rubric R1	24 DC V
Input voltage U_{P2}. Rubric R2	48 V
Rubric R1, 0 signal	- 30 V ... + 5.0 V
Rubric R1, 1 signal	+ 13 V ... + 31.0 V
Rubric R2, 0 signal	- 60 V ... + 10.0 V
Rubric R2, 1 signal	+ 26 V ... + 62.4 V
Permitted excess of the input voltage for	
Rubric R1	for 10 ms U_{P1} = 45 V
Rubric R2	for 10 ms U_{P2} = 90 V
Input current for	
Rubric R1, with 1 signal from U_{P1}	typically 8 mA
Rubric R2, with 1 signal from U_{P2}	typically 4 mA
Signal delay	typically 8 ms
Unscreened line length	600 m
Screened line length	1000m
Simultaneity factor	100 %
Electrical isolation R1/R2	no common reference potential 0 V
Signalization of the input signal	1 green LED per channel in the input circuit
Electro-magnetic compatibility	according to IEC 801/4
Ambient temperature	0 °C ... +55 °C
Storage temperature	- 25 °C ... +75° C
Humidity	F
Mechanical stress when installed	according to VDE 0160
Dimensions	1 pitch
Weight	0.3 kg
Order number **Rubric R1**	GJR5142600 R1
Rubric R2	GJR5142600 R2

Accessories:

Front plug 35 ST 90 R1	GJR5144900R1
Label set 35 SB 90 R1 for rubric R1	GJR5144600R1
Label set 35 SB 90 R2 for rubric R2	GJR5144600R2

13.3.2 Description

The binary input unit 35 EB 91 is a passive subscriber on the MPST-bus. It converts 32 input signals from the front plug terminals to the MPST bus.

The unit is available in two rubrics. Rubric 1 operates with 24 V input voltage, rubric 2 with 48 V input voltage.

The 32 input channels are divided into 4 groups of 8 channels each.

The input signals can only be "read". Reading can take place in words (1 words equals 2 bytes) or bytes via the MPST bus. The entire word is given to the bus when reading in bytes as well.

Prerequisites for the reading operation:
a) Control signal "$\overline{R}$" = 0
b) Control signal "$\overline{I/O}$" = 0
c) A 13, A 14 and A 15 = 1

Internal bus drivers are controlled in twos by the decoded word addresses (W0,W1), after the address detection has taken place. The signal "$\overline{BOV}$" (bus operation valid) is set to 0 by the reading processor card.

The bus drivers are switched on in this way and the input data appear on the MPST bus.

A signal ADET (Address detect signal) is output to the bus with a successful address comparison (unit addressed). This signal can be switched off (remove the resistors for R2).

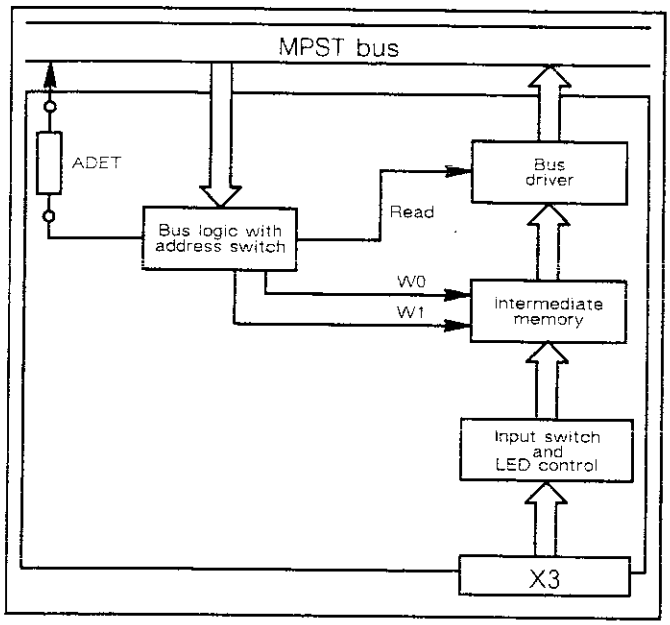


Fig. 13.3-1 Block diagram

13.3.3.2 Address division

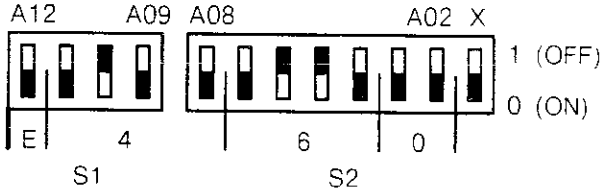
13.3.3 Unit addresses

13.3.3.1 Address setting

The addresses 'A02' to 'A12' of the card are set with the switches S1, S2 (4 bit and 8 bit DIL switches). The separate switch elements can be accessed after opening the transparent cover. See Fig. 13.3-2 for the position of the switches.

Example for setting the unit address:

Selected unit address: E460



Note:
The lowest switch element X of switch S2 is not connected.

(A15 ... A13: always equals 1 for in-/output units
A01: selection of the channel groups)
A00: logical 0

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	
T300 code of the upper passive address area (perm. wired up)			The unit address for switch S1 and S2 can be set. Setting ON = 0												
			Switch S1				Switch S2								

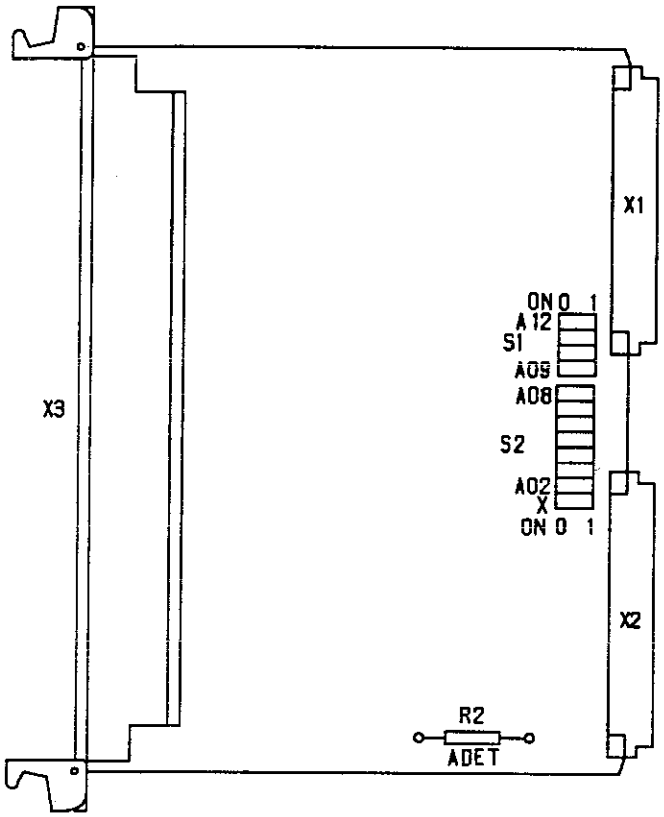
A01	Data	Input channel
0	D15 ... D00	0.15 ... 0.00
1	D15 ... D00	1.15 ... 1.00

13.3.3.3 Assembly positions

The assembly position ADET (Address detect signal, see Fig. 13.3-2) can be equipped with a resistor for R2 (100 Ω), if necessary.

13.3.4 Mechanical Structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.



X = not connected

Fig. 13.3-2 Component side (top view)

Displays:

32 LEDs, green colour to display the input signals

X1, X2	32-polar MPST bus interface according to DIN 41612, part 2, design C
X3	40-polar periphery interface (process data, +24 V, 0 V, free positions)

13.3.5 Pin assignment

13.3.5.1 MPST bus interface, plug X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U_{B1}	5 V voltage	X1. 2c	U_{B1}	5 V voltage
X1. 4a	U_{B1}	5 V voltage	X1. 4c	U_{B1}	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	–	–	X1.24c	–	–
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

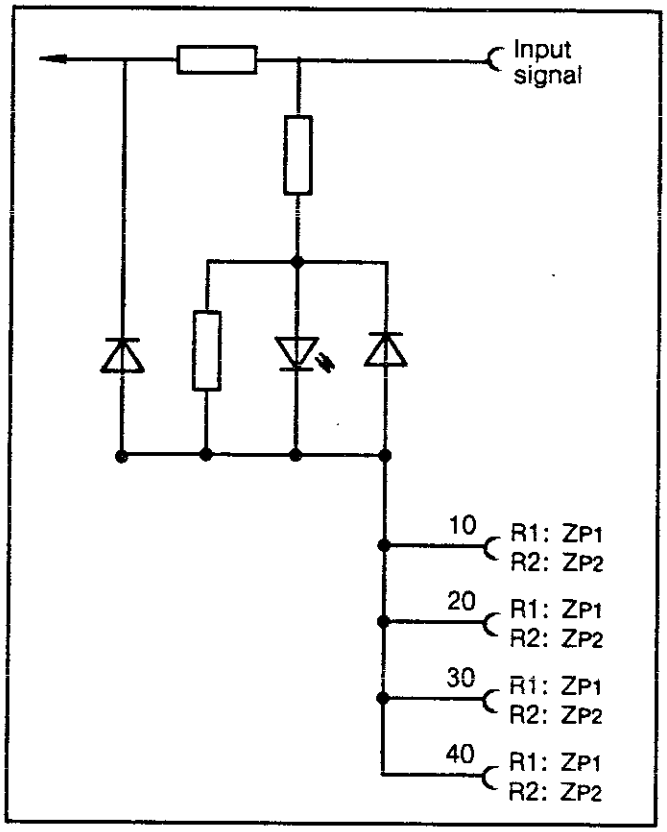
Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{BOV}$	Bus Operation Valid	X2.18c	–	–
X2.20a	–	–	X2.20c	–	–
X2.22a	ADET	Address Detect Signal	X2.22c	–	–
X2.24a	–	–	X2.24c	$\overline{R}$	Read
X2.26a	$\overline{I/O}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

13.3.5.2 Front plug X3

Pin	Signal name	Meaning
X3. 1	–	–
X3. 2	Input signal	Channel 0.00
X3. 3	Input signal	Channel 0.01
X3. 4	Input signal	Channel 0.02
X3. 5	Input signal	Channel 0.03
X3. 6	Input signal	Channel 0.04
X3. 7	Input signal	Channel 0.05
X3. 8	Input signal	Channel 0.06
X3. 9	Input signal	Channel 0.07
X3.10	Rubric R1: ZP1.0 Rubric R2: ZP2.0	0 V process voltage
X3.11	–	–
X3.12	Input signal	Channel 0.08
X3.13	Input signal	Channel 0.09
X3.14	Input signal	Channel 0.10
X3.15	Input signal	Channel 0.11
X3.16	Input signal	Channel 0.12
X3.17	Input signal	Channel 0.13
X3.18	Input signal	Channel 0.14
X3.19	Input signal	Channel 0.15
X3.20	Rubric R1: ZP1.1 Rubric R2: ZP2.1	0 V process voltage
X3.21	–	–
X3.22	Input signal	Channel 1.00
X3.23	Input signal	Channel 1.01
X3.24	Input signal	Channel 1.02
X3.25	Input signal	Channel 1.03
X3.26	Input signal	Channel 1.04
X3.27	Input signal	Channel 1.05
X3.28	Input signal	Channel 1.06
X3.29	Input signal	Channel 1.07
X3.30	Rubric R1: ZP1.2 Rubric R2: ZP2.2	0 V process voltage
X3.31	–	–
X3.32	Input signal	Channel 1.08
X3.33	Input signal	Channel 1.09
X3.34	Input signal	Channel 1.10
X3.35	Input signal	Channel 1.11
X3.36	Input signal	Channel 1.12
X3.37	Input signal	Channel 1.13
X3.38	Input signal	Channel 1.14
X3.39	Input signal	Channel 1.15
X3.40	Rubric R1: ZP1.3 Rubric R2: ZP2.3	0 V process voltage

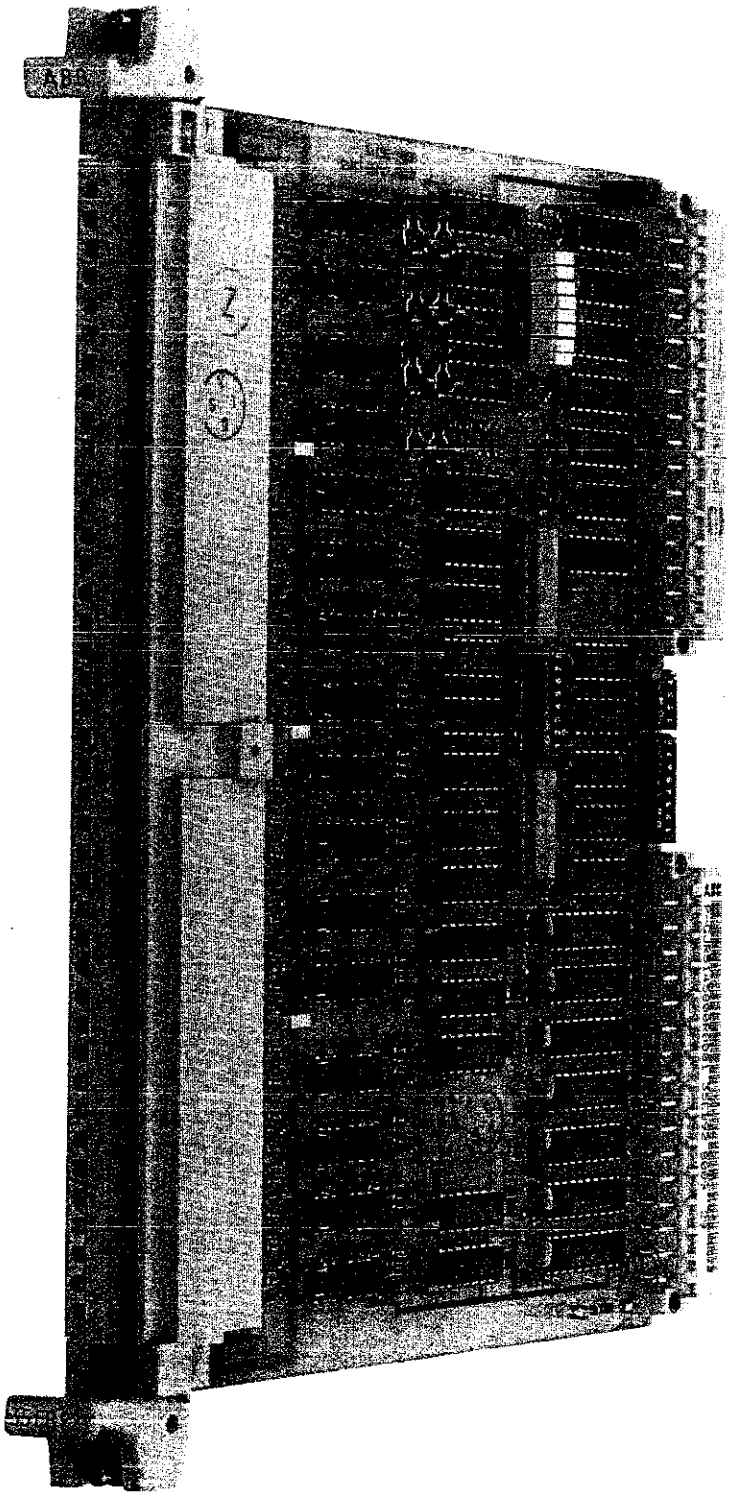
Important: A suitable equipotential bonding is to be created between 0 V voltage of the ABB Procontic T300 and 0 V process voltage. A voltage difference may **not** exist.

The connections of the 0 V process voltage must all be connected. They have a galvanic connection with the 0 V voltage of the ABB Procontic T300 on the unit.



13.3-3 Input switch

13.4 Binary input unit 35 EB 92 R1 and R2



90 01 73

13.4.1 Technical data

Supply voltage U_{B1}		+5 V ± 5%
Current input I_{B1}		typically ≤ 0.4 A
Power loss		8 W
Input voltage for rubric R1, U_{P1}		24 V
0 signal		-30 V ... + 5.0 V
1 signal		+13 V ... +31.0 V
Input voltage for rubric R2, U_{P2}		48 V
0 signal		-60 V ... +10.0 V
1 signal		+26 V ... +62.4 V
Permitted excess of the input voltage		
Rubric R1		for 100 ms, U_{P1} = 36 V
Rubric R2		for 100 ms, U_{P2} = 72 V
Signal delay		typically 3 ms (1.4 ... 5 ms)
Input current		
Rubric R1	with UP1 = 24 V	typically 7 mA
	with UP1 = 5 V	≥ 0.2 mA
	with UP1 = 13 V	≥ 2,0 mA
	with UP1 = 31.2 V	≤ 10.0 mA
Rubric R2	with UP2 = 48 V	typically 4 mA
	with UP2 = 10 V	≥ 0.2 mA
	with UP2 = 26 V	≥ 2.0 mA
	with UP2 = 62.4 V	≤ 10.0 mA
Electrical isolation R1/R2		Optocoupler in groups of 32 inputs or in 4 groups of 8 inputs each or in 2 groups of 16 inputs each.
Common reference potential		0 V
Channels per unit		32
Channels with interrupt initialization		8
Signalization of the input signals		1 green LED per signal in the input circuit
Unscreened line length:		600 m
Screened line length:		1000 m
Electro-magnetic compatibility		IEC 801/4
Ambient temperature		0 ... +55 _C
Storage temperature		-25 ... + 75 _C
Humidity		F
Mechanical stress when installed		in accordance with VDE 0160
Weight		0.3 kg
Dimensions		1 pitch
Order number rubric R1		GJR5145800R1
Order number rubric R2		GJR5145800R2

Accessories:

Front plug 35 ST 90 R1	GJR5144900R1
Label set 35 SB 90 R3 for rubric R1	GJR5144600R3
Label set 35 SB 90 R4 for rubric R2	GJR5144600R4

13.4.2 Description

The 35 EB 92 binary input unit is a passive subscriber on the MPST bus. It converts 32 input signals from the front plug terminals to the MPST bus. The 32 input channels are divided into 4 groups of 8 channels each. The input signals can only be "read" (in words and in bytes).

The unit is available in 2 rubrics. Rubric 1 operates with 24 V DC input voltage, rubric 2 with 48 V DC input voltage.

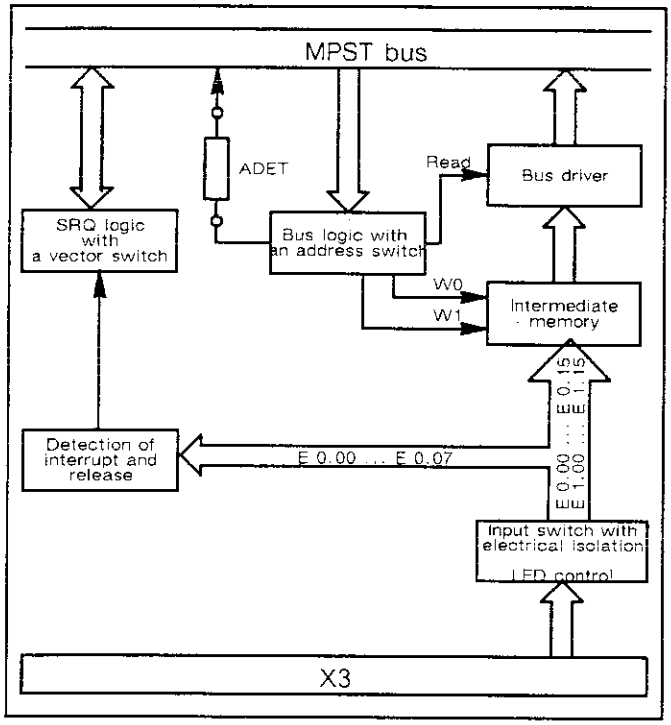


Fig.13.4-1 Block diagram

Diagnosis signal ADET

It can be ascertained with the signal ADET (Address detect signal) and a corresponding diagnosis unit, whether an addressed unit is present, not present or present many times. The signal ADET is output to the bus with a successful address comparison (unit addressed). This signal can be switched off (remove the resistors for R170).

Interrupts

The channels 0.00 to 0.07 can be used to detect interrupts. Signal alterations of 01 and 10 can be detected by corresponding plug-in jumpers. If an interrupt detection is not required, the plug-in jumpers are to be removed (see chapter 13.4.3.4). If a corresponding signal alteration is detected, an interrupt is initiated. This is a group interrupt, i. e., even if several channels detect an interrupt at the same time, only one interrupt is initiated. An interrupt treatment is triggered by the processor unit processing the interrupt (e.g., 35 ZE 93).

Note: The processor unit processing the interrupt is called a central unit (CU) in DIN 66 264 ZST. The input unit must first be read via the T300 bus (input channels 0.00 ... 0.07) after an interrupt has been initiated before another interrupt can be initiated via one of the 8 channels. An interrupt vector serves to detect the unit, which has initiated the interrupt. The value of the interrupt vector, corresponding to the range pregiven by the processor unit, is set via DIL switch S2 (see chapter 13.4.3.3 and Fig. 13.4-2). The signal delay can be varied by soldering in various capacitors in the range from approx . 1 ms to 5 ms with 8 assembly positions for the 8 input channels capable of the interrupt.

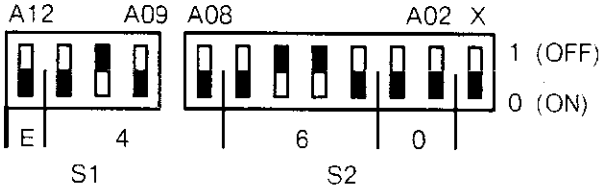
13.4.3 Unit addresses

13.4.3.1 Address setting

The addresses of the card are set via the addresses "A02" to "A12" with the switches S1 and S2 (4 bit and 8 bit DIL switches). The separate switch elements can be accessed by opening the transparent cover. See 13.4-2 for the position of the switches.

Example for setting the unit address:

Selected unit address: E460



Note:
The lowest switch element X of switch S2 is not connected.

Settings:

(A15 ... A13: is always equal to 1 for in-/output units
A01: selection of the channel group)
A00: logical 0

13.4.3.2 Address division

The MPST address lines are assigned as follows:

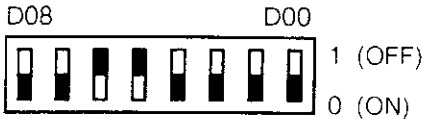
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	
T300 code of the upper passive address area (perm. wired up)			The unit address for switch S1 and S2 can be set. Setting ON = 0												
			Switch S1				Switch S2								

A01	Data	Input channel
0	D15 ... D00	0.15 ... 0.00
1	D15 ... D00	1.15 ... 1.00

13.4.3.3 Interrupt vector setting

The interrupt vector is set with the DIL switch S3. Assignment of the separate switches for the interrupt vector (individual data lines):

DIL switch S3



A logical 0 signal is output in the switch position "ON", a logical 1 signal in the switch position "OFF".

13.4.3.4 Setting the interrupt signal edge detection (polarity)

Plug connector	X11	X10	X3	X2	X14	X1	X13	X12
Assignment input channels	0.00	0.01	0.02	0.03	0.04	0.05	0.06	0.07

Terminal	Status	Function
1-2	bridged	detects signal change 1->0
2-3	bridged	detects signal change 0->1
1-2/2-3	open	Interrupt detect. switched off
1-2-3	bridged	not allowed

13.4.3.5 Assembly positions

Assembly position ADET (Address detect signal, see fig. 13.4-2) is equipped with R170 (100 Ω) by the factory.

Assembly positions for capacitors:

C 14 ... C17 and C19 ... C22

The assembly positions can be provided with capacitors 47 nF ... 100 nF (corresponds to a signal delay of 1 ms ... 5 ms). Factory assembly: 47 nF.

Equipment	Signal delay time
47 nF	1 ... 2 ms
68 nF	2 ... 3 ms
82 nF	3 ... 4 ms
100 nF	4 ... 5 ms

13.4.4 Mechanical structure

Unit in the double-sized Eurocard format 160 x 233.4 mm, 1 pitch.

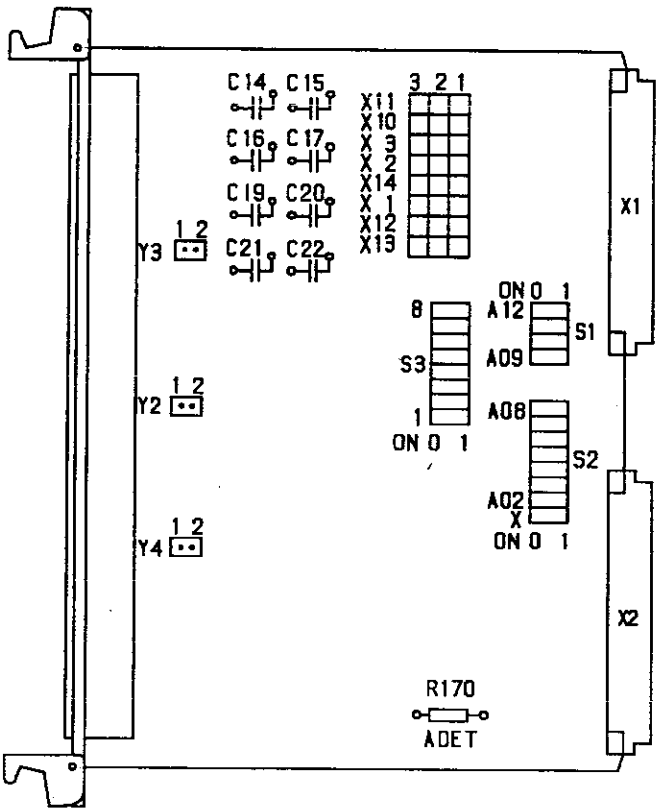


Fig. 13.4-2 Component side (top view)

Factory settings:

- Interrupt signal edge detection is switched off: X11/1, X10/1, X3/1, X2/1, X14/1, X1/1, X13/1, X12/1.
- 0V process voltage (bridged for all channels): Y2/1-2, Y3/1-2, Y4/1-2.

Displays:
32 LEDs, green colour to display the input signals

Plug connectors:

X1, X2	32-polar T300 bus interface in acc. with DIN 41612, part 2, design C
X3	40-polar periphery interface (process data, 0 V, free positions)

13.4.5 Plug Assignment

13.4.5.1 MPST bus interface, plugs X1 , X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	–	–	X1.24c	–	–
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	$\overline{\text{SRQ}}$	Service Request	X1.30c	$\overline{\text{HSRQ}}$	Hold Status SRQ
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	–	–
X2.20a	–	–	X2.20c	–	–
X2.22a	ADET	Address detect signal	X2.22c	–	–
X2.24a	–	–	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

13.4.5.2 Front plug X3

Pin	Signal name	Meaning
X3. 1	–	–
X3. 2	Input signal	Channel 0.00
X3. 3	Input signal	Channel 0.01
X3. 4	Input signal	Channel 0.02
X3. 5	Input signal	Channel 0.03
X3. 6	Input signal	Channel 0.04
X3. 7	Input signal	Channel 0.05
X3. 8	Input signal	Channel 0.06
X3. 9	Input signal	Channel 0.07
X3.10	Rubric R1: ZP1.0 Rubric R2: ZP2.0	0 V process voltage
X3.11	–	–
X3.12	Input signal	Channel 0.08
X3.13	Input signal	Channel 0.09
X3.14	Input signal	Channel 0.10
X3.15	Input signal	Channel 0.11
X3.16	Input signal	Channel 0.12
X3.17	Input signal	Channel 0.13
X3.18	Input signal	Channel 0.14
X3.19	Input signal	Channel 0.15
X3.20	Rubric R1: ZP1.1 Rubric R2: ZP2.1	0 V process voltage
X3.21	–	–
X3.22	Input signal	Channel 1.00
X3.23	Input signal	Channel 1.01
X3.24	Input signal	Channel 1.02
X3.25	Input signal	Channel 1.03
X3.26	Input signal	Channel 1.04
X3.27	Input signal	Channel 1.05
X3.28	Input signal	Channel 1.06
X3.29	Input signal	Channel 1.07
X3.30	Rubric R1: ZP1.2 Rubric R2: ZP2.2	0 V process voltage
X3.31	–	–
X3.32	Input signal	Channel 1.08
X3.33	Input signal	Channel 1.09
X3.34	Input signal	Channel 1.10
X3.35	Input signal	Channel 1.11
X3.36	Input signal	Channel 1.12
X3.37	Input signal	Channel 1.13
X3.38	Input signal	Channel 1.14
X3.39	Input signal	Channel 1.15
X3.40	Rubric R1: ZP1.3 Rubric R2: ZP2.3	0 V process voltage

The four connections of the 0 V process voltage ZP1 or ZP2 (rubric 1: ZP1.0, ZP1.1, ZP1.2, ZP1.3 or rubric 2: ZP2.0, ZP2.1, ZP2.2, ZP2.3) are connected to each other by jumpers. It is possible to create four input channel groups by separating the jumpers. These groups are isolated from each other with a separate supply of UP/ZP.

Jumper	Connection
Y2	Z P1.0 – Z P1.1 or Z P2.0 – Z P2.1
Y3	Z P1.1 – Z P1.2 or Z P2.1 – Z P2.2
Y4	Z P1.2 – Z P1.3 or Z P2.2 – Z P2.3

0 V process voltage	Connections for channels
Z P1.0 or Z P2.0	0.00 ... 0.07
Z P1.1 or Z P2.1	0.08 ... 0.15
Z P1.2 or Z P2.2	1.00 ... 1.07
Z P1.3 or Z P2.3	1.08 ... 1.15

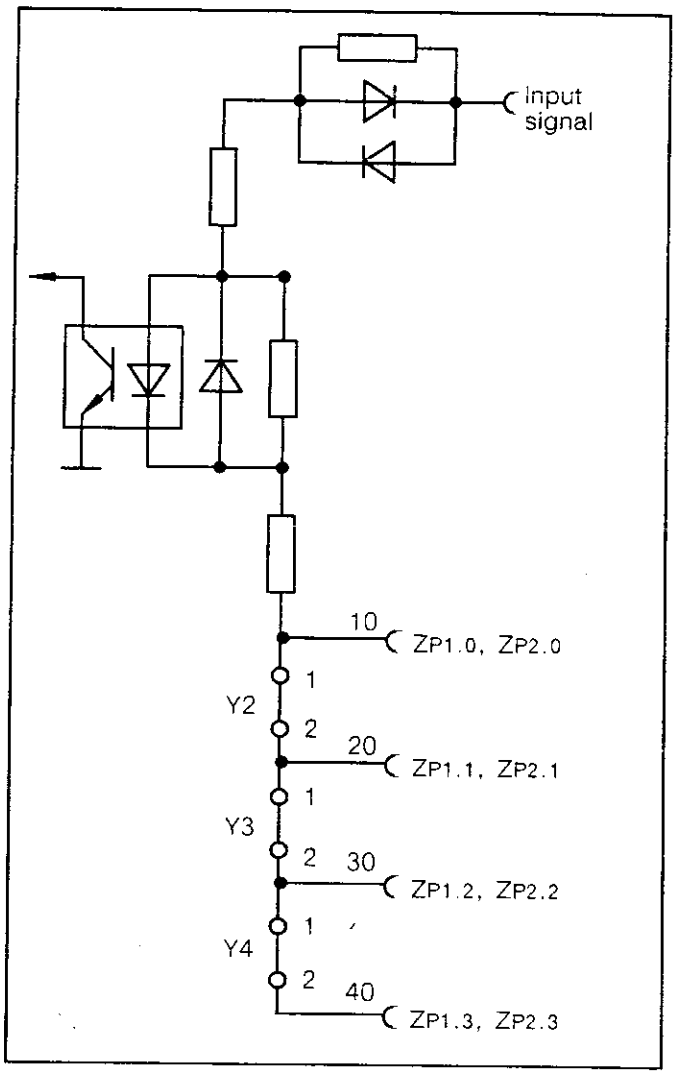


Fig. 13.4-3 Input circuit

14 Analog input units

35 TP 90 R1: Board carrier for 35 EA 90 R1, 35 EA 91 R1, 35 EA 92 R1 and 35 EG 90 R1.

35 EA 90 R1: Analog input,	voltage,	± 5 V, ± 10 V,	12 bit 8-fold.
35 EA 91 R1: Analog input,	voltage	± 5 V, ± 10 V, 0 ... 10 V,	12 bit, 8-fold.
	current	0 ... + 20 mA, + 4 ... + 20 mA,	
35 EA 92 R1: Analog input,	Pt100,	- 50 °C ... +150 °C,	12 bit, 4-fold.
35 EA 92 R2: Analog input,	Pt100,	- 50 °C ... +400 °C,	12 bit, 4-fold.

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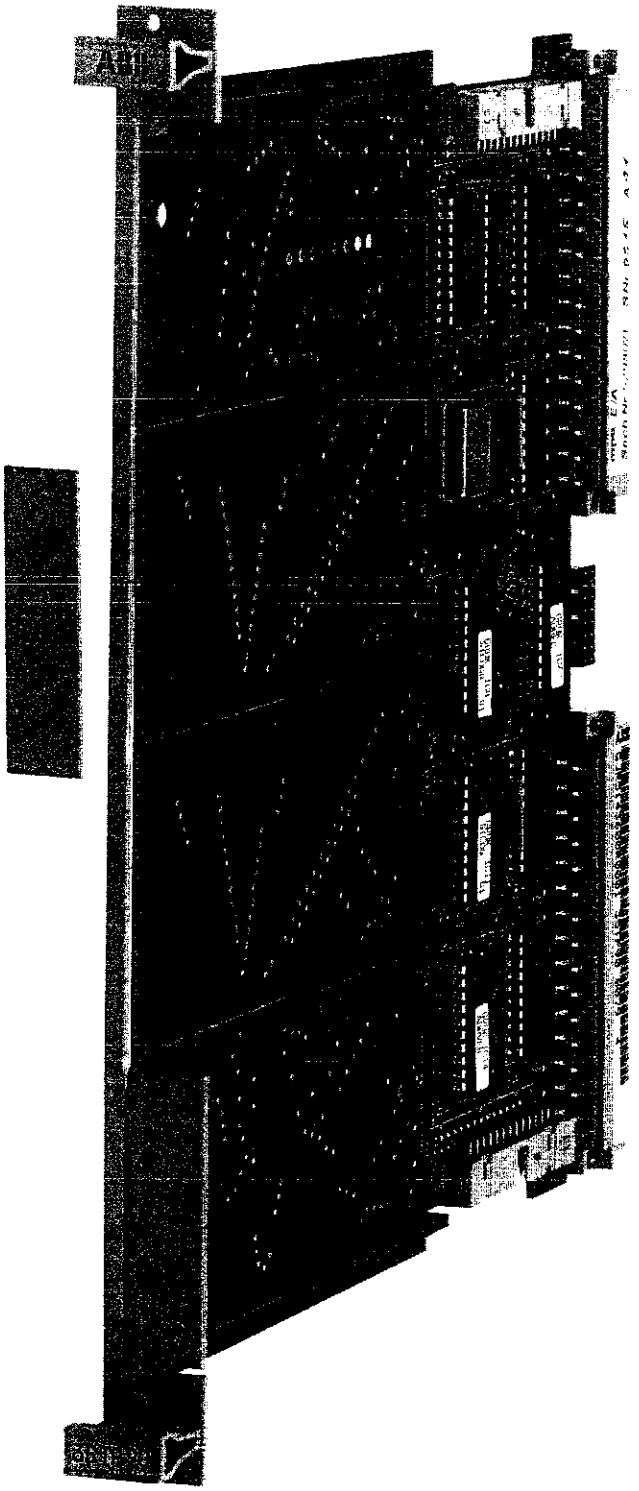
14.1 35 TP 90 R1 board carrier for analog input units



90 07 06

14.1.1 Technical data

Current supply:	
U_{B1} positive supply voltage	+ 5 V, + 0.5 V, - 0.25 V
U_{B2} positive supply voltage	+ 15 V, + 1.5 V, - 3.6 V
U_{B3} negative supply voltage	- 15 V, - 1.5 V, + 3.6 V
I_{B1} for U_{B1}	250 mA, + 50 mA, - 20 mA
I_{B2} for U_{B2}	55 mA, + 20 mA, - 10 mA
I_{B3} for U_{B3}	55 mA, + 20 mA, - 10 mA
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity	F
Mechanical stress when installed	VDE 0160
Weight	0.36 kg
Dimensions	1 pitch
Order number	GJR5143600R1

14.1.2 Description

The 35 TP 90 R1 board carrier has 4 module socket poslitions for the analog input units 35 EA 90 (requires 1 module socket position), 35 EA 91 (requires 2 module socket positions) and 35 EA 92 (requires 2 module socket positions).

The converted analog value is available after addressing a channel and can be read by the unit as a data word file by the MPST bus . For more details, see the respective descriptions of the analog input in the chapters 14.2, 14.3 und 14.4.

The unit is a passive subscriber on the MPST bus.

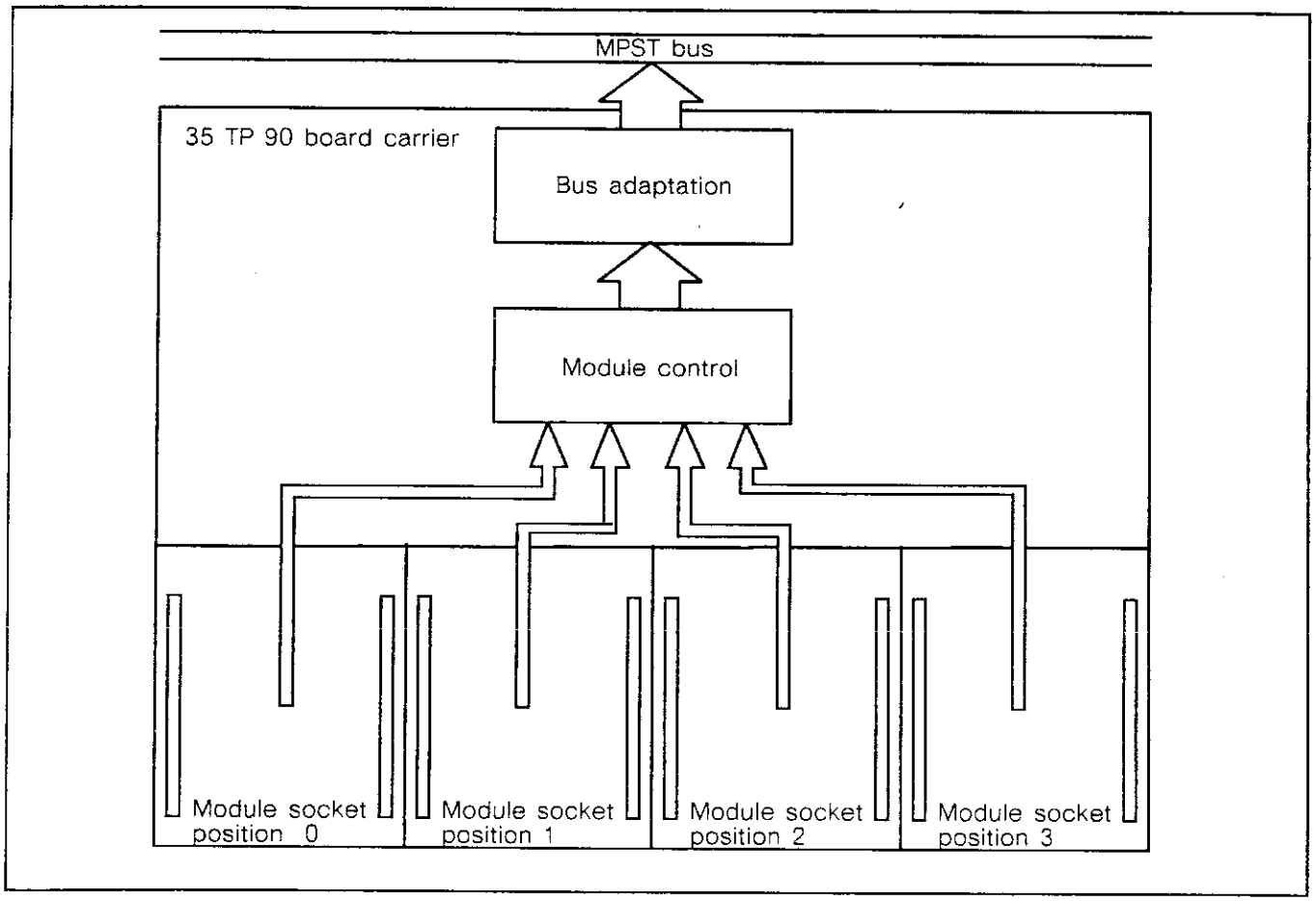


Fig. 14.1-1: Block diagram

14.1.3 Mechanical structure

Unit in the double-size in the Eurocard format 160 x 233.4 mm, 1 pitch.

Plug connectors:

X1, X2	32-polar bus interface according to DIN 41 612, part 2, design C

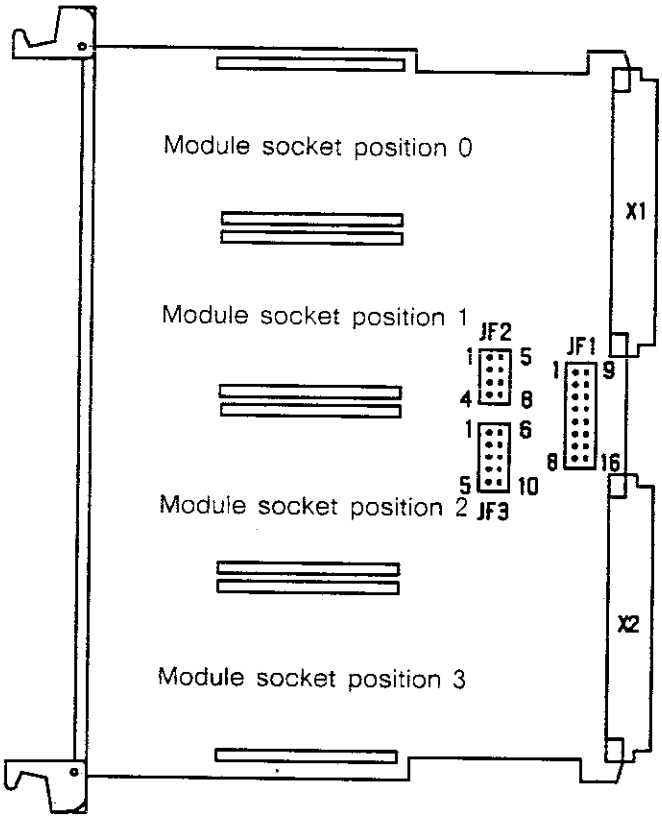


Fig. 14.1-2: Component side (top view)

14.1.4 Plug assignment

14.1.4.1 ABB Procontic T300 bus interface, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	U B3	- 15 V voltage	X1. 6c	U B2	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transmission	X1.24c	$\overline{\text{PFD}}$	Power Fail Detect
X1.26a	–	–	X1.26c	–	–
X1.28a	$\overline{\text{BB}}$	Bus Busy	X1.28c	$\overline{\text{RBB}}$	Reset Bus Busy
X1.30a	$\overline{\text{SRQ}}$	Service Request	X1.30c	$\overline{\text{HSRQ}}$	Hold Status SRQ
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plugr X2:

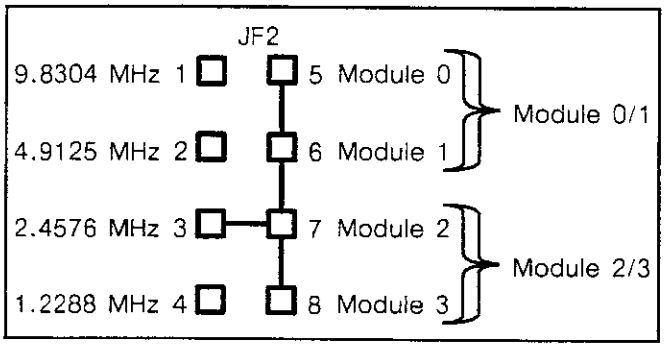
Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{BOV}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	SYNC	Synchronisation signal	X2.20c	CC	Central Clock
X2.22a	–	–	X2.22c	$\overline{RS}$	Reset
X2.24a	$\overline{W}$	Write	X2.24c	$\overline{R}$	Read
X2.26a	$\overline{IO}$	I/O memory area	X2.26c	–	–
X2.28a	$\overline{DMARQ}$	DMA Request	X2.28c	DMACK	DMA Acknowledge
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

14.1.5 Settings

14.1.5.1 Clock setting

Each module is to be supplied by the board carrier 35 TP 90 with the clock. To this end, a frequency generated by the 35 TP 90 is selected and switched through to all modules via the jumper zone JF2.

The anologue input module 35 EA 91 requires a frequency of 2.4576 MHz.

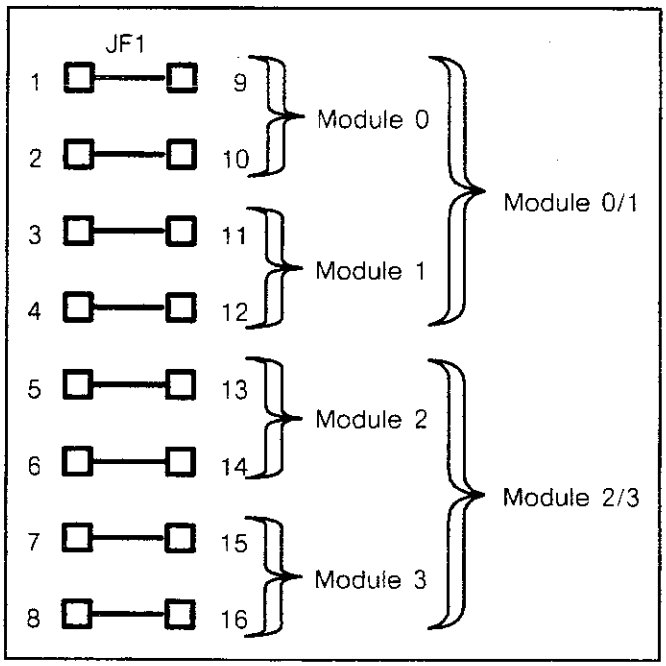


Jumper zone **JF2**: Clock setting on the 35 TP 90 for 35 EA 91

The anologue input module 35 EA 90 requires a frequency of 9.8304 MHz.

14.1.5.2 Setting the module arrangement

All the jumpers must be inserted on the jumper zone JF1 for the arrangement of the 2 analog modules (i.e. the factory setting remains unchanged). The arrangement of the modules 0/1 and 2/3 is thus created on the board carrier.



Jumper zone **JF1**: Moduel arrangement on 35 TP 90

Explanation:
module 0, 1, 2 and 3: 35 EA 90
module 0/1: 35 EA 91 or 35 EA 92
module 2/3: 35 EA 91 or 35 EA 92

14.1.5.3 Unit address setting

The upper hexidecimal figures (A8...A15) are significant for addressing the anologue input, whereby the uppermost three address bits A13...A15 are permanently set to logically 1. The address bits A8...A12 are set in the jumper zone JF3 ((inserted jumper = 0, disconnected jumper = 1).

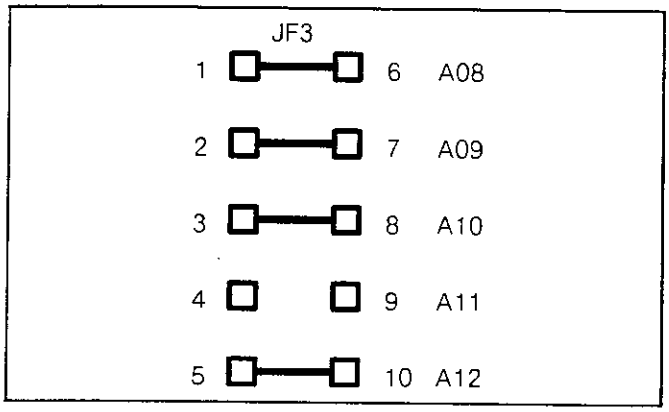
The MPST bus address E800H corresponds to the following bit example:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	0	0
← Unit address →													← Module number →		

256 addresses are occupied starting from the set address. The addresses E800H...E8FFH are occupied by the 35 TP 90 in the example shown.

It depends on the **analog module used** under which addresses the analog values can be read.These addresses can be taken from the respective unit description of the analog inputs.

The unit address shown in the example is to be set in the following way in the jumper zone JF3 on the board carrier:



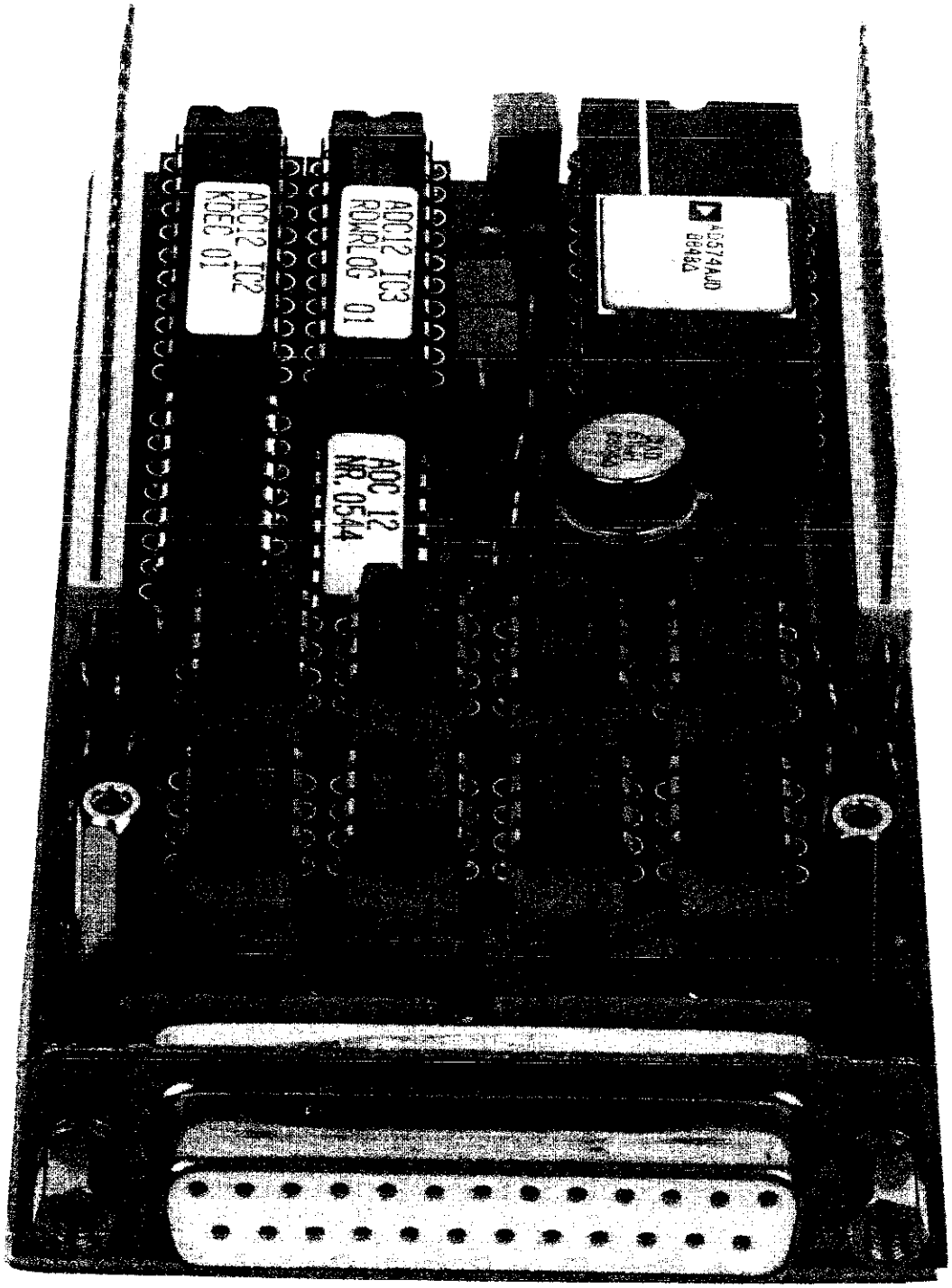
Jumper zone **JF3**: Unit address on the 35 TP 90

The module release signals (Address bits A00 ... A02) are shown in the table 14.2-4 .

Module	A2	A1	A0
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	0

Table14.2-4: Module release

14.2 Analog input unit 35 EA 90 R1



90 01 89

14.2.1 Technical data

Conversion range:

Range 1:	- 10 V to + 10 V
Range 2:	- 5 V to + 5 V

Note:
The range - 10 V to + 10 V is set by the factory

Accuracy (with 25 degree centigrade):	Conversion range	
	± 5 V	± 10 V
Linearity error (analog)	2.44 mV	4.88 mV
Unipolar offset (analog)	4.88 mV	9.76 mV
Linearity error (digital)	± 1 LSB	
Unipolar offset (digital)	± 2 LSB	
Drift (Bipolar offset) above the temperature range	± 10 LSB 0,000001/°C	
Value assignment	Analog	Digital
	+ 10 V (+ 5 V)	+ 2047 (7FFH)
	- 10 V (- 5 V)	- 2048 (800H)
	0 V	0
Conversion time (12 bit cycle)	< 40 µsec	
Data format	12 bit INTEGER (Two's complement) on the right	
Front plug	25-polar D plug	
Spatial requirement	1 Module socket position on the 35 TP 90 R1 board carrier	
Weight	0.1 kg	
Order number: Analog module 35 EA 90 R1	GJV3073002R1	

Accessories:

35 TP 90 R1 board carrier	GJR5143600R1

14.2.2 Description

The analog input with 32 channels consists of a basic card and 1 to 4 analog modlules (subprints). Each of the analog modules (module 0 to module 3) is assigned 8 input channels, so that the unit has a total of 32 input channels with four modules assembled.

The unit can function with 1 to 4 analog modules connected.

Each of the 8 input channels can be switched to the A/D converter via a multiplexer. The channel to be selected by the multiplexer is pregiven by writing the analog module with a control word.

The converted analog value is available after the channel has been activated and the conversion time is over and can be read by the unit as a data word via the MPST bus.

The unit is a passive subscriber on the MPST bus.

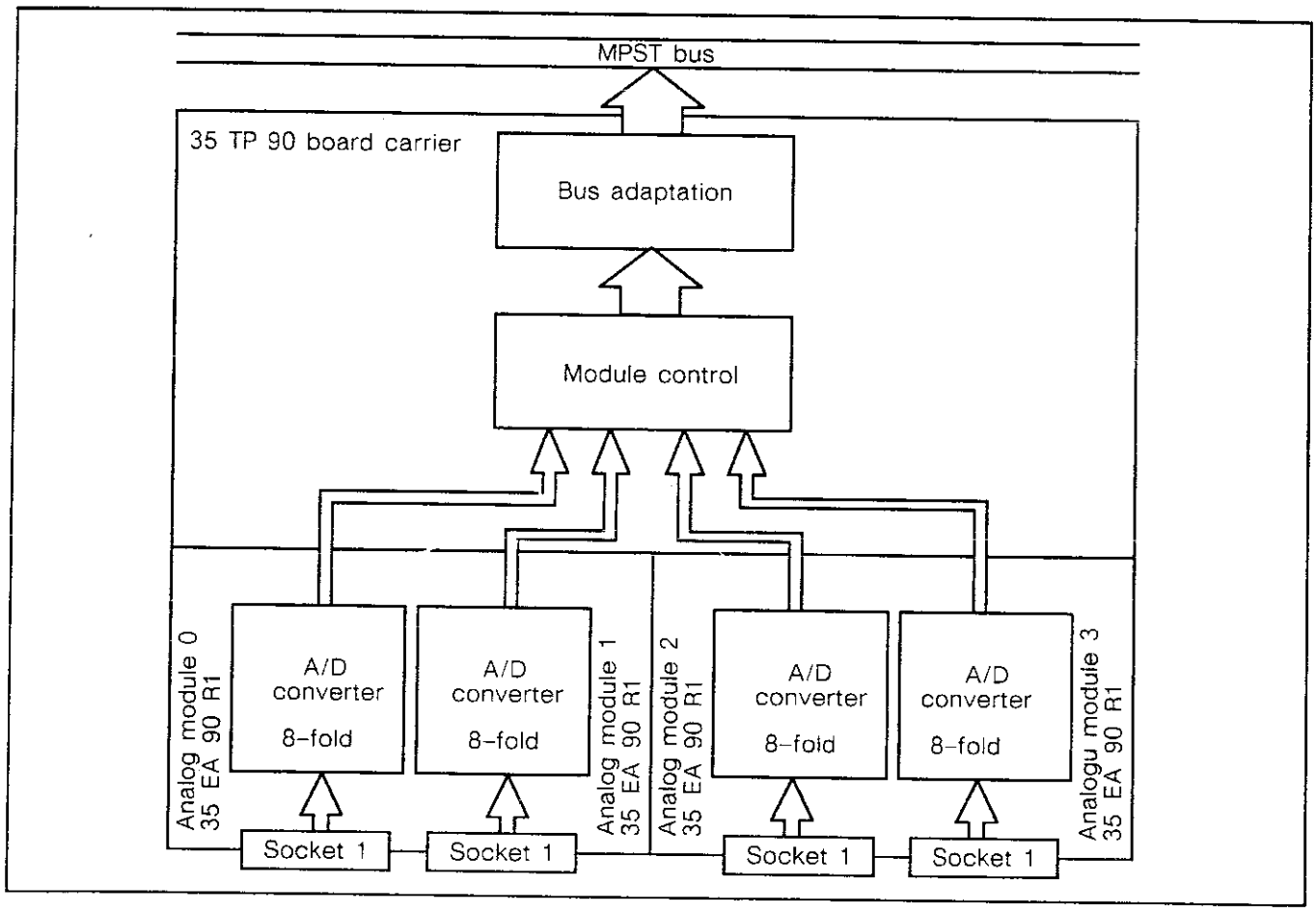


Fig.14.2-1: Block diagram

14.2.3 Basic settings of the board carrier

14.2.3.1 Clock setting

Every analog input 35 EA 90 R1 is to be supplied by the 35 TP 90 R1 board carrier with the clock. To this end, a frequency generated by the 35 TP 90 R1 is selected and switched through to all the modules via the jumper zone JF2.

Example:
All the analog inputs 35 EA 90 R1 on the board carrier are set to a frequency of 2.4576 MHz. Another clock is not practicable.

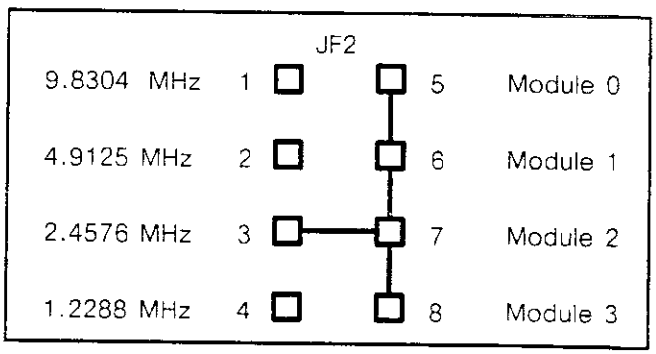


Fig. 14.2-2: Jumper zone **JF2**, clock setting on the 35 TP 90

14.2.3.2 Setting the module arrangement

All the jumpers must be inserted on the jumper zone JF1 for the arrangement (i.e., the factory setting remains unchanged. The arrangement of the modules 0, 1, 2 and 3 is thus created on the board carrier (see also 14.1.5.2).

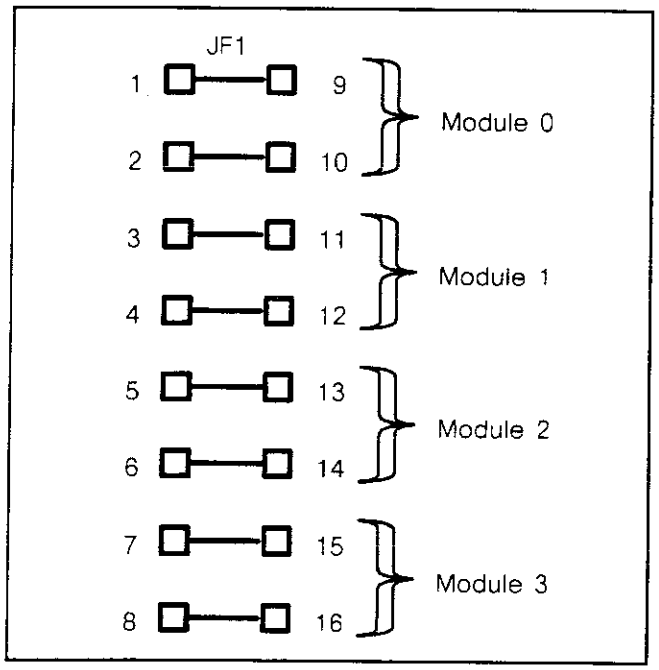


Fig.14.2-3: Jumper zone **JF1**, module arrangement on the 35 TP 90

14.2.3.3 Unit address setting

The upper hexadecimal figures (A08...A15) are significant for addressing the anologue input 35 EA 90 R1 whereby the uppermost three address bits A13...A15 are permanently set to logically 1. The address bits A08...A12 are set in the jumper zone JF3 (inserted jumper = 0, disconnected jumper = 1).

The MPST bus address E800H corresponds to the following bit pattern:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	0	0
← Unit address →													← Module number →		

The unit address E800H shown in the example is to be set in the following way in the jumper zone JF3 on the board carrier:

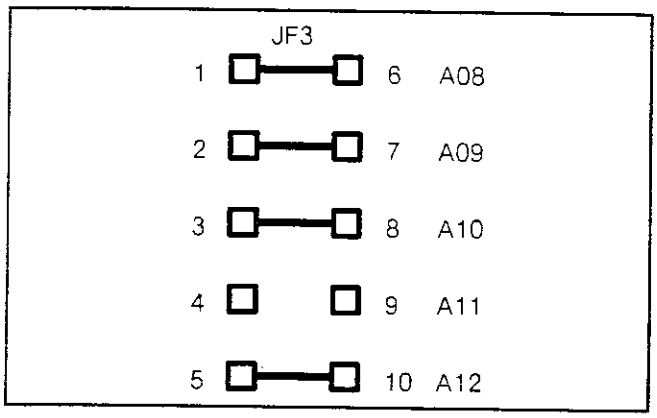


Fig.14.2-4: Jumper zone **JF3**, unit address on the 35 TP 90

The module release signals (Address bits A00 ... A02) are shown in the table 14.2-5.

Module	A02	A01	A00
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	0

Table 14.2-5 Module release

Setting up the lowest address bits for the respective module can be seen from table 14.2-5.

Example:
Module 0 and channel 1 should be read; this corresponds to the address E800H (A00, A01 and A02 equal logically 0). The address E804H is valid for channel 1 and module 3 (A02 equals logically 1, hexadecimally 4). This is also valid for other channels, whereby the addresses for module 3 are composed in the following way:
Address module 2 (in hexadecimal numbers) = address module 1 (in hexadecimal numbers) + 4H.

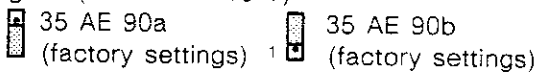
The possible address area of the analog input ranges from E0XXH to FFXXH.

14.2.4 Analog module setting

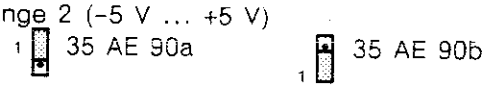
14.2.4.1 Setting the voltage range

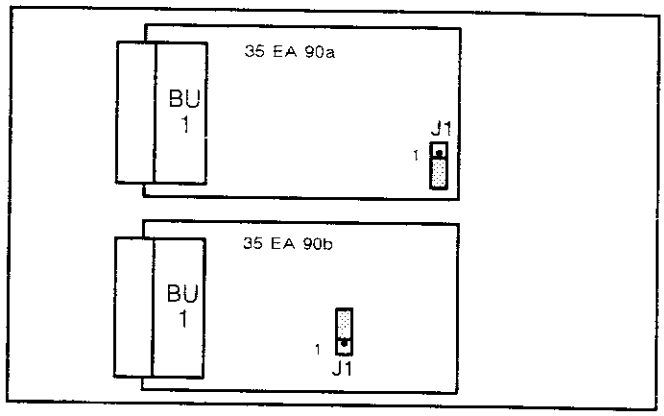
The conversion range of the analog module can be set by jumper J1 on the analog module. The following assignment is valid:

Range 1 (-10 V ... +10 V)



Range 2 (-5 V ... +5 V)





14.2.4.2 Activating an analog channel

If an analog value is to be read by the unit, the corresponding channel must be activated beforehand for the desired module. The multiplexer is set to the desired channel here.

The activation is carried out by writing a control word on the corresponding module. This word includes the number of the channel to be selected in the data bits D0 ... D2 . Moreover, the data bit 5 must have the value logically 1 (sample mode).

Example:
Selecting the channel 3 on the module 2. Unit address E8XX in the sample mode

MPST bus address:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	1	0
← Unit address →								← without meaning →					← Module number →		

Control word:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1

D0 ... D2: Channel number (3 here)

D5: 1 —> Sample Mode
0 —> Hold Mode

14.2.4.3 Reading an analog channel

The converted analog value is available after activating a channel and after the conversion time is over (< 40 µs). This can then be read as a data word via the MPST bus.

Structure of the data word:

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
STS	X	X	X	V	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

D0 ... D10: Converted value in the two's complement (Y)
D11: Sign of the value (V)
D12 ... D14: Meaningless (X)
D15: Status
1 —>Value is still not valid
0 —>Value is valid

Example:
Reading the value from channel 3 on Module 2

MPST bus address:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	1	0
← Unit address →								← without meaning →					← Module number		

Control word as described under 3.3.6.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
STS	X	X	X	V	Value										

D00 ... D10: Converted value in the two's complement
D11: Sign of the value (V)
D12 ... D14: Meaningless (X)
D15: Status (STS)

The unit can be addressed with the function block 'ANAEIN', using the PLC central units.

14.2.5 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

Plug connectors:

X1, X2	32-polar bus interface in accordance with DIN 41 612, part 12, design C
BU1	25-polar analog interface on analog input module 35 EA 91 (AMP HDP 20)

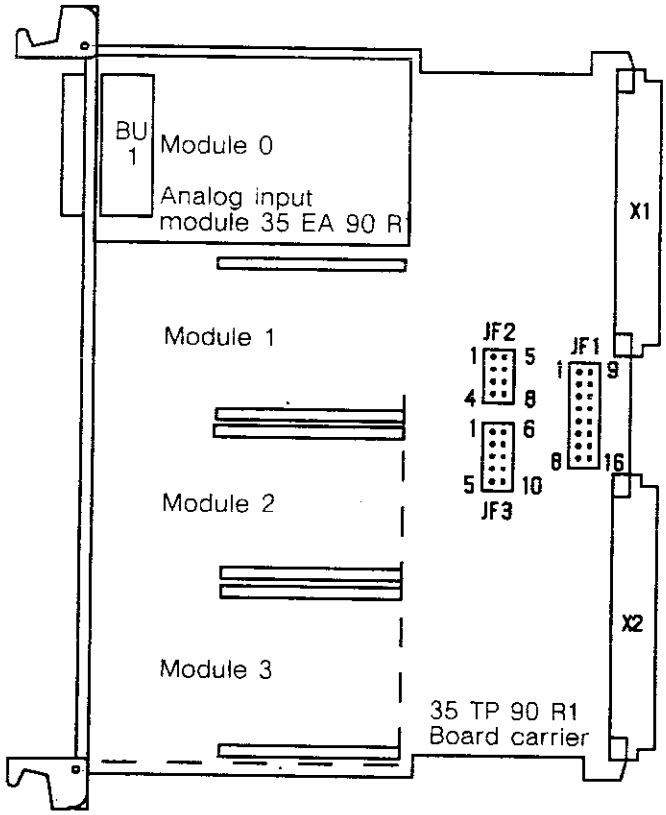


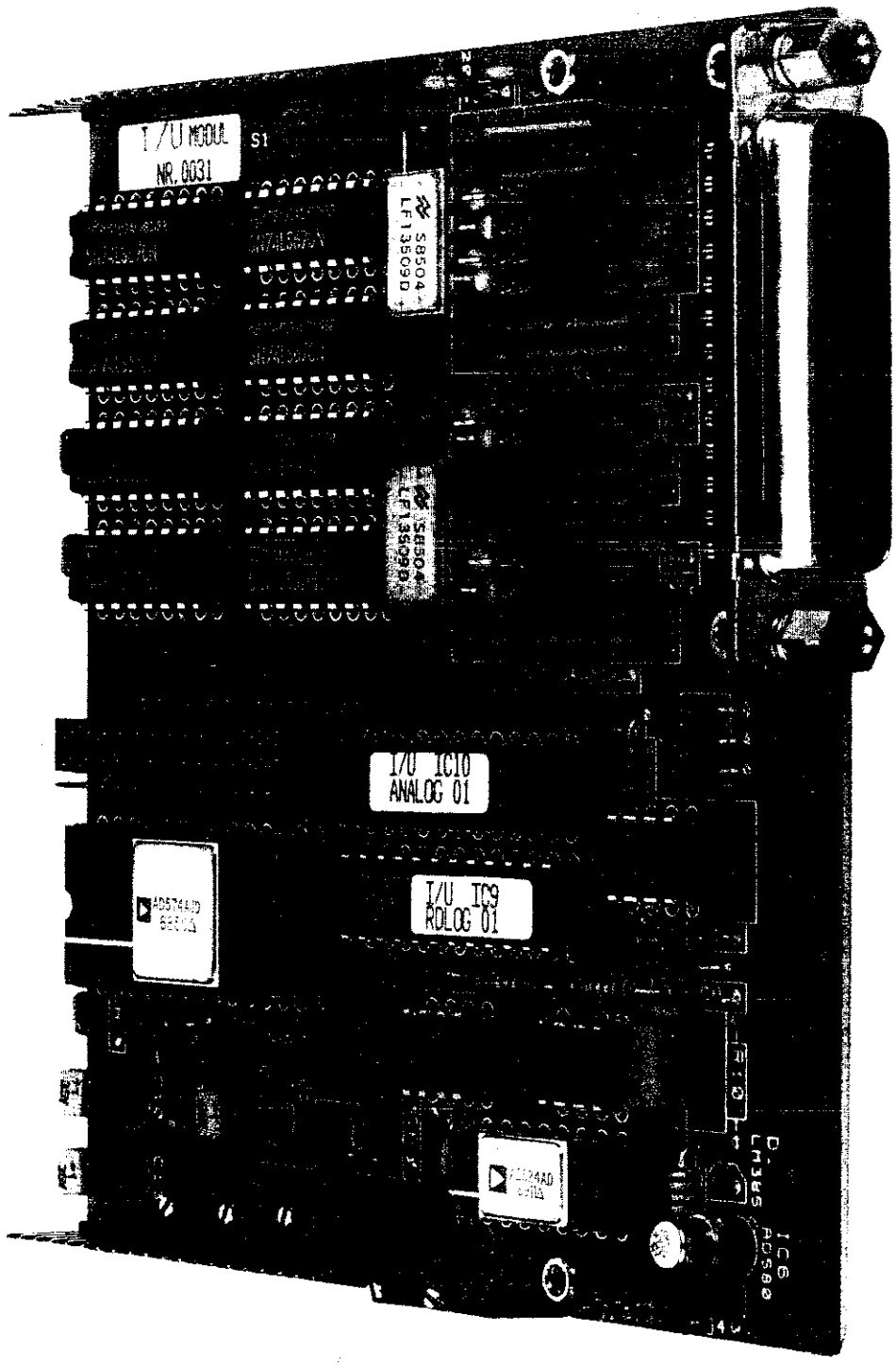
Bild 14.2-4: Component side (top view)

14.2.6 Plug assignment

Pin	Signal	Meaning	Pin	Signal	Meaning
BU1. 1	Screen	Screen	BU1.14	–	–
BU1. 2	E1	Channel 1, analog input +	BU1.15	–	–
BU1. 3	E2	Channel 2, analog input +	BU1.16	–	–
BU1. 4	E3	Channel 3, analog input +	BU1.17	AGND	Analog ground
BU1. 5	E4	Channel 4, analog input +	BU1.18	AGND	Analog ground
BU1. 6	E5	Channel 5, analog input +	BU1.19	–	–
BU1. 7	E6	Channel 6, analog input +	BU1.20	–	–
BU1. 8	E7	Channel 7, analog input +	BU1.21	–	–
BU1. 9	E8	Channel 8, analog input +	BU1.22	DGND	Digital ground
BU1.10	$\overline{\text{SHOUT}}$	Sample Hold Out *	BU1.23	–	–
BU1.11	–	–	BU1.24	–	–
BU1.12	–	–	BU1.25	–	–
BU1.13	–	–			

* Output signal: 0 = Sample mode
1 = Hold mode

14.3 Analog input unit 35 EA 91 R1



90 01 87

14.3.1 Technical data

Number of inputs	8 voltage/ current inputs
Electrical isolation	No
Input range	± 5 V, ± 10 V, 0 V ... +10 V *) 0 mA ... +20 mA, +4 mA ... +20 mA
Input resistance for current	100 Ω
Input resistance for voltage	> 200 KΩ
Digital representation of the input signal	12 bits + sign (bipolar and unipolar)
Conversion principle	successive approximation
Conversion time per channel	< 40 µs
Conversion time for 4 channels	320 µs
Common-mode rejection CMR	typically 90 dB
Basic error limits	2.5 promille
Usual error limits (0 °C ... + 60 °C)	3.0 promille
Screened line lengths	200 m
Current input with 5 V	< 450 mA
Current input with + 15 V	< 50 mA
Front plug	25-polar D plug
Spatial requirements	2 module socket positions on the 35 TP 90 R1 board carrier
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	according to VDE 0160
Weight	0.10 kg
Order number	GJV3073003R1

Accessories:

35 TP 90 R1 board carrier	GJR5143600R1

*) absolute limits

14.3.2 Description

The input unit is only to be operated together with the 35 TP 90 R1.

Every 35 TP 90 basic unit can be equipped with one to two analog modules 35 EA 91 R1 selectively. Each of the analog inputs (module 0/1 to module 2/3) has eight input channels, so that the unit has a total of 16 input channels when equipped with two modules. The basic unit (board carrier) has 4 module socket positions, whereby an analog module 35 EA 91 R1 requires two socket positions.

Meaning of the read out value W (unipolar):

D15	D14	D13	D12	D11	D10	D09	D0ß	D07	D06	D05	D04	D03	D02	D01	D00
0	W	W	W	W	W	W	W	W	W	W	W	W	0	0	0

Meaning of the read out value W (bipolar):

D15	D14	D13	D12	D11	D10	D09	D0ß	D07	D06	D05	D04	D03	D02	D01	D00
V	W	W	W	W	W	W	W	W	W	W	W	W	V	V	V

(V = sign; W = digital value)

The converted value is available after addressing a channel and can be read by the unit as a data word via the MPST bus.

The unit is a passive subscriber on the MPST bus.

Conversion range and value assignment:

Range Analogue value	Converted digital values
0...20 mA	0000H...7FF8H
0 mA...4 mA...+20 mA	8007H...0000H...7FF8H
0...+10 V	0000H...7FF8H
-10 V...0 V...+10 V	800FH...0000H...7FF0H
-5 V...0 V...+5 V	800FH...0000H...7FF0H

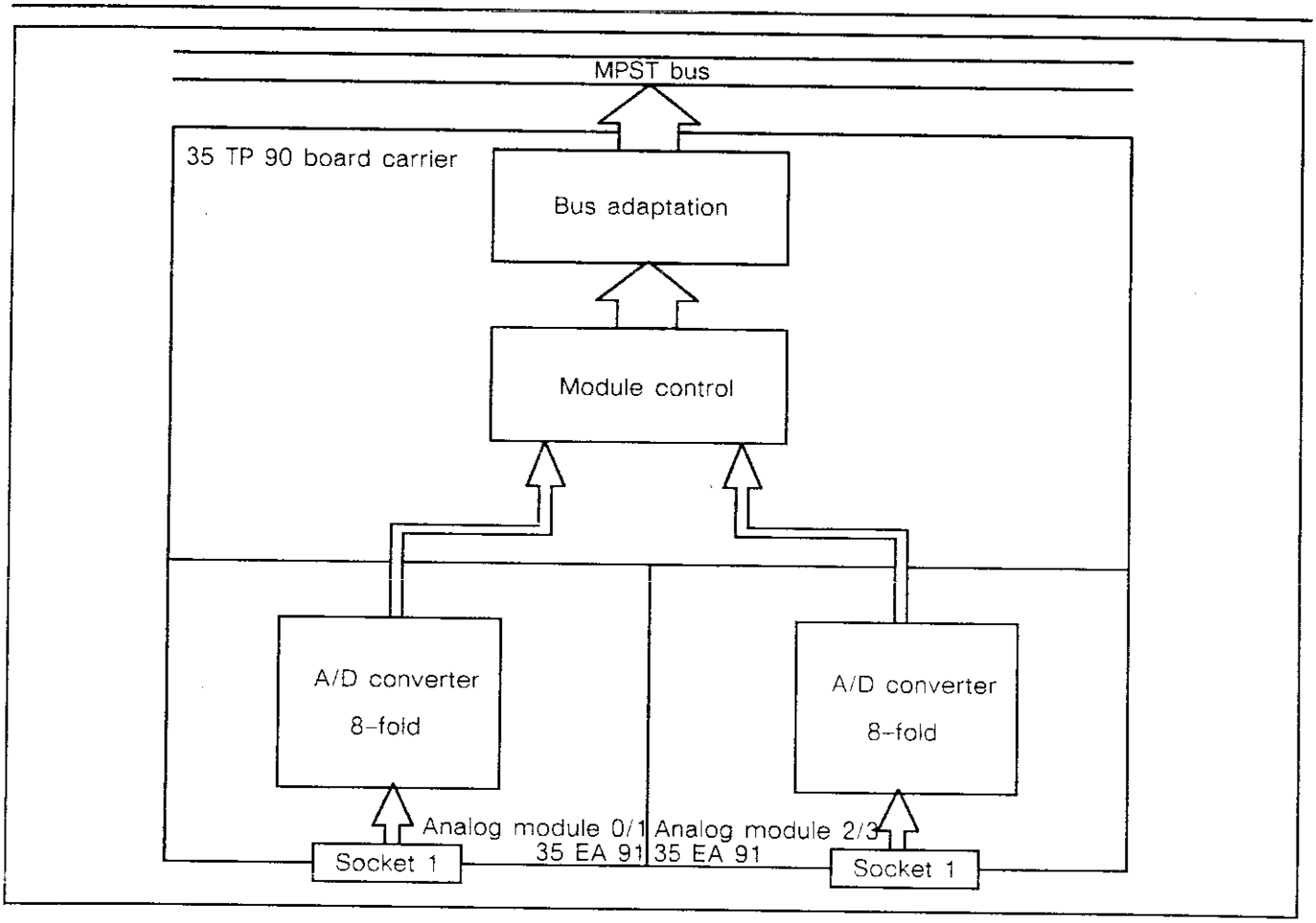


Fig. 14.3-1: Block diagram

14.3.3 Basic settings of the board carrier

14.3.3.1 Clock setting

Each module is to be supplied by the board carrier 35 TP 90 R1 with the clock. To this end, a frequency generated by the 35 TP 90 R1 is selected and switched through to all the modules via the jumper zone JF2.

Example:
The analog input module 35 EA 91 R1 requires a frequency of 2.4576 MHz

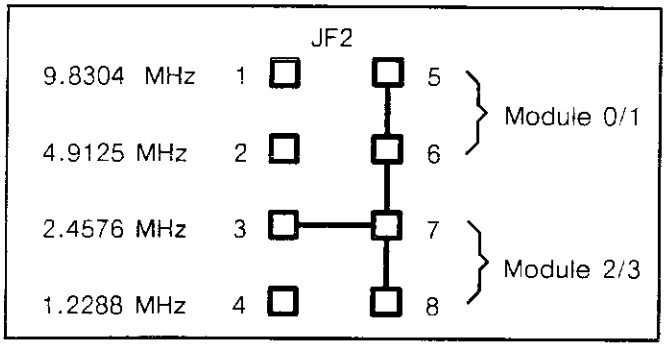


Fig.14.3-2: Jumper zone **JF2**: Clock setting on the 35 TP 90

14.3.3.2 Setting the module arrangement

All the jumpers must be inserted on the jumper zone JF1 for the arrangement of the two analog modules (i.e., the factory setting remains unchanged). The arrangement of the modules 0/1 and 2/3 is thus created on the board carrier.

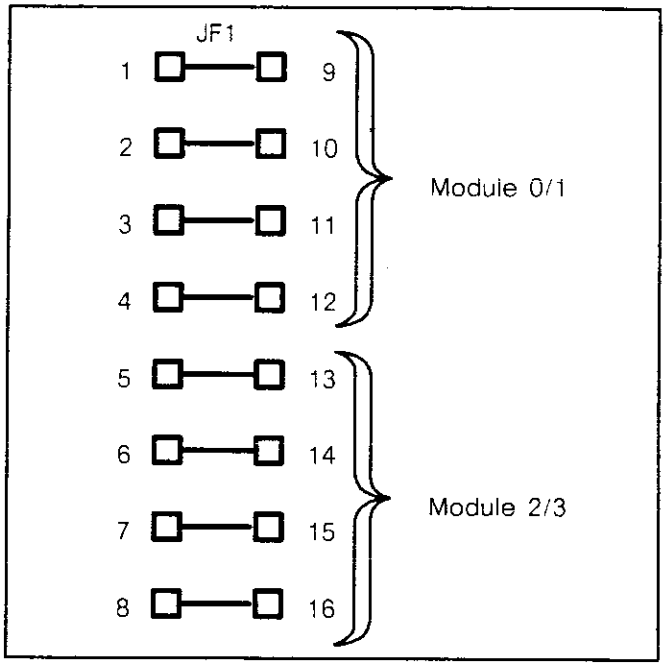


Fig. 14.3-3: Jumper zone **JF1**: Module arrangement on the 35 TP 90 R1

14.3.3.3 Unit address setting

The upper hexadecimal figures (A08 ... A15) are important for addressing the analog input, whereby the uppermost three address bits A13 ... A15 are set permanently to logically 1. The address bits A08 ... A12 are set in the jumper zone JF3 (inserted jumper = logically 0, disconnected jumper = logically 1).

The MPST bus address E800H corresponds to the following bit pattern:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	0	0
← Unit address →													← Module number →		

The unit address shown in the example is to be set in the following way in the jumper zone JF3 on the board carrier::

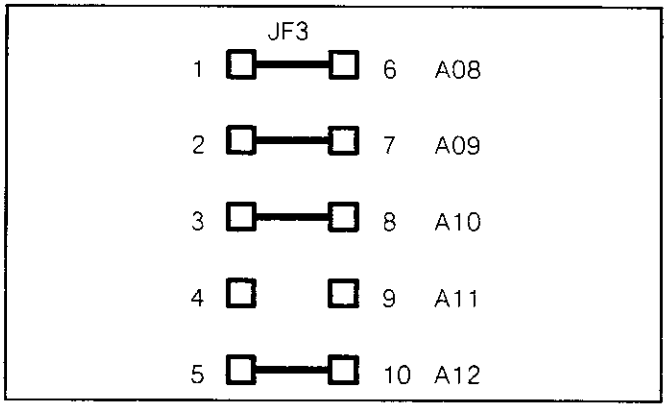


Fig.14.3-4: Jumper zone **JF3**: Clock setting on the 35 TP 90

The MPST bus addresses for the modules and their channels are given in table 14.3-5. The input words (EW) given in the table are to be used to address the module when using the PLC central units.

35TP90/35EA91		MPST bus addresses		
Module	Channel	Offset**	Segment	Input word
0/1	1	E800H	passive subscriber*	EW 00.00
0/1	2	E808H	"	EW 00.04
0/1	3	E810H	"	EW 00.08
0/1	4	E818H	"	EW 00.12
0/1	5	E820H	"	EW 01.00
0/1	6	E828H	"	EW 01.04
0/1	7	E830H	"	EW 01.08
0/1	8	E838H	"	EW 01.12
2/3	1	E804H	"	EW 00.02
2/3	2	E80CH	"	EW 00.06
2/3	3	E814H	"	EW 00.10
2/3	4	E81CH	"	EW 00.14
2/3	5	E824H	"	EW 01.02
2/3	6	E82CH	"	EW 01.06
2/3	7	E834H	"	EW 00.10
2/3	8	E83CH	"	EW 00.14

Table 14.3-5: Address overview

The possibility exists to address the input words without gaps by altering the data block index (DBI) using the PLC central units of the ABB Procontic T300 system. The required alteration is shown in table 14.3-6.

35TP90/35EA91		MPST bus addresses		
Module	Channel	Offset**	Segment	Input words
0/1	1	E800H	passive subscriber*	EW 00.00
0/1	2	E808H	"	EW 00.01
0/1	3	E810H	"	EW 00.02
0/1	4	E818H	"	EW 00.03
0/1	5	E820H	"	EW 00.04
0/1	6	E828H	"	EW 00.05
0/1	7	E830H	"	EW 00.06
0/1	8	E838H	"	EW 00.07
2/3	1	E804H	"	EW 00.08
2/3	2	E80CH	"	EW 00.09
2/3	3	E814H	"	EW 00.10
2/3	4	E81CH	"	EW 00.11
2/3	5	E824H	"	EW 00.12
2/3	6	E82CH	"	EW 00.13
2/3	7	E834H	"	EW 00.14
2/3	8	E83CH	"	EW 00.15

Tabelle 14.3-6: Address overview

*) The address capacity for passive subscribers is addressed by the units 35 ZP 93 and 35 ZE 93 with the segment address 2000 H.

**) The offset corresponds to the T300 bus address.

The module release signals (address bits A00 ... A02) are shown here in table 14.3-7.

Module	A02	A01	A00
0	0	0	0
2	1	0	0

Table 14.3-7 Module release

Setting up the lowest address bits for the respective module can be seen from table 14.3-7 .

Example:
Module 0 and channel 1 are to be read; this correspond to the address E800H (A00, A01 and A02 equals logically 0). The address E804H (A02 equals logically 1, hexadecimal number equals 4) for the same channel and module 2. The same is valid for other channels, whereby the addresses for module 2 are composed in the following way:
Address module 2 (in hexadecimal figures) = address module 1 (in hexadecimal figures) + 4H.

The possible address area of the analog input ranges from E0XXH to FFXXH.

14.3.4 Analog module setting

The analog input module 35 EA 91 R1 is a subprint for the 35 TP 90 R1 board carrier. The spatial requirement of a module amounts to two socket positions, i.e., a maximum of two modules can be plugged into one board carrier. This analog module 35 EA 91 R1 (current/voltage input) must be set to the respective current or voltage range by means of jumpers, before it is plugged into the board carrier.

Current range: 0 mA ... 20 mA
4 mA ... 20 mA (factory settings)
Voltage range: 0 V ... +10 V
- 5 V ... + 5 V
-10 V ... +10 V

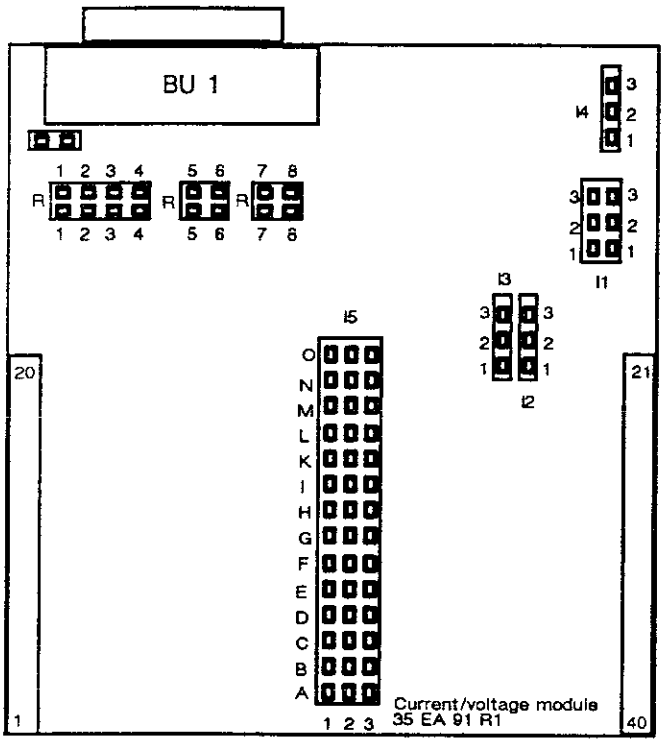


Fig. 14.3-8: Jumper zones of the analog input module 35 EA 91 R1

14.3.4.1 Setting the current ranges

The current ranges 0 mA ... +20 mA and 4 mA ... +20 mA are set with the corresponding jumpers in accordance with tables 14.3-9 and 14.3-10.

If a skirting is present on the analog module instead of the plug connector "R", "R" is not bridged with jumpers but equipped* with the available resistors. The resistors are already installed by the factory in this case. All the settings are valid for all 8 channels of the analog input module.

Current range	Plug connector	Pin No.	Status
0 ... +20 mA	R	1-1...8-8	bridged or * equipped
	I1	1-1	bridged
	I2	2-3	bridged
	I3	1-2	bridged
	I4	1-2	bridged
	I5	A...O;1-2	bridged

Table 14.3-9: Setting the current range 0 mA ... +20 mA

Current range	Plug connector	Pin No.	Status
4 ... +20 mA	R	1-1...8-8	bridged or * equipped
	I1	2-2	bridged
	I2	2-3	bridged
	I3	1-2	bridged
	I4	2-3	bridged
	I5	A...O;1-2	bridged

Table 14.3-10: Setting the current range 4 mA ... +20 mA

14.3.4.2 Setting the voltage ranges

The voltage ranges 0 V ... +10 V, -5 V ... +5 V and -10 V ... +10 V are set with the corresponding jumpers in accordance with tables 14.3-11, 14.3-12 and 14.3-13.

The settings are valid for all 8 channels of the analog input module.

Voltage range	Plug connector	Pin No.	Status
0 ... +10 V	R	1-1...8-8	open
	I1	1-1...3-3	open
	I2	2-3	bridged
	I3	1-2	bridged
	I4	1-2	bridged
	I5	A...O;1-2	bridged

Table 14.3-11: Setting the voltage range 0 V ... +10 V

Voltage range	Plug connector	Pin No.	Status
-5 V...+5 V	R	1-1...8-8	open
	I1	1-1...3-3	open
	I2	1-2	bridged
	I3	1-2	bridged
	I4	1-2	bridged
	I5	A...O;2-3	bridged

Table 14.3-12: Setting the voltage range -5 V ... +5 V

Voltage range	Plug connector	Pin No.	Status
-10 V...+10 V	R	1-1...8-8	open
	I1	1-1...3-3	open
	I2	1-2	bridged
	I3	2-3	bridged
	I4	1-2	bridged
	I5	A...O;2-3	bridged

Table 14.3-13: Setting the voltage range -10 V ... +10 V

14.3.5 Mechanical Structure

Double-size plug-in card in the Europe format 6U, 1 pitch, 160 mm deep.

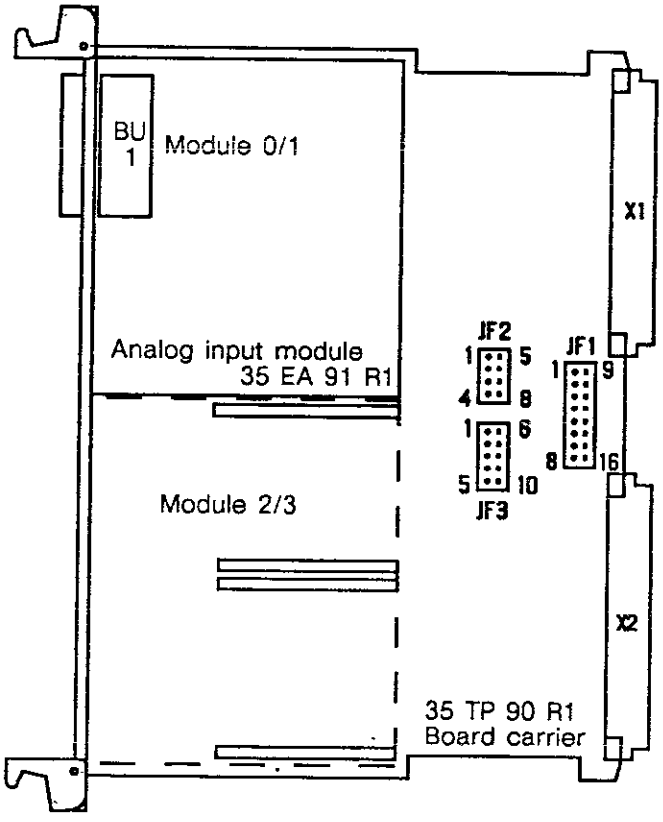


Fig. 14.3-14: Component side (top view)

Plug connectors:

X1, X2	32-polar bus interface in accordance with DIN 41 612, part 2, design C
BU1	25-polar analogue input on the analogue input module 35 EA 91 (AMP HDP 20)

14.3.6 Plug assignment

14.3.6.1 Front plug socket BU1

The analog ground connections (BU1.12 and BU1.24) are to be connected to each other and laid to the respective analog input channel (negative). Pin BU1.1 must be connected (cable sreen), and the jumper on the unit connected.

Pin	Signal	Meaning	Pin	Signal	Meaning
BU1. 1	Screen	Screen	BU1.14	-I1	Channel 1, analog input -
BU1. 2	I1	Channel 1, analog input +	BU1.15	-I2	Channel 2, analog input -
BU1. 3	I2	Channel 2, analog input +	BU1.16	-I3	Channel 3, analog input -
BU1. 4	I3	Channel 3, analog input +	BU1.17	-I4	Channel 4, analog input -
BU1. 5	i4	Channel 4, analog input +	BU1.18	-I5	Channel 5, analog input -
BU1. 6	I5	Channel 5, analog input +	BU1.19	-I6	Channel 6, analog input -
BU1. 7	I6	Channel 6, analog input +	BU1.20	-I7	Channel 7, analog input -
BU1. 8	I7	Channel 7, analog input +	BU1.21	-I8	Channel 8, analog input -
BU1. 9	I8	Channel 8, analog input +	BU1.22	DGND	Digital ground
BU1.10	DGND	Digital ground	BU1.23	UB1	5 V voltage
BU1.11	UB1	5 V voltage	BU1.24	AGND	Analogue ground
BU1.12	AGND	Analogue ground	BU1.25	UB2	15 V voltage
BU1.13	-	-			

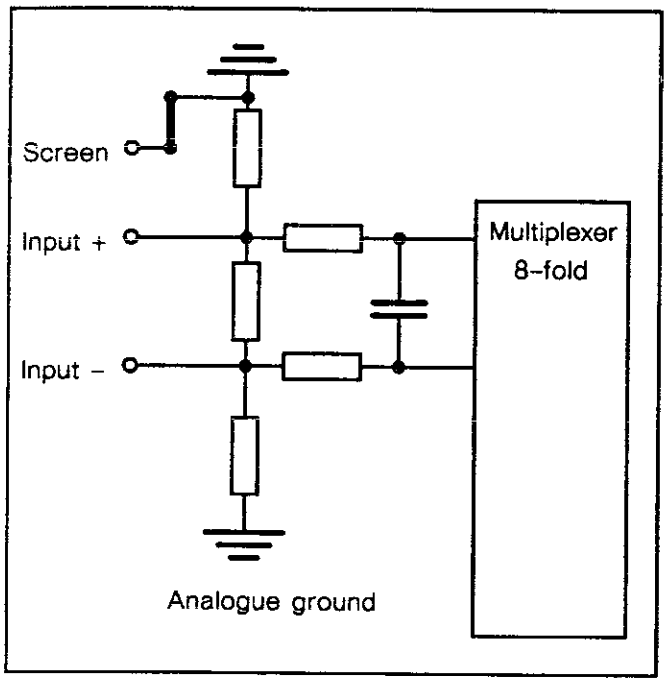


Fig. 14.3-14: Input circuit

14.3.7 Connecting technology and earthing concept

Application-specific instructions are given in order to guaratee the interferencefree data transmission. The ideal earthing concept is given in the following figure, 14.3-15.

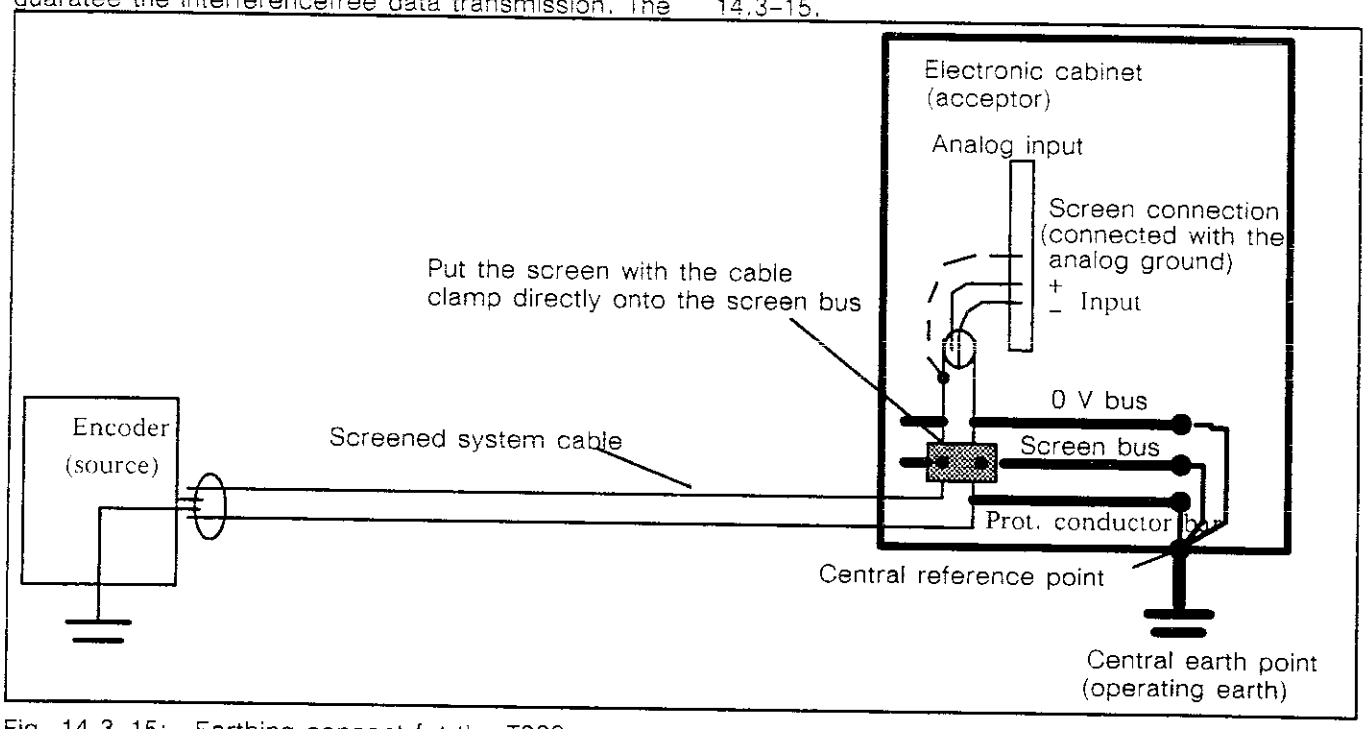
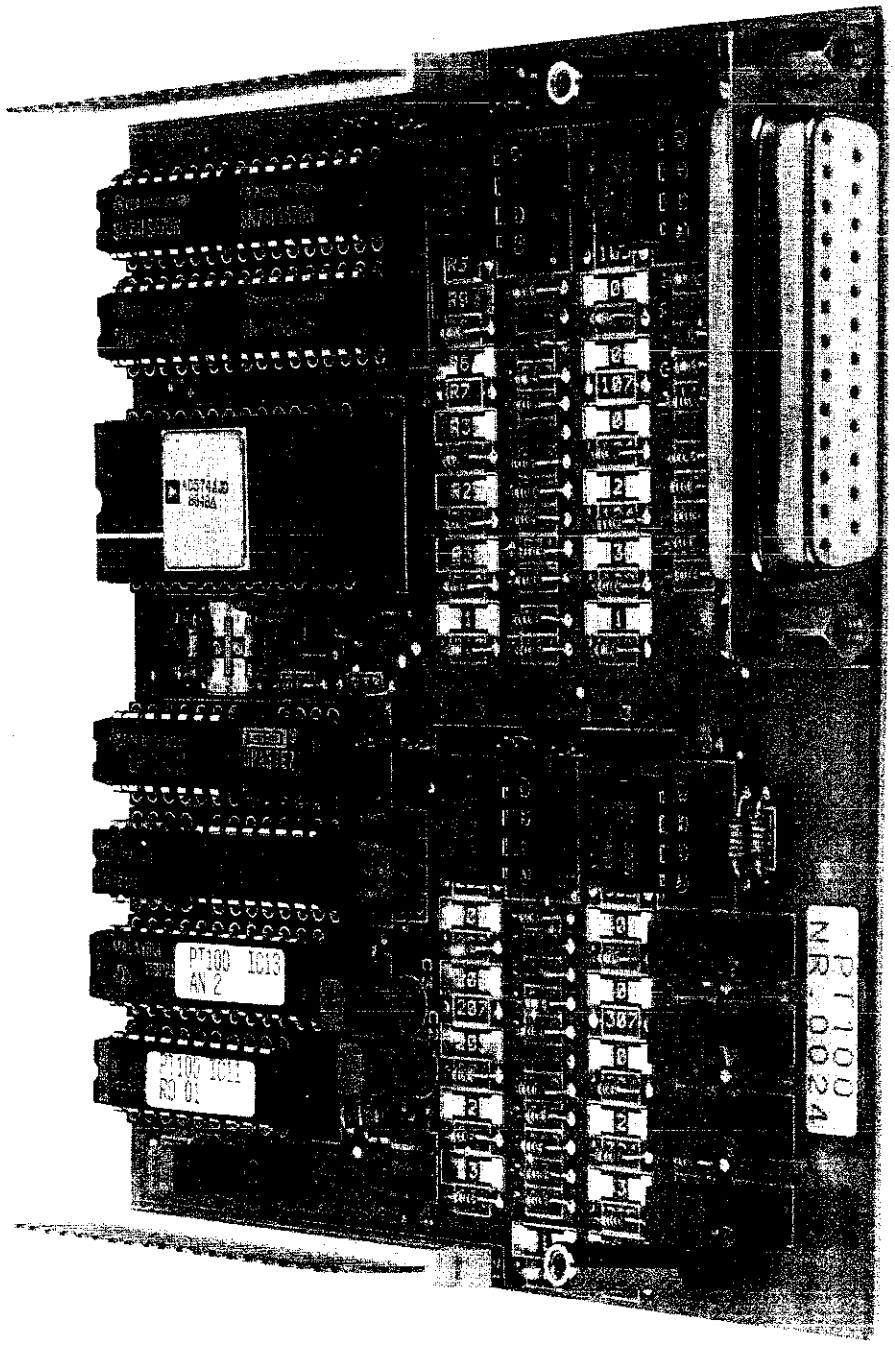


Fig. 14.3-15: Earthing concept fot the T300 system with an analog input

The screened process cable may only be put directly onto the screen bus (cable clamp) for the acceptor (electronic cabinet). The screen is therefore connected on one side only. The screen is also connected at pin 1 of the periphery plug (screen connection). A prerequisite for these measures is very short and strong (at least 16 mm) connections of the screens with a central earth reference point within the cabinet according to Fig. 14.3-15. The connection of the analog ground via the encoder cable on the encoder side only cannot be used for an interferencefree operation. The screened process cable must be laid on the screen bus immediately after it has entered the electronic cabinet. The blank screen is screwed directly onto the screen bus with a cable clamp. The screen bus must be in the lower part of the cabinet.

14.4 Analog input unit 35 EA 92 R1



90 01 90

14.4.1 Technical data

Number of inputs	4 x Pt100 (2 board measurement or 4 board measurement)
Electrical isolation	No
Input range	- 50 °C ... + 150 °C
Input current	2 mA
Digital representation of the input signal	12 bits (unipolar current)
Conversion principle	successive approximation
Conversion time per channel	< 40 µs
Conversion time for 4 channels	160 µs
Common-mode rejection CMR	typically 50 dB
Basic error limits	2.5 promille
Usual error limits (0 °C ... + 60 °C)	6.5 promille
Shielded line lengths	100 m
Current input with 5 V	< 400 mA
Current input with +15 V	< 40 mA
Front plug	25-polar D plug
Spatial requirements	2 module socket positions on the 35 TP 90 R1 board carrier
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F ,
Mechanical stress when installed	in accordance with VDE 0160
Weight of the Pt100 module 35 EA 92 R1	0.10 kg
Order number of the Pt100 module 35 EA 92 R1	GJV3073004R1

Accessories:

35 TP 90 R1 board carrier	GJR5143600R1

14.4.2 Description

The input unit is to be operated together with the 35 TP 90 only.

Each 35 TP 90 basic unit can be equipped with one to two analog modules 35 EA 92 R1 selectively. Each of the analog input modules (module 0/1 to module 2/3) has four input channels, so that the unit has a total of 8 input channels when equipped with two modules. The basic unit (board carrier) has 4 module socket positions, whereby one analog module 35 EA 92 R1 requires two socket positions.

The converted analog value is available after addressing a channel and can be read by the unit as a data word via the MPST bus. The unit is a passive subscriber on the MPST bus.

Calculation formulae:
Digital value (decimal) = DV_D
Digital value (hexadecimal) = DV_H
Temperature in degrees centigrade = T

1. Converting the temperature into a digital value (decimal):

$DV_D = ((T + 50\ °C) / 200\ °C) \times 32768$

Calculation DV_D (Temperature T = 120 °C):
$DV_D = ((120\ °C + 50\ °C) / 200\ °C) \times 32768$
$DV_D = 27853$
$DV_H = 6CCDH$ (displayed value 6CC8H)

2. Conveting a digital value (decimal) into the temperature:

$T = ((DV_D \times 200\ °C) / 32768) - 50\ °C$

Calculating the temperature (DV_D = 2000 corresponds to 07D0H)
$T = ((DV_D \times 200\ °C) / 32768) - 50\ °C$
$T = - 37.8\ °C$

Value assignment:

Temperature	Digital values	Decimal values
- 50 ° C	0000H	0
0 ° C	2000H	8192
+ 50 ° C	4000H	16384
+100 ° C	6000H	24576
+150 ° C	7FF8H	32760

One digit = 200 °C/4096 = 0.049 °C.

The meaning of the read out value (V):

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	V	V	V	V	V	V	V	V	V	V	V	V	0	0	0

Sum V corresponds to D11 ... D00.

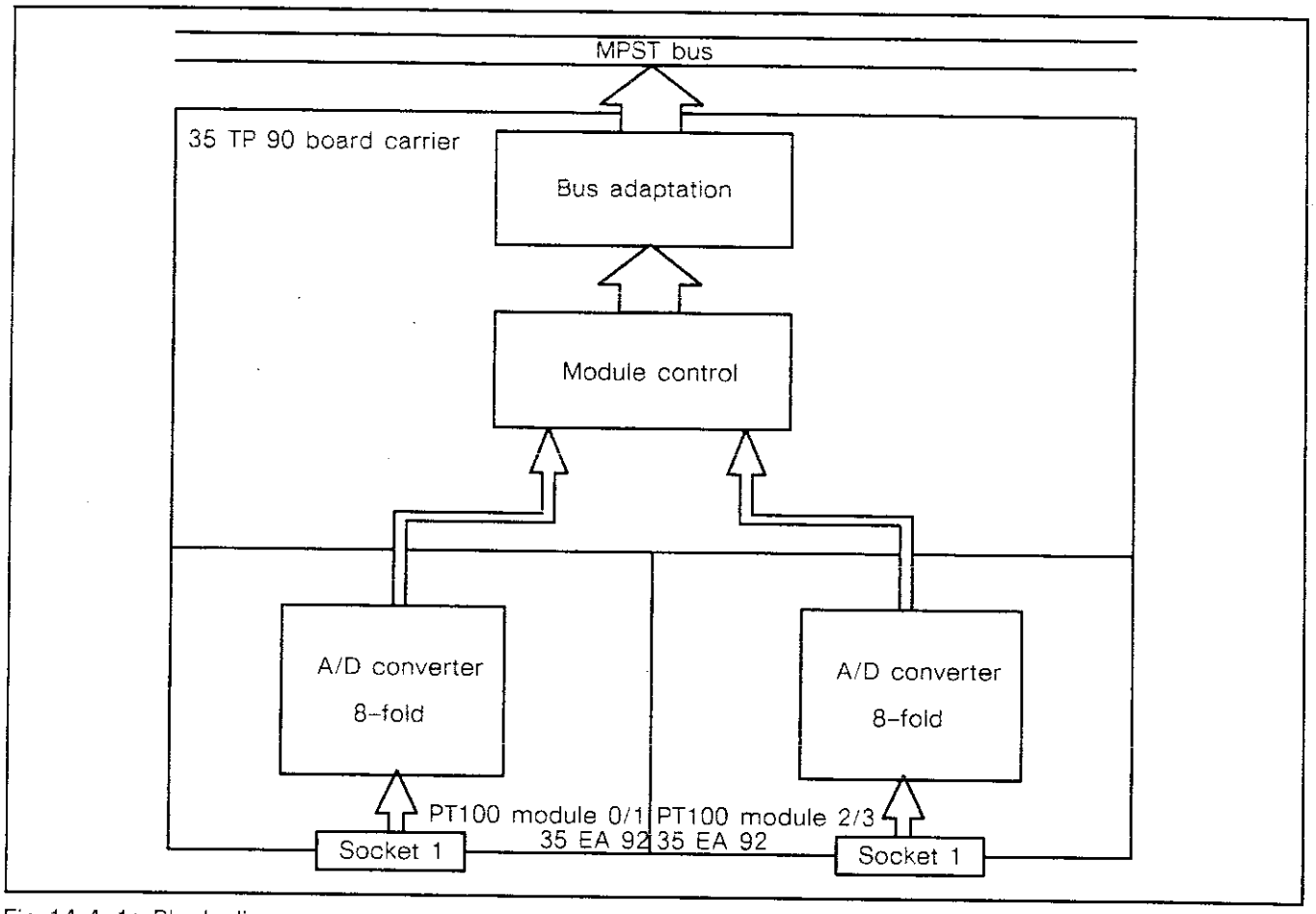


Fig.14.4-1: Block diagram

14.4.3 Basic settings of the board carrier

14.4.3.1 Clock setting

Each module is to be supplied by the 35 TP 90 R1 board carrier with the clock.

Example:
The analog input module 35 EA 91 R1 requires a frequency of 2.4576 MHz. The frequency can be set in the jumper zone JF2.

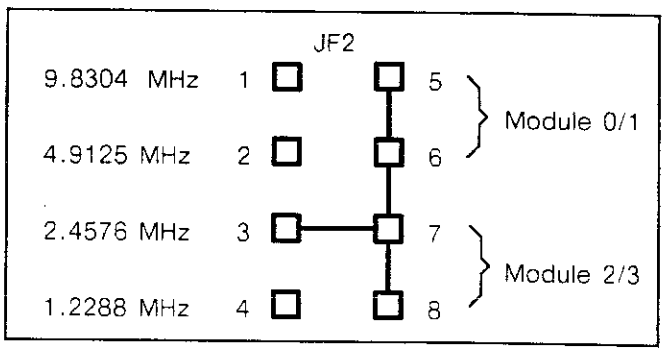


Fig.14.4-2: Jumper zone **JF2**: Clock setting on the 35 TP 90

14.4.3.2 Setting the module arrangement

All the jumpers must be inserted on the jumper zone JF1 for the arrangement of the two Pt100 modules (i.e., the factory setting remains unchanged). The arrangement of the modules 0/1 and 2/3 is thus created on the board carrier.

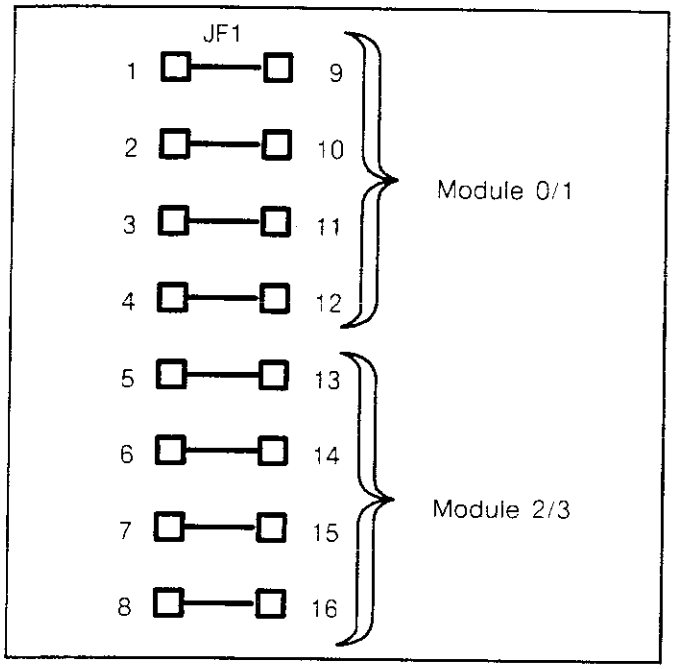


Fig. 14.4-3: Jumper zone **JF1**: Module arrangement on the 35 TP 90 R1

14.4.3.3 Setting the unit address

The upper hexadecimal figures (A08 ... A15) are important for addressing the analog input (Pt100), whereby the uppermost three address bits A13 ... A15 are set permanently to logically 1. The address bits A08 ... A12 are set in the jumper zone JF3 (inserted jumper = logically 0, disconnected jumper = logically 1).

The T300 bus address E800H corresponds to the following bit pattern:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	0	0
← Unit address →													← Module number →		

The unit address shown in the example is to be set in the following way in the jumper zone JF3 on the board carrier:

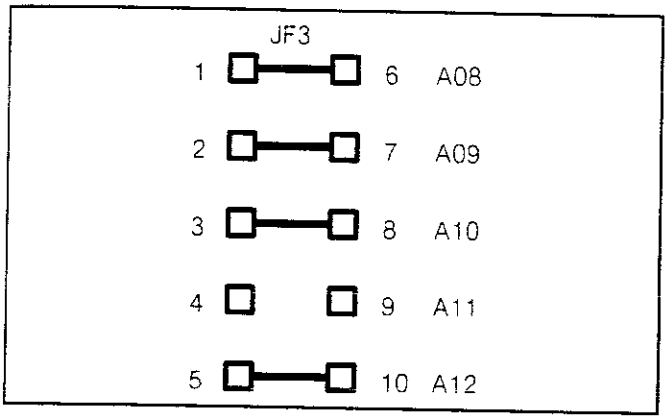


Fig.14.4-4: Jumper zone **JF3**, unit address on the 35 TP 90 R1

The MPST bus addresses for the modules and their channels are given in table 14.4-5. The input words (EW) given in the table are to be used to address the modules when using the PLC central units.

35TP90	35AE92	MPST bus addresses		
Module	Channel	Offset**	Segment	Input word
0/1	1	E800H	passive subscriber *	EW 00.00
0/1	2	E808H	„	EW 00.04
0/1	3	E810H	„	EW 00.08
0/1	4	E818H	„	EW 00.12
2/3	1	E804H	„	EW 00.02
2/3	2	E80CH	„	EW 00.06
2/3	3	E814H	„	EW 00.10
2/3	4	E81CH	„	EW 00.14

Table 14.4-5: Address overview 1

* The address overview for passive subscribers is addressed by the units 35 ZP 93 and 35 ZE 93 with the segment address 2000H .

** Offset corresponds to the ABB Procontic T300 bus address

The possibility exists to address the input words without gaps by altering the data block index (DBI) when using the PLC central units of the ABB Procontic T300 system. The required alteration is shown in table 14.4-6.

35TP90	35EA92	MPST bus addresses		
Module	Channel	Offset **	Segment	Input word
0/1	1	E800H	passive subscriber *	EW 00.00
0/1	2	E808H	„	EW 00.01
0/1	3	E810H	„	EW 00.02
0/1	4	E818H	„	EW 00.03
2/3	1	E804H	„	EW 00.04
2/3	2	E80CH	„	EW 00.05
2/3	3	E814H	„	EW 00.06
2/3	4	E81CH	„	EW 00.07

Table 14.4-6: Address overview 2

The module relaease signals (address bits A00 ... A02) are shown in the following table..

Module	A02	A01	A00
0	0	0	0
2	1	0	0

Table 14.4-7 Module release

Setting the lowest address bits for the respective module can be seen from table 14.4-7.

Example:
Module 0 and channel 1 should be read; this corresponds to the address E800H (A00, A01 and A02 equal logically 0). The address E804H (A02 equals logically 1; the hexadecimal number equals 4) is valid for the same channel and module 2. The same is valid for other channels, whereby the addresses for module 2 are composed in the following way:

Address module 2 (in hexadecimal figures) = address module 1 (in hexadecimal figures) + 4H. The possible address area of the analog input ranges from E0XXH to FFXXH.

14.4.4. Mechanical structure

Unit in the double-sized Eurocard format 160 x 233.4 mm, 1 pitch.

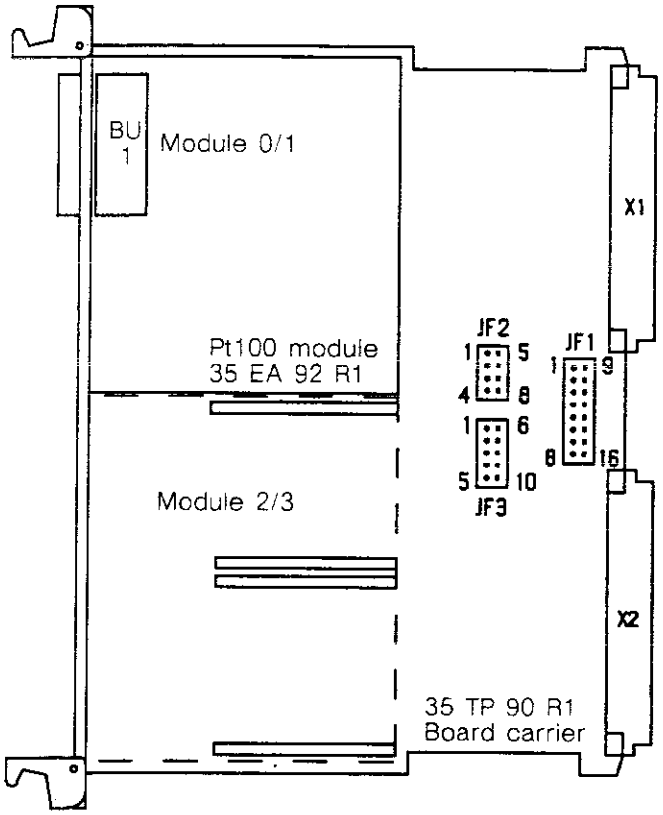


Fig. 14.4-8 Component side (top view)

Plug connectors:

X1, X2	32-polar bus interface in accordance with DIN 41 612, part 2, design C
BU1	25-polar analogue input on the Pt100 module 35 EA 92 (AMP HDP 20)

14.4.5. Plug assignment

14.4.5.1 Front plug socket BU1

Pin BU1.1 must be connected to the process cable screen. All the jumpers on the unit must remain connected (supply status). The Pt100 sensor is connected according to Fig. 14.4-9 for a four-wire connection (compensation of the line length). The lines to U and -U are not required for the respective channel with a two-wire connection (without line compensation).

Pin	Signal	Meaning	Pin	Signal	Meaning
BU1. 1	Screen	Screen	BU1.14	–	–
BU1. 2	I1	Channel 1, current input +	BU1.15	U1	Channel 1, voltage input +
BU1. 3	– U1	Channel 1, voltage input –	BU1.16	– I1	Channel 1, current input –
BU1. 4	I2	Channel 2, current input +	BU1.17	U2	Channel 2, voltage input +
BU1. 5	– U2	Channel 2, voltage input –	BU1.18	– I2	Channel 2, current input –
BU1. 6	I3	Channel 3, current input +	BU1.19	U3	Channel 3, voltage input +
BU1. 7	– U3	Channel 3, voltage input –	BU1.20	– I3	Channel 3, current input –
BU1. 8	I4	Channel 4, current input +	BU1.21	U4	Channel 4, voltage input +
BU1. 9	– U4	Channel 4, voltage input –	BU1.22	– I4	Channel 4, current input –
BU1.10	GND	Ground	BU1.23	UB1	5 V voltage
BU1.11	UB1	5 V voltage	BU1.24	GND	Ground
BU1.12	GND	Ground	BU1.25	UB2	15 V voltage
BU1.13	–	–			

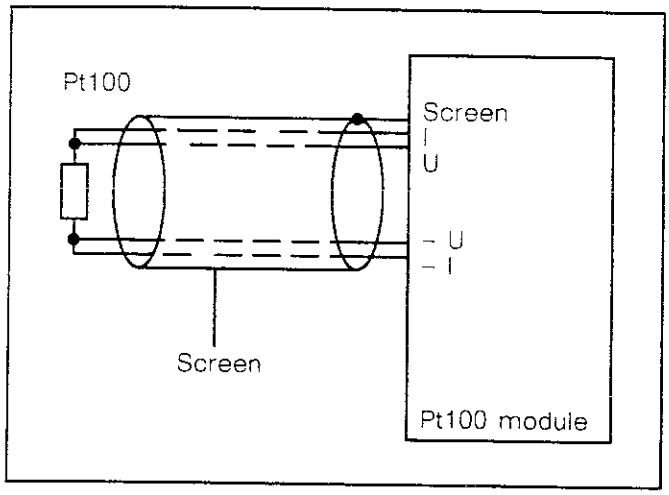


Fig. 14.4-9 Four-wire connection of the Pt100 module

14.4.6 Connecting technology and earthing concept

Application-specific instructions are given in order to guarantee the interference-free data transmission. The ideal earthing concept is given in the following figure, 14.4-10.

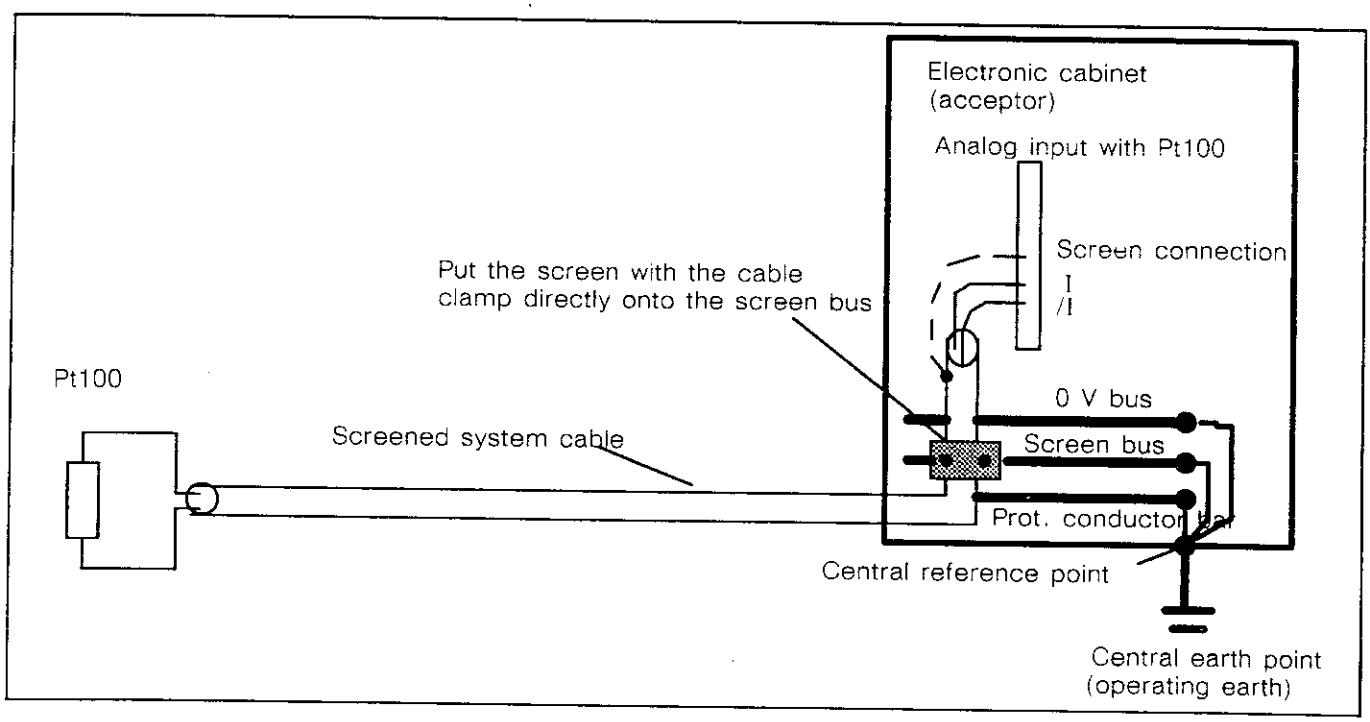
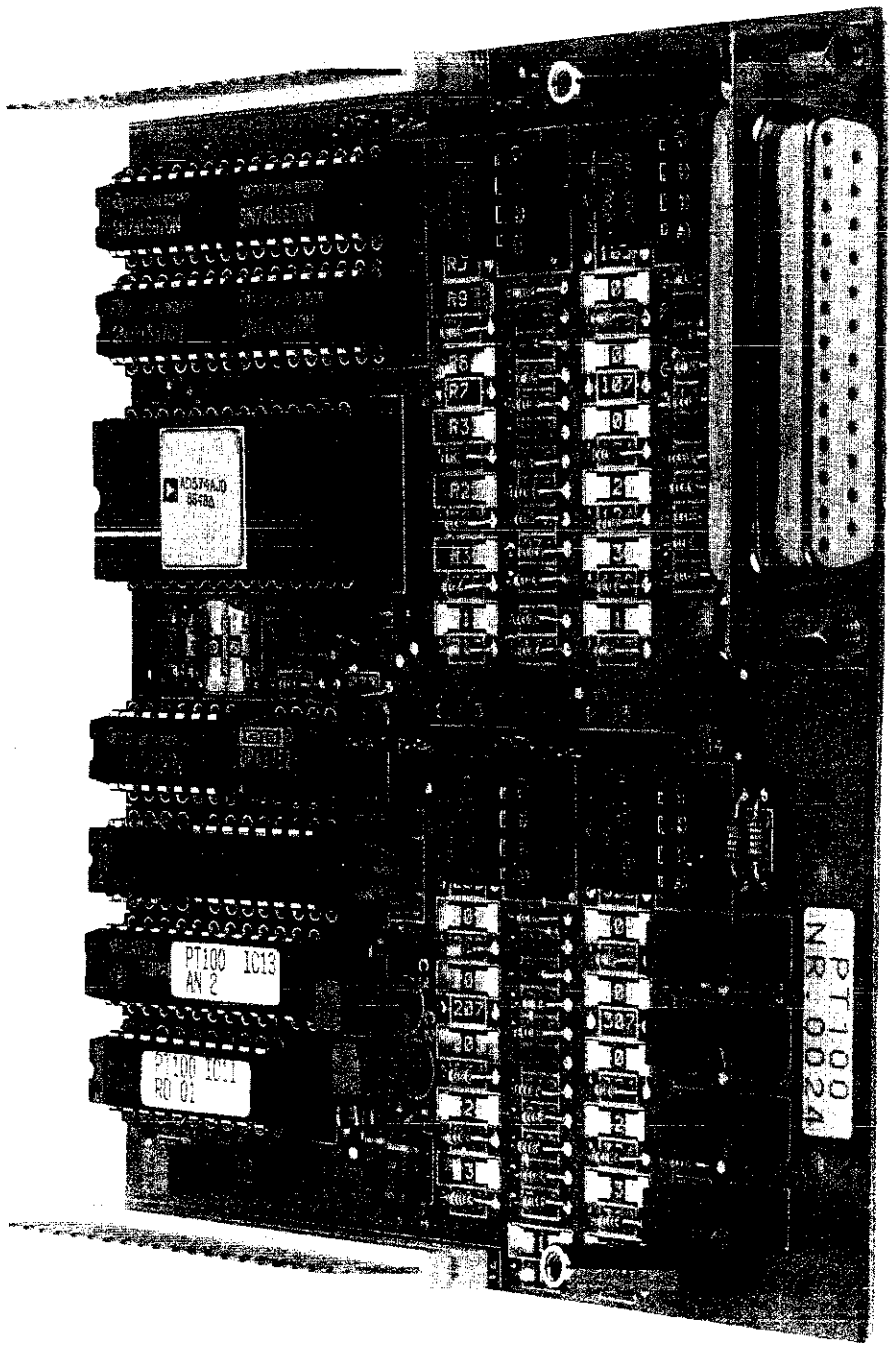


Fig. 14.4-10: Earthing concept fot the T300 system with the analog input 35 EA 92 R1 (Pt100)

The screened process cable may only be put directly onto the screen bus (cable clamp) for the acceptor (electronic cabinet). The screen is therefore connected on one side only. The screen is also connected at pin 1 of the periphery plug (screen connection). A prerequisite for these measures is very short and strong (at least 16 mm^2) connections of the screens with a central earth reference point within the cabinet according to Fig. 14.4-10. The connection of the analog ground via the encoder cable on the encoder side only cannot be used for an interference-free operation. The screened process cable must be laid on the screen bus immediately after it has entered the electronic cabinet. The blank screen is screwed directly onto the screen bus with a cable clamp. The screen bus must be in the lower part of the cabinet.

14.5 Analog input unit 35 EA 92 R2



90 01 90

14.5.1 Technical data

Number of inputs	4 x Pt100 (2 board measurement or 4 board measurement)
Electrical isolation	No
Input range	- 50 °C ... + 400 °C
Input current	2 mA
Digital representation of the input signal	12 bits (unipolar current)
Conversion principle	successive approximation
Conversion time per channel	< 40 µs
Conversion time for 4 channels	160 µs
Common-mode rejection CMR	typically 50 dB
Basic error limits	2.5 promille
Usual error limits (0 °C ... + 60 °C)	6.5 promille
Screned line lengths	100 m
Current input with 5 V	< 400 mA
Current input with +15 V	< 40 mA
Front plug	25-polar D plug
Spatial requirements	2 module socket positions on the 35 TP 90 R1 board carrier
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	in accordance with VDE 0160
Weight	0.10 kg
Order number	GJV3073004R2
Accessories:	
35 TP 90 R1 board carrier	GJR5143600R1

14.5.2 Description

The input unit is to be operated together with the 35 TP 90 only.

Each 35 TP 90 basic unit can be equipped with one to two analog modules 35 EA 92 R2 selectively. Each of the analog input modules (module 0/1 to module 2/3) has four input channels, so that the unit has a total of 8 input channels when equipped with two modules. The basic unit (board carrier) has 4 module socket positions, whereby one analog module 35 EA 92 R2 requires two socket positions.

The converted analog value is available after addressing a channel and can be read by the unit as a data word via the MPST bus. The unit is a passive subscriber on the MPST bus.

Calculation formulae:
Digital value (decimal) = DV_D
Digital value (hexadecimal) = DV_H
Temperature in degrees centigrade = T

1. Converting the temperature into a digital value (decimal):

$DV_D = ((T + 50\ °C) / 450\ °C) \times 32768$

Calculation DV_D (Temperature T = 120 °C):
$DV_D = ((120\ °C + 50\ °C) / 450\ °C) \times 32768$
$DV_D = 12379$
$DV_H = 305BH$ (displayed value 3058H)

2. Conveting a digital value (decimal) into the temperature:

$T = ((DV_D \times 450\ °C) / 32768) - 50\ °C$

Calculating the temperature (DV_D = 2000 corresponds to 07D0H)
$T = ((DV_D \times 450\ °C) / 32768) - 50\ °C$
$T = - 22.5\ °C$

Value assignment:

Temperature	Digital values	Decimal values
- 50 ° C	0000H	0
0 ° C	0E38H	3640
+100 ° C	2AAAH	10922
+200 ° C	471CH	18204
+400 ° C	7FF8H	32760

One digit = 450 °C/4096 = 0.11 °C.

The meaning of the read out value (V):

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	V	V	V	V	V	V	V	V	V	V	V	V	0	0	0

Sum V corresponds to D11 ... D00.

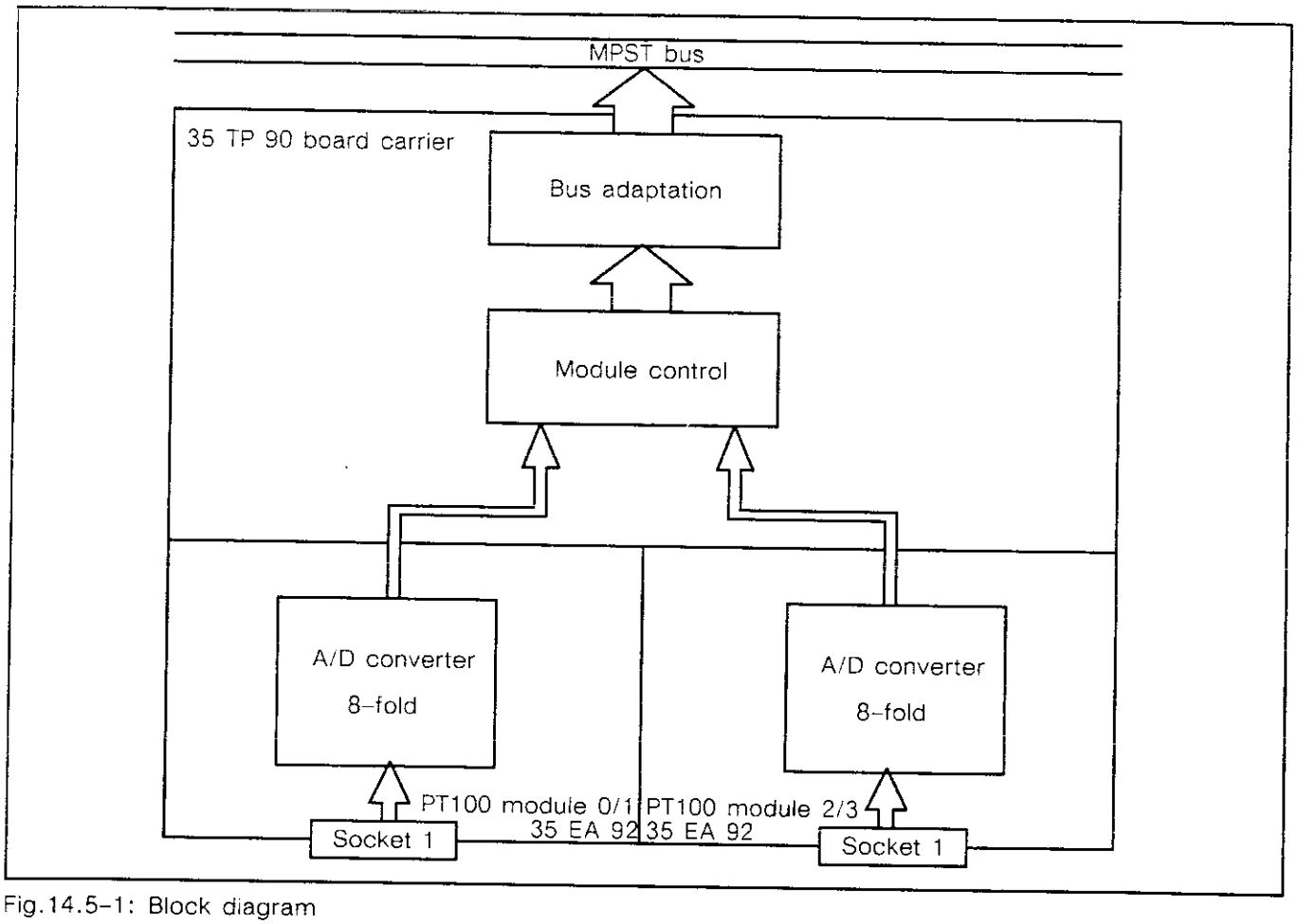


Fig.14.5-1: Block diagram

14.5.3 Basic settings of the board carrier

14.5.3.1 Clock setting

Each module is to be supplied by the 35 TP 90 R2 board carrier with the clock. To this end, a frequency generated by the 35 TP 90 R2 is selected and switched through to all the modules via the jumper zone JF2.

The analog input module 35 EA 91 R2 requires a frequency of 2.4576 MHz

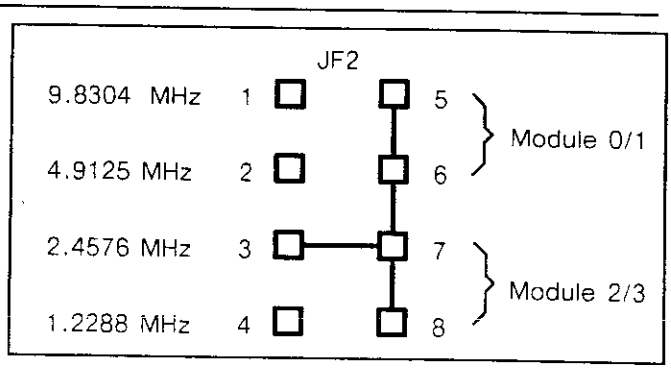


Fig.14.5-2: Jumper zone JF2: Clock setting on the 35 TP 90

14.5.3.2 Setting the module arrangement

All the jumpers must be inserted on the jumper zone JF1 for the arrangement of the two Pt100 modules (i.e., the factory setting remains unchanged). The arrangement of the modules 0/1 and 2/3 is thus created on the board carrier.

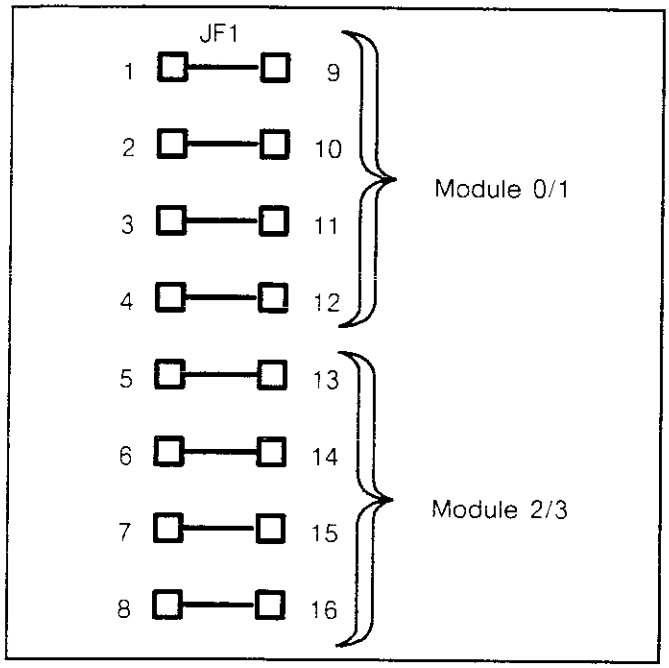


Fig. 14.5-3: Jumper zone JF1: Module arrangement on the 35 TP 90 R1

14.5.3.3 Setting the unit address

The upper hexadecimal figures (A08 ... A15) are important for addressing the analog input (Pt100), whereby the uppermost three address bits A13 ... A15 are set permanently to logically 1. The address bits A08 ... A12 are set in the jumper zone JF3 (inserted jumper=logically 0, disconnected jumper = logically 1).

The T300 bus address E800H corresponds to the following bit pattern:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	0	1	0	0	0	X	X	X	X	X	0	0	0
← Unit address →													← Module number →		

The unit address shown in the example is to be set in the following way in the jumper zone JF3 on the board carrier:

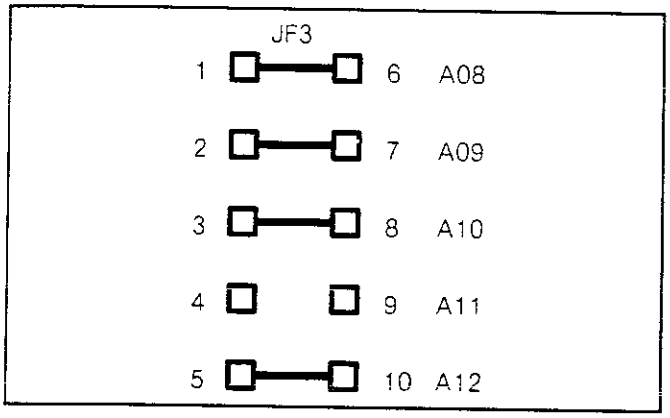


Fig.14.5-4: Jumper zone JF3, unit address on the 35 TP 90 R1

The MPST bus addresses for the modules and their channels are given in table 14.5-4. The input words (EW) given in the table are to be used to address the modules when using the PLC central units.

35TP90	35EA92	MPST bus addresses		
Module	Channel	Offset **	Segment	Input word
0/1	1	E800H	passive subscriber *	EW 00.00
0/1	2	E808H	„	EW 00.04
0/1	3	E810H	„	EW 00.08
0/1	4	E818H	„	EW 00.12
2/3	1	E804H	„	EW 00.02
2/3	2	E80CH	„	EW 00.06
2/3	3	E814H	„	EW 00.10
2/3	4	E81CH	„	EW 00.14

Table 14.5-5: Address overview 1

* The address overview for passive subscribers is addressed by the units 35 ZP 93 and 35 ZE 93 with the segment address 2000H .

** Offset corresponds to the ABB Procontic T300 bus address

The possibility exists to address the input words without gaps by altering the data block index (DBI) when using the PLC central units of the ABB Procontic T300 system.The required alteration is shown in table 14.5-6 .

35TP90	35EA92	MPST bus addresses		
Module	Channel	Offset **	Segment	Input word
0/1	1	E800H	passive subscriber *	EW 00.00
0/1	2	E808H	„	EW 00.01
0/1	3	E810H	„	EW 00.02
0/1	4	E818H	„	EW 00.03
2/3	1	E804H	„	EW 00.04
2/3	2	E80CH	„	EW 00.05
2/3	3	E814H	„	EW 00.06
2/3	4	E81CH	„	EW 00.07

Table 14.5-6: Address overview 2

The module relaease signals (address bits A00 ... A02) are shown in the following table.

Module	A02	A01	A00
0	0	0	0
2	1	0	0

Table 14.5-7 Module release

Setting the lowest address bits for the respective module can be seen from table 14.5-7.

Example:
Module 0 and channel 1 should be read; this corresponds to the address E800H (A00, A01 and A02 equal logically 0). The address E804H (A02 equals logically 1; the hexadecimal number equals 4) is valid for the same channel and module 2. The same is valid for other channels, whereby the addresses for module 2 are composed in the following way:

Address module 2 (in hexadecimal figures) = address module 1 (in hexadecimal figures) + 4H. The possible address area of the analog input ranges from E0XXH to FFXXH.

14.5.4. Mechanical structure

Unit in the double-sized Eurocard format 160 x 233.4 mm, 1 pitch.

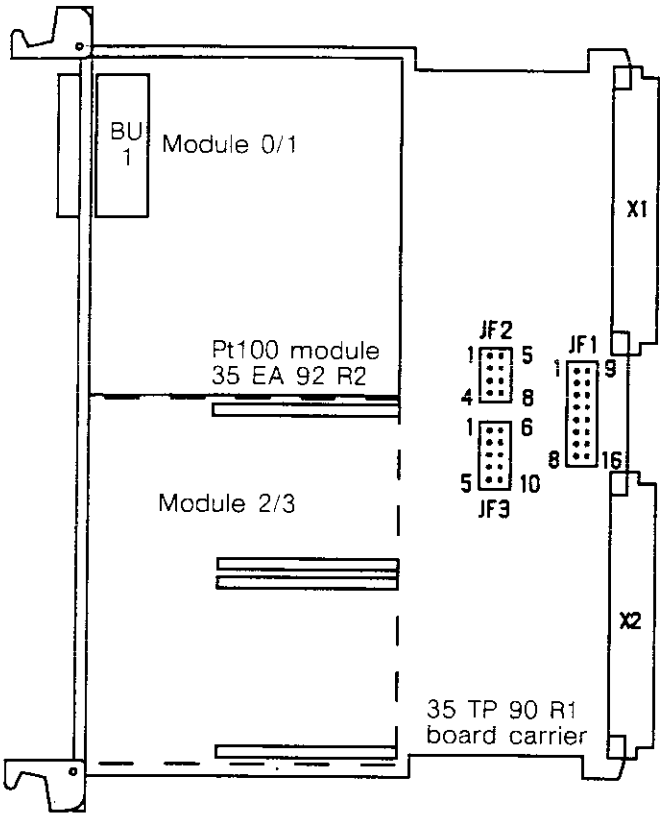


Fig. 14.5-8 Component side (top view)

Plug connectors:

X1, X2	32-polar bus interface in accordance with DIN 41 612, part 2, design C
BU1	25-polar analogue input on the Pt100 module 35 EA 92 (AMP HDP 20)

14.5.5. Plug assignment

14.5.5.1 Front plug socket BU1

Pin BU1.1 must be connected to the process cable screen. All the jumpers on the unit must remain connected (supply status). The Pt100 sensor is connected according to Fig. 14.5-9 for a four-wire connection (compensation of the line length). The lines to U and -U are not required for the respective channel with a two-wire connection (without line compensation).

Pin	Signal	Meaning	Pin	Signal	Meaning
BU1. 1	Screen	Screen	BU1.14	–	
BU1. 2	I1	Channel 1, current input +	BU1.15	U1	Channel 1, voltage input +
BU1. 3	– U1	Channel 1, voltage input –	BU1.16	– I1	Channel 1, current input –
BU1. 4	I2	Channel 2, current input +	BU1.17	U2	Channel 2, voltage input +
BU1. 5	– U2	Channel 2, voltage input –	BU1.18	– I2	Channel 2, current input –
BU1. 6	I3	Channel 3, current input +	BU1.19	U3	Channel 3, voltage input +
BU1. 7	– U3	Channel 3, voltage input –	BU1.20	– I3	Channel 3, current input –
BU1. 8	I4	Channel 4, current input +	BU1.21	U4	Channel 4, voltage input +
BU1. 9	– U4	Channel 4, voltage input –	BU1.22	– I4	Channel 4, current input –
BU1.10	GND	Ground	BU1.23	UB1	5 V voltage
BU1.11	UB1	5 V voltage	BU1.24	GND	Ground
BU1.12	GND	Ground	BU1.25	UB2	15 V voltage
BU1.13	–	–			

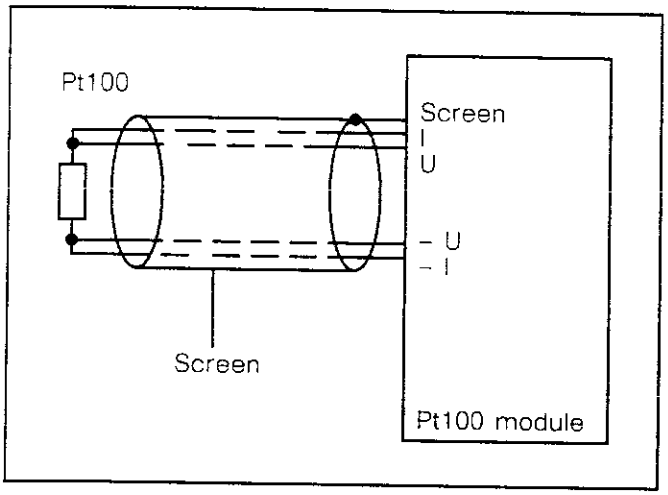


Fig. 14.5-9 Four-wire connection of the Pt100 module

14.5.6 Connecting technology and earthing concept

Application-specific instructions are given in order to guarantee the interference-free data transmission and the EMC-resistance. The ideal earthing concept is given in the following figure, 14.5-10.

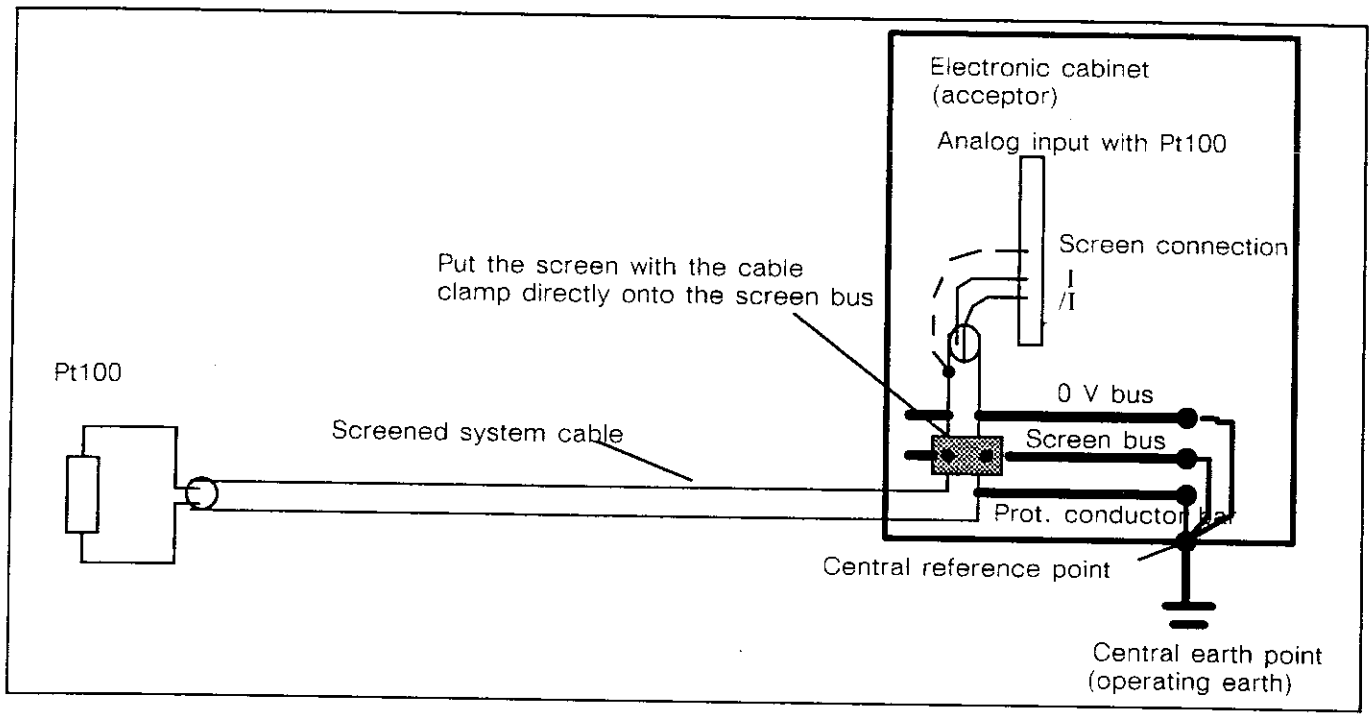


Fig. 14.5-10: Earthing concept fot the T300 system with the analog input 35 EA 92 R2 (Pt100)

The screened process cable may only be put directly onto the screen bus (cable clamp) for the acceptor (electronic cabinet). The screen is therefore connected on one side only. The screen is also connected at pin 1 of the periphery plug (screen connection). A prerequisite for these measures is very short and strong (at least 16 mm) connections of the screens with a central earth reference point within the cabinet according to Fig. 14.5-10. The connection of the analog ground via the encoder cable on the encoder side only cannot be used for an interference-free operation. The screened process cable must be laid on the screen bus immediately after it has entered the electronic cabinet. The blank screen is screwed directly onto the screen bus with a cable clamp. The screen bus must be in the lower part of the cabinet.

15 Binary output units

35 AB 90 R1: Binary output unit,	transistor outputs	24 V DC, 4 mA,	64-fold.
35 SK 90 R3: Flat system cable.			
35 SK 91 R3: Flat system cable.			
35 SK 92 R3: Flat system cable.			
07 RM 61 R1: Switch stage,	relay outputs	220 V AC, 4 A,	electrically isolated, 4-fold.
07 LM 61 R1: Lamp driver stage,	transistor outputs	24 V DC, 210 mA,	electrically isolated, 8-fold.
07 TM 61 R1: Switch stage,	transistor outputs	24 V DC, 2 A,	electrically isolated, 4-fold.
07 RM 61 R2: Switch stage,	reedrelay outputs	60 V DC, 100 mA,	electrically isolated, 8-fold.
35 AB 94 R1: Binary output unit,	transistor outputs	24 V DC, 100 mA,	32-fold.
35 AB 95 R1: Binary output unit,	transistor outputs	24 V DC, 500 mA,	electrically isolated, 32-fold.
35 AB 96 R1: Binary output unit,	relay outputs	220VAC/48VDC/24VDC,	electrically isolated, 16-fold.
35 AB 97 R2: Binary output unit,	transistor outputs	24 V DC, 2 A,	electrically isolated, 16-fold.

15.1 Binary output unit 35 AB 90 R1 ..... 15.1- 1
15.1.1 Technical data 15.1- 2
15.1.2 Description 15.1- 3
15.1.3 Mechanical structure 15.1- 3
15.1.4 Settings 15.1- 4

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15.2.1 Flat system cable 35 SK 90 R* 15.2- 1
15.2.2 Flat system cable 35 SK 91 R* 15.2- 1
15.2.3 Flat system cable 35 SK 92 R* 15.2- 2
15.2.4 Relay switch stage 07 RM 61 . 15.2- 3
15.2.5 Lamp driver stage 07 LM 61 .. 15.2- 5
15.2.6 Transistor switch stage 07 TM 61 ..... 15.2- 7
15.2.7 Reed relay switch stage 07 AM 62 ..... 15.2- 9

15.3 Binary output unit 35 AB 94 R1 ..... 15.3- 1
15.3.1 Technical data 15.3- 2
15.3.2 Description 15.3- 3
15.3.3 Unit addresses 15.3- 3
15.3.3.1 Address setting 15.3- 3
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15.3.3.3 Assembly positions 15.3- 4
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15.3.5.1 MPST bus interface, plug X1, X2 ..... 15.3- 5
15.3.5.2 Front plug X3 ..... 15.3- 6

15.4 Binary output unit 35 AB 95 R1 ..... 15.4- 1
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15.4.2 Description 15.4- 3
15.4.3 Unit addresses 15.4- 3
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15.6 Binary output unit 35 AB 97 R2 ..... 15.6- 1
15.6.1 Technical data 15.6- 3
15.6.2 Description 15.6- 4
15.6.3 Unit addresses 15.6- 4
15.6.3.1 Address setting 15.6- 4
15.6.3.2 Address division 15.6- 4
15.6.3.3 Assembly positions 15.6- 4
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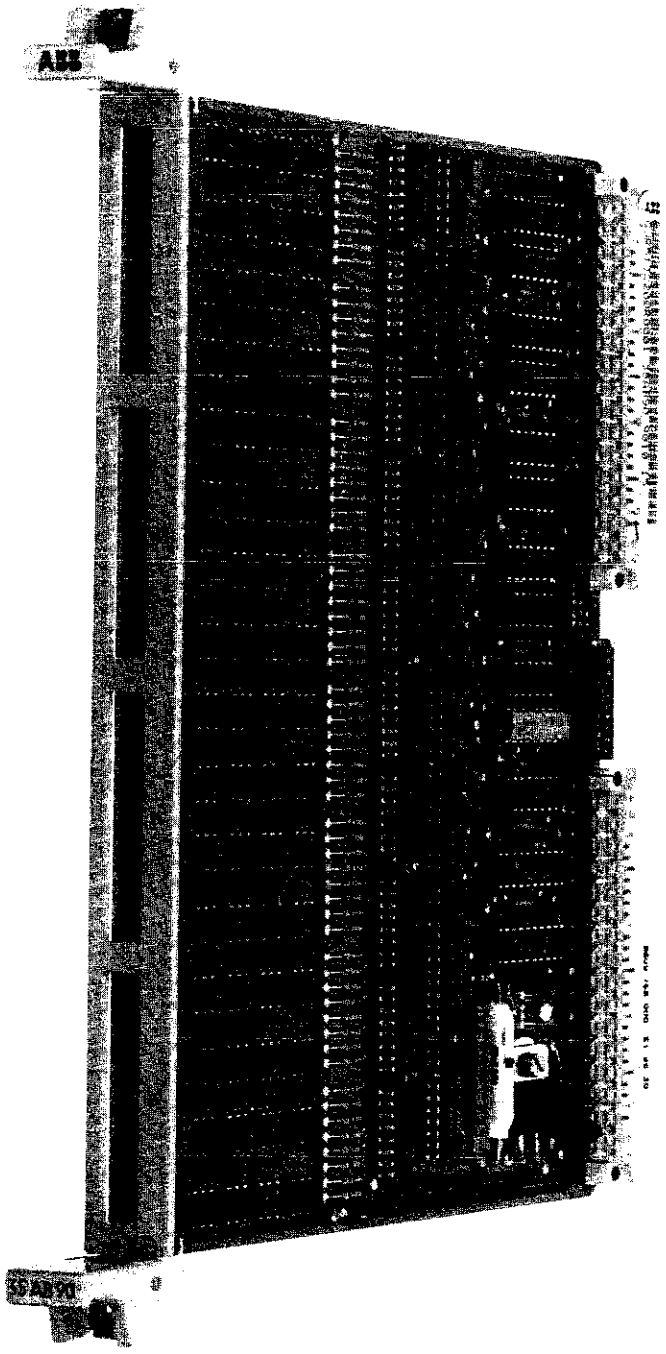
15.6.5 Plug assignment 15.6- 6
15.6.5.1 MPST bus interface, plugs X1, X2 ..... 15.6- 6
15.6.5.2 Front plug X3 ..... 15.6- 7
15.6.6 Short-circuit and overload treatment 15.6- 7

15.1 Binary output unit 35 AB 90 R1



15.1.1 Technical data

Supply voltage	+5 V + 5 % (TTL)
Current input	< 1.5 A
Signal level of all control signals, Data and address signals	TTL
Max. ouput current, optocoupler transistor	4 mA
Reverse voltage, optocoupler transistor	+24 V + 30 %
Max. voltage reduction for the optocoupler transistor	2 V
Test voltage	2 kV eff.
Permitted temperature range	0 °C ... +55 °C

15.1.2 Description

The ouput unit 35 AB 90 is the interface for binary signals between the control ABB Procontic T300 and the process.

64 output channels, which are galvanically isolated via optocouplers, are available on one unit. These are combined in groups of 16 channels each and are connected to the various output modules via prefabricated ribbon cables.

The output is a passive subscriber on the MPST bus.

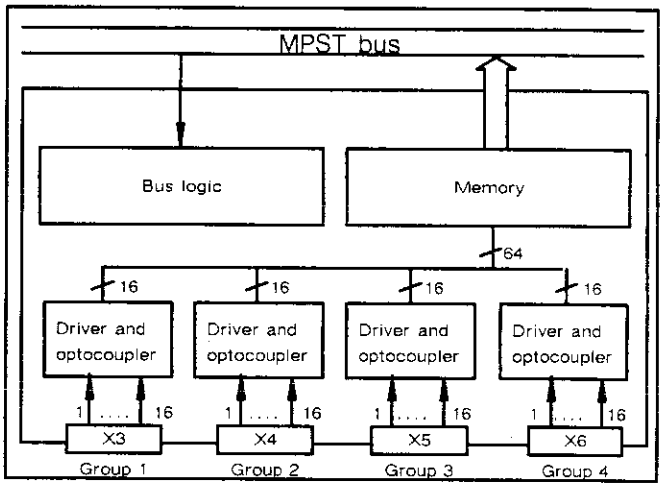


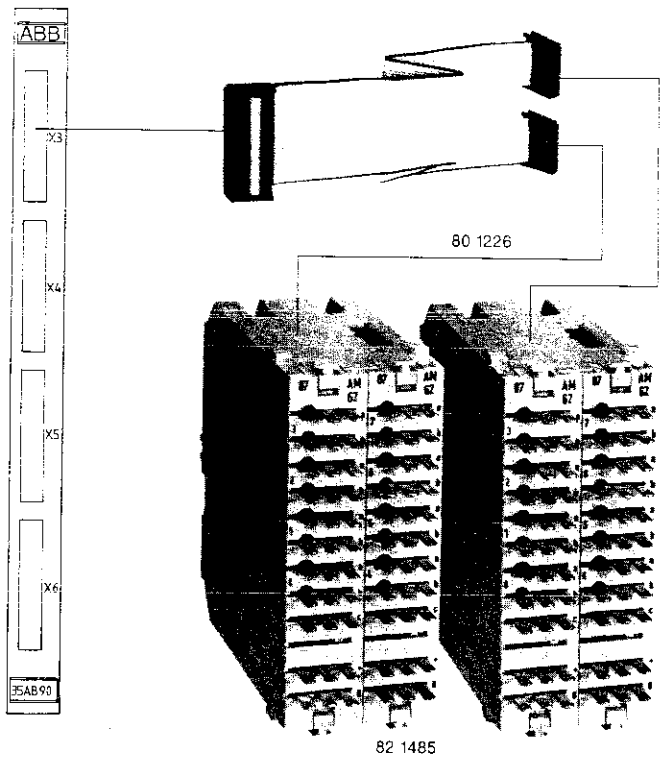
Fig. 15.1-1 Block diagram

15.1.3 Mechanical structure

Mechanical dimensions according to DIN 41 494, part 2	233.4 x 160 mm H x W
Width of the front panel	4 R = 20.32 mm
Connecting elements on the rear according to DIN 41 612, part 2, design C	2 x 32-polar plug connectors
Connection elements on the front side	4 x 34-polar Berg connector, Quickie type
Dimensions	1 pitch
Weight	0.5 kg
Order number	GJR5132200R1

Overview 1

Connection of the output modules (e.g. 07 LM 61) via system cable 35 SK 90 to the output unit 35 AB 90



output module channel 24–31 chanel 16–23

When providing your own system cable or when using non-ABB output modules it must be noted that the emitters of the phototransistor always have to be connected to the right contact row of the Berg plug connector (seen from the front panel). The collectors are connected to the left row.

5.3.4 Settings

The module can be driven byte by byte as well as word by word.

Perequisit for switching through of the data bus from the data bus to the outputs:

1. W = Low
2. I/O = Low
3. A13, A14, A15, = HIGH

Data transfer in case of '$\overline{\text{BOV}}$' line signal change from 1 to 0.

The address of the module set by means of a 10-polar DIL switch. The switch position OFF represents a logical 1; the position ON represents a logical 0.

The data lines A00, A01, A02 as well as WO are controlled so that the data are output to the Berg connectors word by word (WO = 1) or byte by byte (WO = 0).

Table for "WO" = 0 (Byte prompting)

A00	A01	A02	A03 ... A12	A13	A14	A15	Signals on Berg plugs
0	0	0	x ... x	1	1	1	X3, low byte
1	0	0	x ... x	1	1	1	X3, high byte
0	1	0	x ... x	1	1	1	X4, low byte
1	1	0	x ... x	1	1	1	X4, high byte
0	0	1	x ... x	1	1	1	X5, low byte
1	0	1	x ... x	1	1	1	X5, high byte
0	1	1	x ... x	1	1	1	X6, low byte
1	1	1	x ... x	1	1	1	X6, high byte

Table for "WO" = 1 (Word prompting):

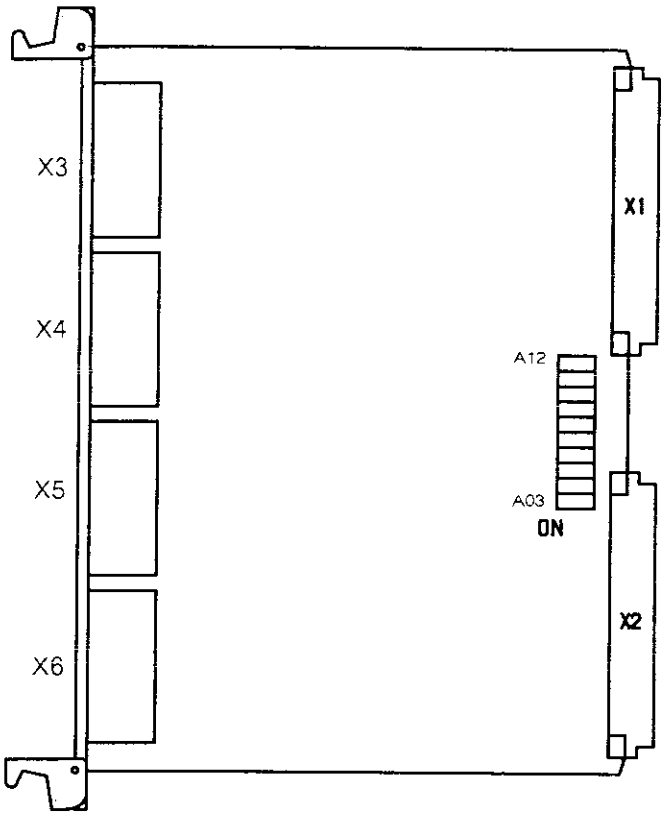
A00	A01	A02	A03 ... A12	A13	A14	A15	Signals on Berg plug
0	0	0	x ... x	1	1	1	X3
0	1	0	x ... x	1	1	1	X4
0	0	1	x ... x	1	1	1	X5
0	1	1	x ... x	1	1	1	X6

x for A3 to A12 means either 1 or 0.

Setting of the unit address

Overview 2

Mechanical structure 35 AB 90



X1 MPST bus
X2 MPST bus
} 32-polar MPST bus interface according to DIN 41 612, part 2, design C

X3 Output cable Channels 0–15
X4 Output cable Channels 16–31
X5 Output cable Channels 32–47
X6 Output cable Channels 48–63
} 34-polar plug connectors system cable 35 SK 90, 35 SK 91, 35 SK 92

Fig. 13.1-2 Component side (top view)

Overview 3

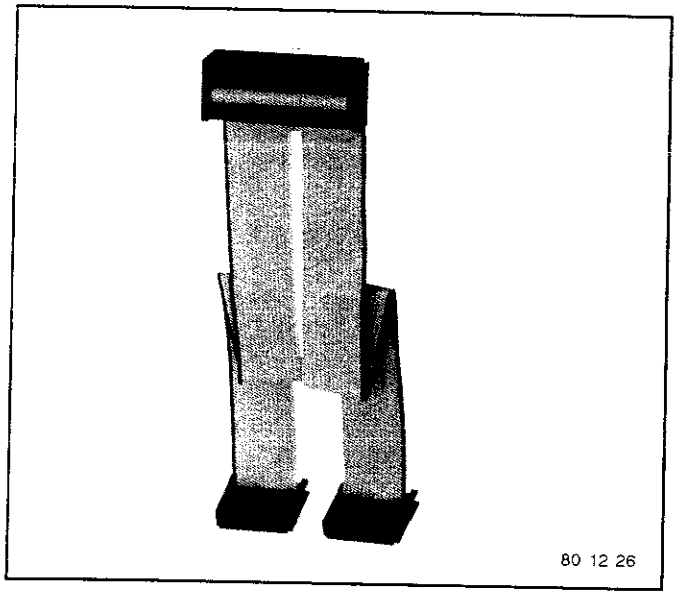
Plug assignment of 35 AB 90

Plug	Channel	Pin	Plug	Channel	Pin
X3	0	33–34	X4	16	33–34
	1	31–32		17	31–32
	2	29–30		18	29–30
	3	27–28		19	27–28
	4	25–26		20	25–26
	5	23–24		21	23–24
	6	21–22		22	21–22
	7	19–20		23	19–20
	8	15–16		24	15–16
	9	13–14		25	13–14
	10	11–12		26	11–12
	11	9–10		27	9–10
	12	7– 8		28	7– 8
	13	5– 6		29	5– 6
	14	3– 4		30	3– 4
	15	1– 2		31	1– 2

Plug	Channel	Pin	Plug	Channel	Pin
X5	32	33–34	X6	48	33–34
	33	31–32		49	31–32
	34	29–30		50	29–30
	35	27–28		51	27–28
	36	25–26		52	25–26
	37	23–24		53	23–24
	38	21–22		54	21–22
	39	19–20		55	19–20
	40	15–16		56	15–16
	41	13–14		57	13–14
	42	11–12		58	11–12
	43	9–10		59	9–10
	44	7– 8		60	7– 8
	45	5– 6		61	5– 6
	46	3– 4		62	3– 4
	47	1– 2		63	1– 2

15.2 Cables and output modules

15.2.1 Flat system cable 35 SK 90 R*



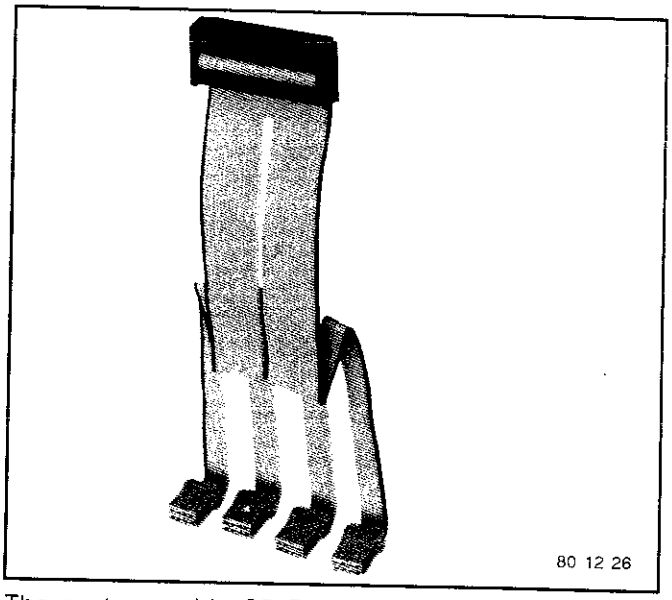
The system cable 35 SK 90 connects the 34-polar plug connectors of the ABB Procontic T300 in-/output unit with the 16-polar plug connectors of 1 or 2 in-/output modules.

Examples:
35 EB 90 07 EM 61
35 AB 90 07 LM 61
35 AB 90 07 LM 61 or 07 AM 62

The following lengths are supplied as standard:

Cable length	Type	Order no.
0.5 m	35 SK 90 R1	GJR5135000R1
1.0 m	35 SK 90 R2	GJR5135000R2
1.5 m	**35 SK 90 R3**	**GJR5135000R3** (preferred)
2.0 m	35 SK 90 R4	GJR5135000R4
2.5 m	35 SK 90 R5	GJR5135000R5

15.2.2 Flat system cable 35 SK 91 R*



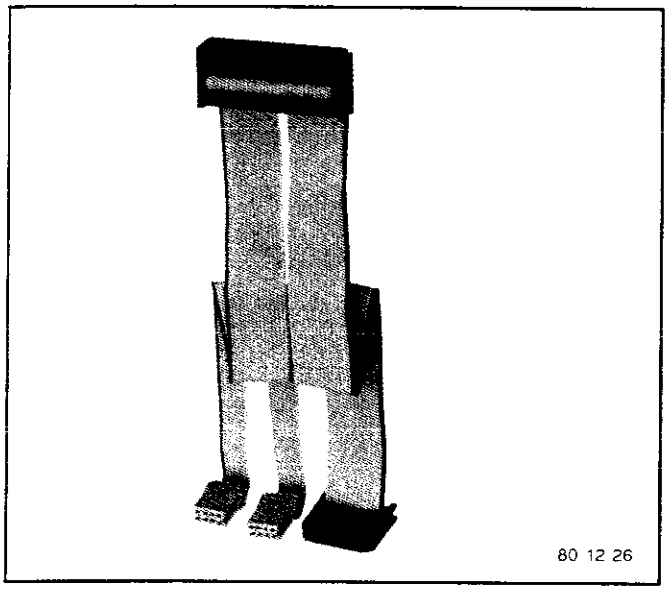
The system cable 35 SK 91 connects the 34-polar plug connectors of the ABB Procontic T300 output units with the 8-polar plug connectors of 1 to 4 output modules.

Examples:
35 AB 90 07 TM 61
35 AB 90 07 TM 61, 07 RM 61 and 07 RM 61

The following lengths are supplied as standard:

Cable length	Type	Order no.
0.5 m	35 SK 91 R1	GJR5135100R1
1.0 m	35 SK 91 R2	GJR5135100R2
1.5 m	**35 SK 91 R3**	**GJR5135100R3** (preferred)
2.0 m	35 SK 91 R4	GJR5135100R4
2.5 m	35 SK 91 R5	GJR5135100R5

15.2.3 Flat system cable 35 SK 92 R*



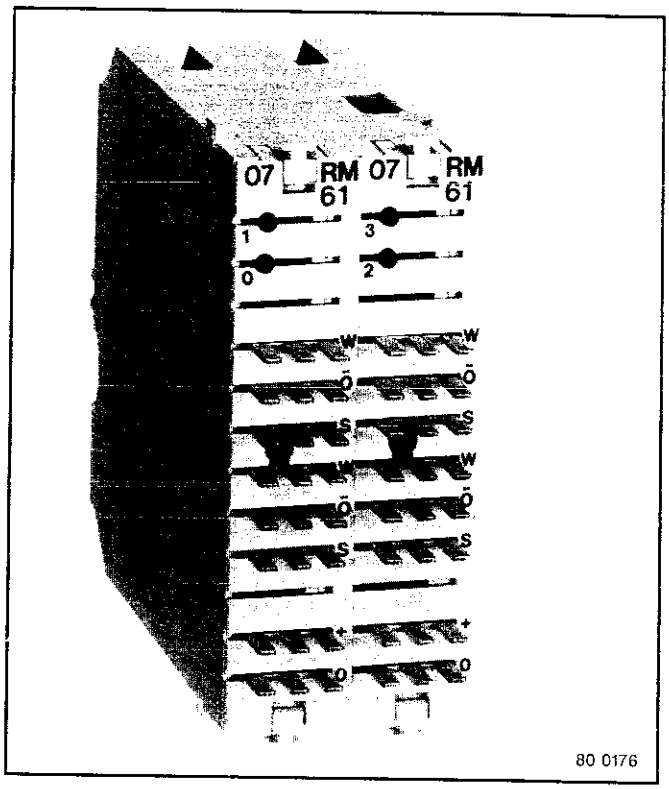
The system cable 35 SK 92 connects the 34-polar plug connectors of the ABB Procontic T300 output units with the 16-polar plug connector of an output module as well as the 80-polar plug connectors of 1 or 2 output modules.

Examples: 35 AB 90 07 LM 61 and 07 TM 61
35 AB 90 07 LM 62, 07 TM 61 or 07 RM 61

The following lengths are supplied as standard:

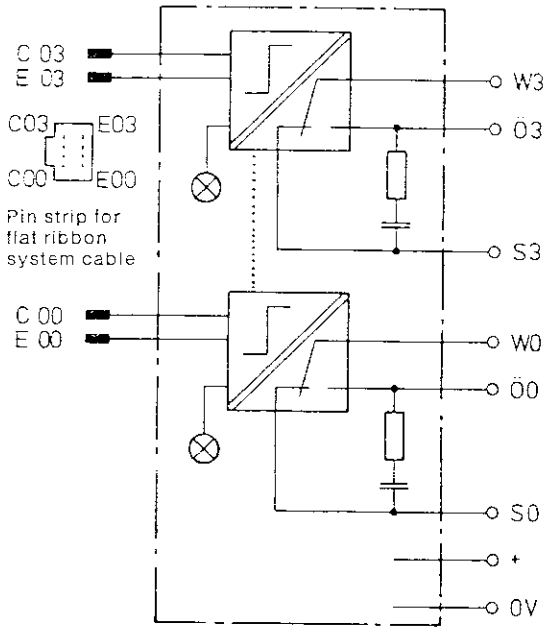
Cable length	Type	Order no.
0.5 m	35 SK 92 R1	GJR5135300R1
1.0 m	35 SK 92 R2	GJR5135300R2
1.5 m	**35 SK 92 R3**	**GJR5135300R3** (preferred)
2.0 m	35 SK 92 R4	GJR5135300R4
2.5 m	35 SK 92 R5	GJR5135300R5

15.2.4 Relay switch stage 07 RM 61
4 ouput channels 220 V AC, 4 A with LED



Technical data

Supply voltage U_s	24 V DC ± 30 %
Insulation group	C/250 according to VDE 0110
Permitted ambient temperature	-20 ...+ 55° C
Switching voltage U_a	max. 250 V
Current switched I_a	max. 4 A
Switching capacity P_a	
with U = 250 V AC	1 kVA per channel
with U = 30 V DC	100 W
with U = 250 V DC	50 W
Limit frequency	approx. 20 Hz
Contact life time 1, unloaded	approx. 1 x 10^7 operating cycles
with 220 V / 4 A	approx. 1 x 10^6 operating cycles
Cut-in delay t_E	approx. 3 ms
Cut-out delay t_A	approx. 7 ms
Bounce time t_P	approx. 4 ms
Current input	35 mA
Signalisation of the output signal	1 red LED each
Weight	0.2 kg
Order number	GJR5211000R1



Block diagram

The relay switch stage 07 RM 61 is controlled by the ABB Procontic T300 and switches consumers with a high power requirement.

The module includes 4 independent output channels with one relay each with change-over contacts. The inputs are isolated galvanically from the outputs. The loadability of the change-over contact amounts to 4 A with 220 V. The switch status of each output channel is displayed by a red light-emitting diode.

ARC combination is switched between the source and working contact for the protection of the contact, above all when switching inducting consumers. This represents a matching resistance for the AC current. It is for this reason, that a greater or smaller voltage can be measured at an open contact depending on the sensitivity of the instrument used.

A demagnetization circuit is also required parallel to the consumer to switch inductive DC loads, e.g., a free-wheeling diode alone or a series connection of a diode and a Zener diode.

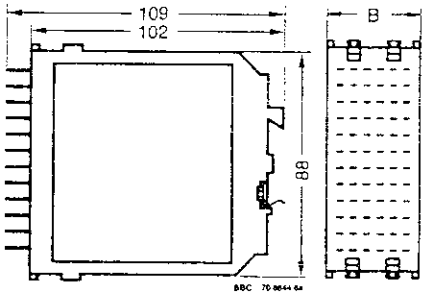
Experience has shown, that the lifetime of AC contacters or solenoid valves in the range of 100 ... 1200 VA and phi = 0.3 ... 0.5 when switching amounts to > 10^6 operating cycles.

The circuitry is located in a plastic casing, which is snapped onto a top-hat-rail of 35 mm in accordance with DIN 46 277, page 3.

The input signals coming from the ABB Procontic T300 are guided from above via an 8-polar plug connector by means of the system cables 35 SK 91 or 35 SK 92.

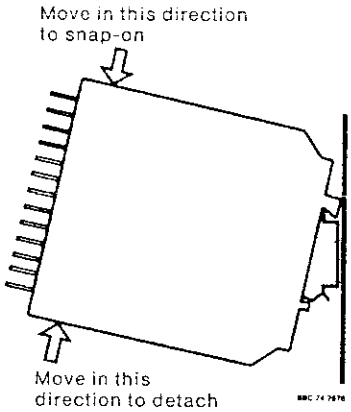
The process signals are output to the front via flat plugs 2.8 x 0.8 mm, which are in three parts and are connected to each other, in accordance with DIN 46 244.

The module requires a 24 V DC ± 30 % supply voltage, which is connected to the flat plugs + and 0, as it comes from a separate power supply unit.



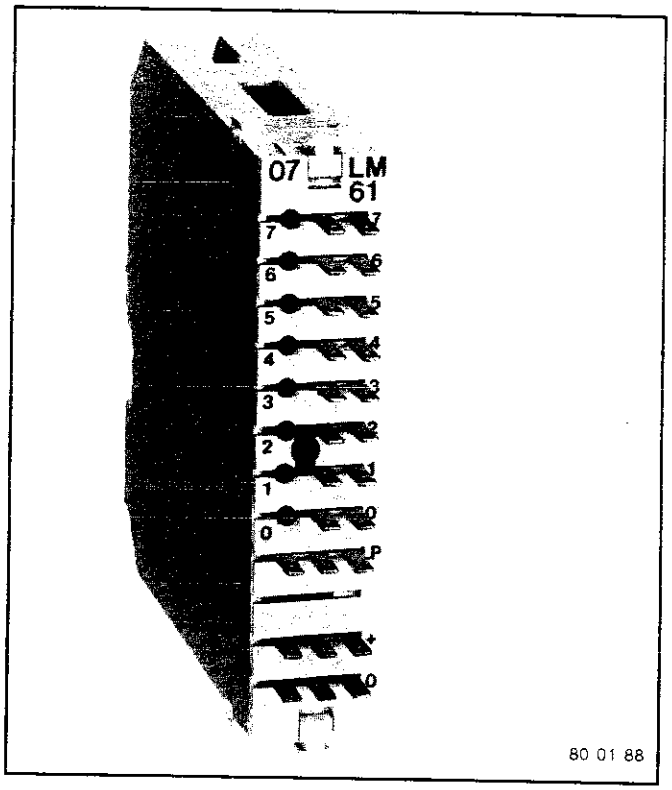
Module type	Meas. B
07 EM 61	20
07 LM 61	20
07 TM 61	40
07 RM 61	40
07 AM 62	40

Mounting measurements



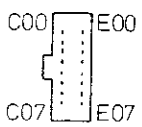
Notes for mounting

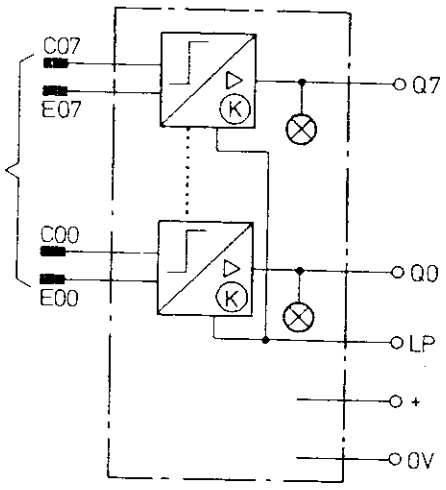
15.2.5 Lamp driver stage 07 LM 61
8 output channels 24 V DC, 210 mA with LED



Technical data

Supply voltage U_S	24 V DC ± 30 %
Insulation group	C/380 according to VDE 0110
Permitted ambient temperature	-20 ... +55° C
Output voltage U_A	≥ (U_S - 3 V)
Output current I_A	210 mA per channel
Sum I_A	850 mA per module
Current input, all outputs 0 signal	typically 30 mA
all outputs 1 signal	typically 100 mA + output currents
Signalisation of the output signal	1 red LED each
Weight	0.1 kg
Order number	GJR5210900R1





Block diagram

The lamp driver stage 07 LM 61 is controlled by the ABB Procontic T300 and switches ohmic, inductive and lamps or loads with a smaller power.

The module includes 8 independent output channels. These outputs are resistant against short-circuits and switch themselves on again automatically after removing a short-circuit and if the control is present. The output loadability per channel amounts to 210 mA with 24 V DC. The switch status of each ouput channel is displayed by a red light-emitting diode.

The circuitry is in a plastic casing, which is snapped onto a top-hatrail of 35 mm in accordance with DIN 46 277, page 3.

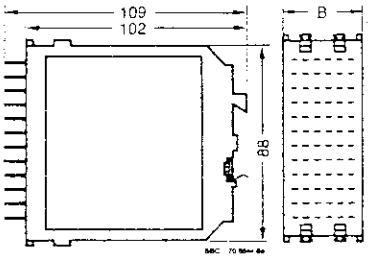
The input signals coming from the ABB Procontic T300 are guided from above via a 16-polar plug connector by means of the system cable 35 SK 90 or 35 SK 92.

The process signals are output to the front via flat plugs 2.8 x 0.8 mm, which are in two parts and connected to each other, according to DIN 46 244.

The module requires a 24 V DC ± 30 % supply voltage, which is connected to the flat plugs + and 0, as it comes from a separate power supply unit.

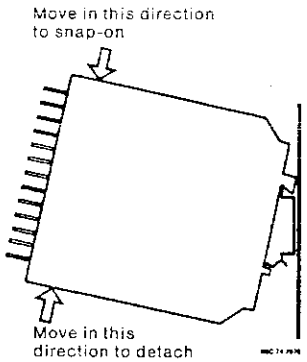
The flat plug connection LP serves to test the lamp. If the input LP is connected with 24 V, the process outputs are switched through independently of the signal input (the 8 red LEDs light up). All the outputs can be loaded with 210 mA for a short time to test the lamps.

The maximum permitted power loss of the module limits the total output current to 850 mA, i.e. the simultaneity factor of the outputs amounts to 0.5.



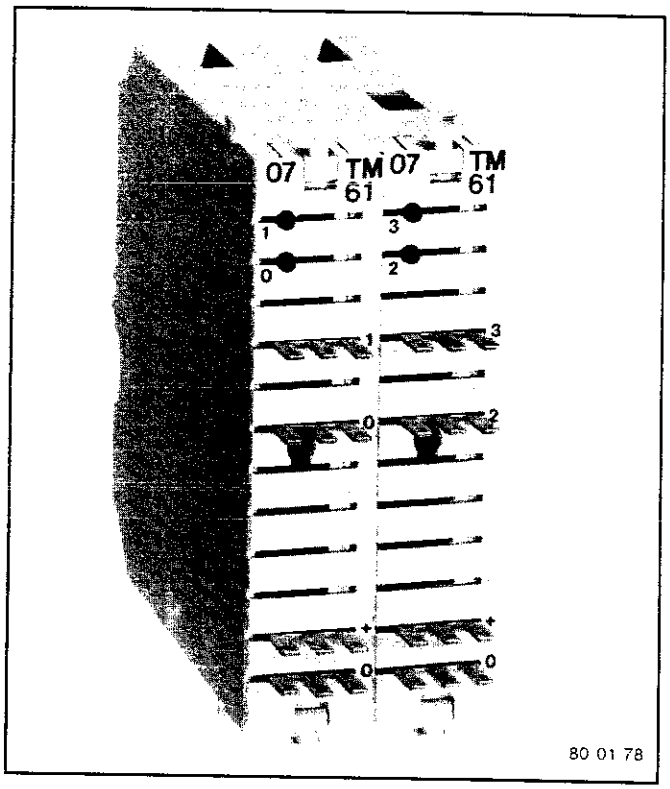
Module type	Meas. B
07 EM 61	20
07 LM 61	20
07 TM 61	40
07 RM 61	40
07 AM 62	40

Mounting measurements



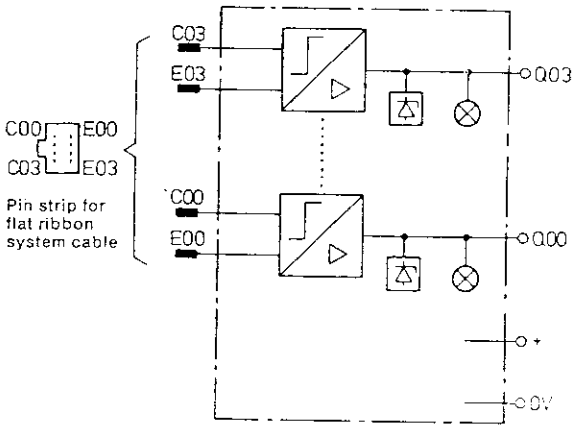
Notes for mounting

15.2.6 Transistor switch stage 07 TM 61 8 output channels 24 V DC, 2 A with LED



Technical data

Supply voltage U_S	24 V DC ± 30 %
Insulation group	C/380 according to VDE 0110
Permitted ambient temperature	-20 ... +55° C
Output voltage U_A	≥ (U_S– 3 V)
Output current I_A	2 A per channel
Sum I_A	4 A per module
(inductive or ohmic)	1.8 A + lamp 2 W
Together with incandescent lamps	1.5 A + lamp 5 W
1.0 A + lamp 10 W	
or only lamp 18 W	
Current input, all outputs 0 signal	typically 9 mA
all outputs 1 signal	typically 65 mA + output currents
Signalisation of the output signal	1 red LED each
Weight	0.2 kg
Order number	GJR5211100R1



Block diagram

The transistor switch stage 07 TM 61 is controlled by the ABB Procontic T300 anad switches ohmic, inductive lamps/loads of a greater power.

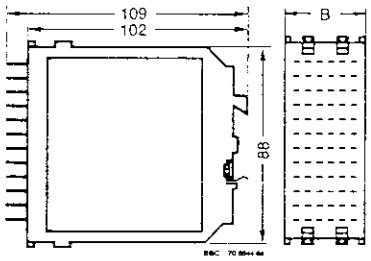
The module includes 4 independent output channels. The output loadability per channel amounts to 2 A with 24 V DC. A fast de-excitation is the case with an inductive load, since the outputs are provided with a series connection of a diode and a Zener diode (47 V). The switch status of each output channel is displayed by a red light-emitting diode.

The circuitry is in a plastic casing, which is snapped onto a top-hatrail of 35 mm according to DIN 46 277, page 3.

The input signals coming from the ABB Procontic T300 are guided from above via an 8-polar plug connector by means of the system cable 35 SK 91 or 35 SK 92. The process signals are output to the front via flat plugs 2.ß x 0.8 mm, which are in three parts and connected to each other, according to DIN 46 244.

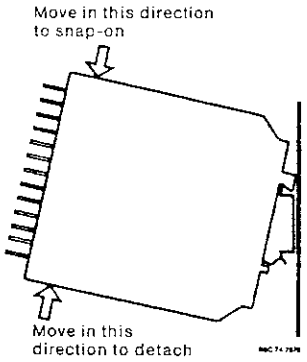
The module requires a 24 V DC ± 30 % supply voltage, which is connected to the flat plugs + and 0, as it comes from a separate power supply unit.

The maximum permitted power loss of the module limits the total output current to 4 A, i.e., the simultaneity factor of the output amounts to 0.5.



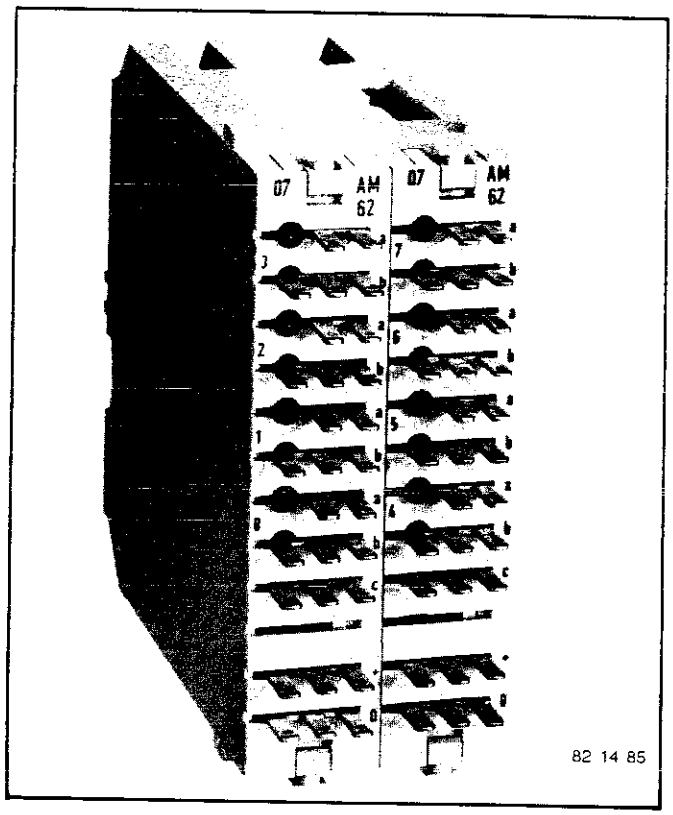
Module type	Meas. B
07 EM 61	20
07 LM 61	20
07 TM 61	40
07 RM 61	40
07 AM 62	40

Mounting measurements



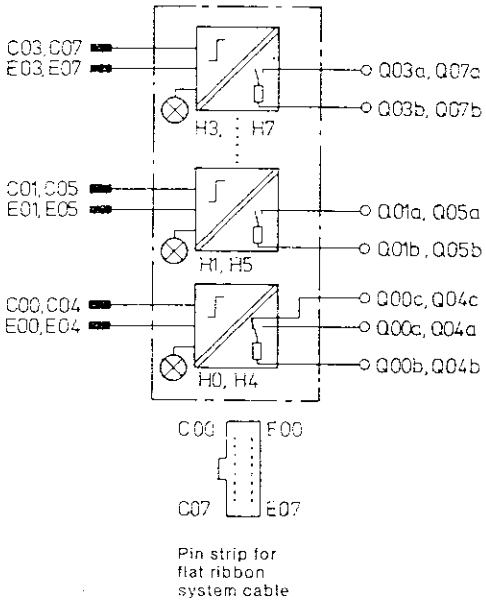
Notes for mounting

15.2.7 Reed relay switch stage 07 AM 62 8 output channels 60 V, 100 mA, with LED



Technical data

Supply voltage U_S		24 V ± 30 %	
Permitted ambient temperature		–20 ... +55° C	
Switching voltage U_A	Make contact	max. 60 V	each channel
	Change-over contact	max. 28 V	
Permanent current switched I_A	Make contact	max. 100 mA	
	Change-over contact	max. 100 mA	
Peak current switched	Make contact	500 mA	
	Change-over contact	250 mA	
Switching capacity P_A	Make contact	max. 3 W	
	Change-over contact	max. 1.5 W	
Current input		typically 15 mA	
Contact life time		> 10 operating cycles	
Cut-in delay t_E		approx. 2 ms	
Cut-out delay t_E		approx. 2 ms	
Bounce time t_P		< 1 ms	
Signalisation of the output signal		1 red LED each	
Weight		0.2 kg	
Order number		GJR5214500R2	



Block diagram

The reed relay switch stage 07 AM 62 is controlled by the ABB Procontic T300 and switches light current analogue signals.

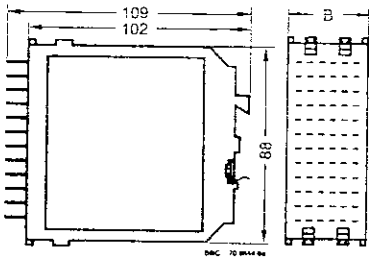
The modules includes 8 independent output channels, 6 channels with 1 make contact each and 2 channels with 1 change-over contact each. The inputs are isolated galvanically from the output. A component (resistor, wire jumper, decoupling diode, etc.) can be put on solder tags in the row with the make contact. The switch stage is equipped as a standard with 10 Ohm/0.25 W to stop the contacters from sticking.

The switch status of each output channel is displayed by a red light-emitting diode. The connection is located in a plastic casing, which is snapped onto a top-hat rail of 35 mm in accordance with DIN 46 277, page 3.

The input signals are guided from above via a 16-polar plug connector by means of the system cable 35 SK 90 or 35 SK 92.

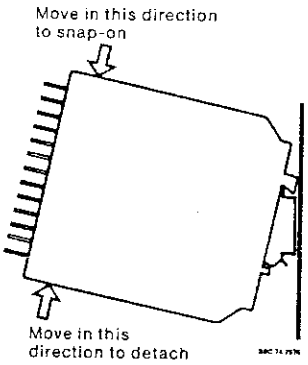
The process signals are output to the front via flat plugs 2.8 x 0.8 mm, which are in three parts and connected to each other, according to DIN 46 244.

The module requires a 24 V DC ± 30 % supply voltage, which is connected to the flat plugs + and 0, as it comes from a separate power supply unit.



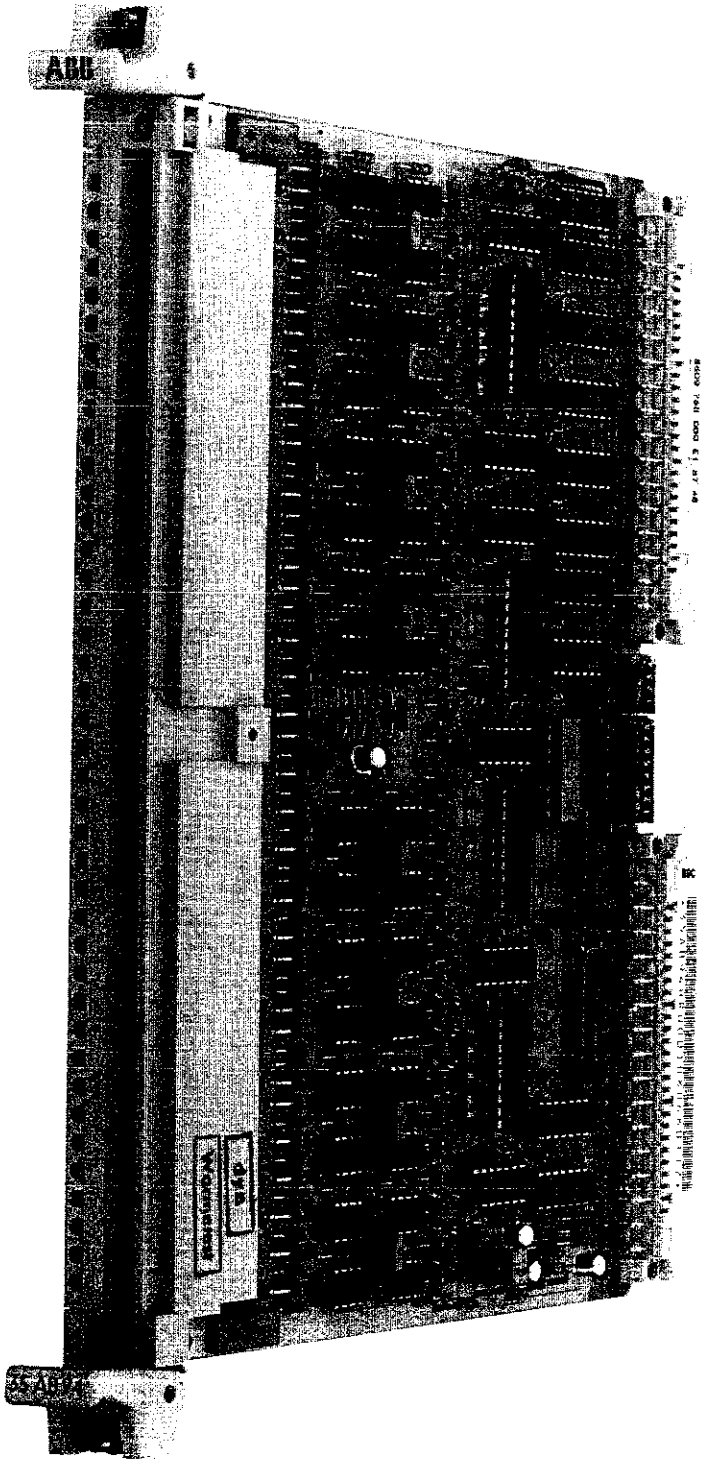
Module type	Meas. B
07 EM 61	20
07 LM 61	20
07 TM 61	40
07 RM 61	40
07 AM 62	40

Mounting measurements



Notes for mounting

15.3 Binary output unit 35 AB 94 R1



90 01 70

15.3.1 Technical data

Supply voltage U_{B1}	+5 V ±5 %
Current input I_{B1} with U_{B1}	typically < 0.4 A
Supply voltage U_{B2}	+ 15 V +/– 5%
Current input I_{B2} with U_{B2}	typically < 15 mA
Power loss	8.5 W
Channels per unit	32
Current supply (on the front):	
Supply voltage U_{P1}	+ 24 V ± 30%
Permitted excess of the supply voltage U_{P1}	
without a time limit	+ 35 V
for 10 ms	+ 45 V
Current input	< 3.7 A
Output voltage:	
1 signal	U_{P1} – 3 V referring to 0 V externally
0 signal, output unloaded	< 0.4 V
Output current:	
Nominal value	100 mA
Maximum value	125 mA
Inductive load	100 %
Demagnetization	via free–wheeling diode
Switch frequency	any
Short–circuit resistance	present, automatic switch–on again after removing the short–circuit
Simultaneity factor	100 %
Electrical isolation	none, common reference potential 0 V
Signalisation	1 yellow LED per channel
Electro magnetic compatibility	in accordance with IEC 801/4
Thermal protection	The output drivers are switched off with too high a thermal load. The time to switch them on again is max. 16 s.
Ambient temperature	0 °C ... +55 °C
Storage temperature	–25 °C ... +75 °C
Humidity rating	F
Mechanical stress when installed	VDE 0160
Dimensions	1 pitch
Weight	0.5 kg
Order number	GJR5142800 R1

Accessories:

Front plug 35 SK 90 R1	GJR5144900R1
Label set 35 SB 90 R5	GJR5144600R5

15.3.2 Description

The binary output unit 35 AB 94 is a passive subscriber on the MPST bus. 32 channels with a loadability of 100 mA are converted by the MPST bus to the front plug terminals. The unit supplies 24 V signals and is resistant against short-circuits.

The 32 output channels are divided into 4 groups of 8 channels each.

The output signals can only be "written". The writing can take place in words (decoded word address W0 = 1) or in bytes (decoded word address W0 = 0).

Prerequisites for the writing operation:
a) Control signal '$\overline{W}$' = 0
b) Control signal '$\overline{I/O}$' = 0
c) A13, A14 and A15 = 1

The data are copied into the output register with the decoded addresses A00, A01 and the status change of the signal 'BOV' from 1 to 0, after the address coding has taken place..

A signal ADET (Address detect signal) is output to the bus with a successful address comparison (unit addressed). This signal can be switched off (removing the resistor assembly for R9).

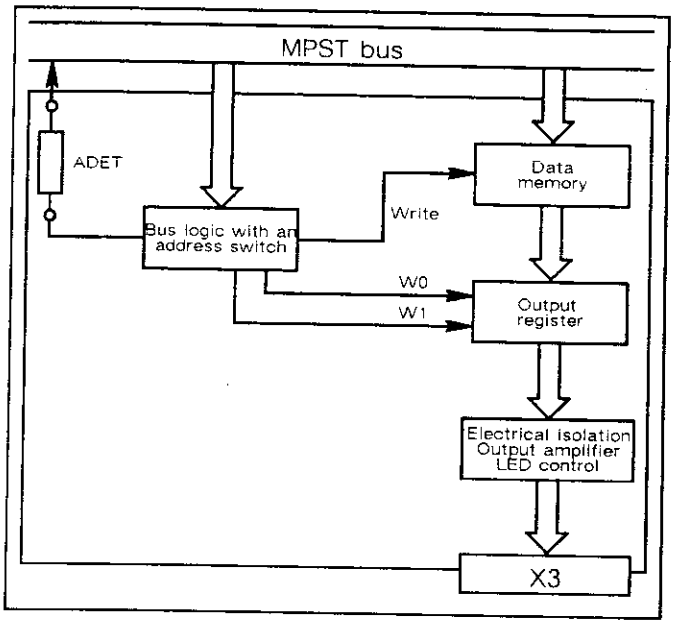


Fig.15.3-1 Block diagram

15.3.3 Unit addresses

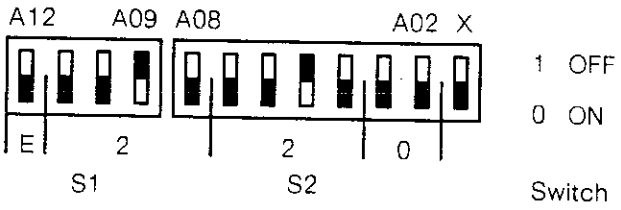
15.3.3.1 Address setting

The addresses 'A02' to 'A12' of the card are set with the switches S1, S2 (4 bit and 8 bit DIL switches). The individual switch elements can be accessed by opening the transparent cover. See fig. 15.3-2 for the position of the switches.

Note: The lowest switch element of switch S2 is not connected.

Example for setting the unit address:

Selected unit address: E220



(A15 ... A13: always equal 1 for in-/output units
A01 ... A00: selection of the channel groups)

15.3.3.2 Address division

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
T300 code of the upper, passive address area (perm. wired up)			S1				S2								
			The unit address for switches S1 and S2 can be adjusted. Setting ON = 0												

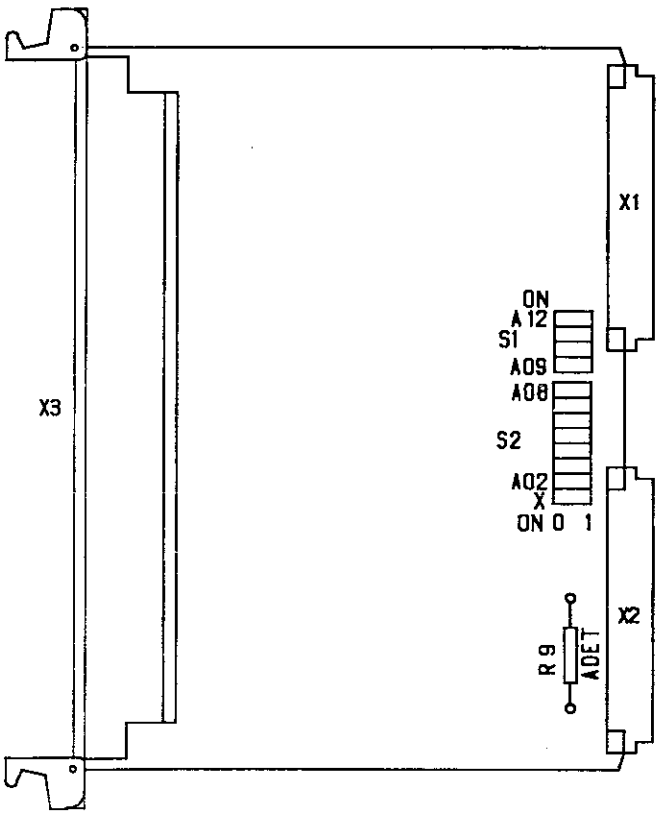
A01	A00	W0	Data	Output channel
0	0	0	D07 ... D00	0.07 ... 0.00
0	1	0	D15 ... D08	0.15 ... 0.08
1	0	0	D07 ... D00	1.07 ... 1.00
1	1	0	D15 ... D08	1.15 ... 1.08
0	0	1	D15 ... D00	0.15 ... 0.00
1	0	1	D15 ... D00	1.15 ... 1.00

15.3.3.3 Assembly positions

The assembly positions ADET (address detect signal, see Fig. 15.3-2) can be equipped with the resistor R9 (100 Ohms), if necessary.

15.3.4 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.



X = not connected

Fig. 15.3-2 Component side (top view)

Displays:

32 LEDs Yellow colour to display the output signals

Plug connectors:

X1, X2	32-polar MPST interface according to DIN 46 612, part 2, design C
X3	40-polar periphery interface (process data, +24 V, 0 V, free positions)

15.3.5 Plug assignment

15.3.5.1 MPST bus interface, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{\text{PFD}}$	Power fail detect
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	ADET	Adress Detect Signal	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	–	–
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

15.3.5.2 Front plug X3

Pin	Signal name	Meaning
X3.01	U P1	Process voltage
X3.02	Output signal	Channel 0.00
X3.03	Output signal	Channel 0.01
X3.04	Output signal	Channel 0.02
X3.05	Output signal	Channel 0.03
X3.06	Output signal	Channel 0.04
X3.07	Output signal	Channel 0.05
X3.08	Output signal	Channel 0.06
X3.09	Output signal	Channel 0.07
X3.10	Z P1	0 V process voltage
X3.11	–	–
X3.12	Output signal	Channel 0.08
X3.13	Output signal	Channel 0.09
X3.14	Output signal	Channel 0.10
X3.15	Output signal	Channel 0.11
X3.16	Output signal	Channel 0.12
X3.17	Output signal	Channel 0.13
X3.18	Output signal	Channel 0.14
X3.19	Output signal	Channel 0.15
X3.20	–	–
X3.21	–	Process voltage
X3.22	Output signal	Channel 1.00
X3.23	Output signal	Channel 1.01
X3.24	Output signal	Channel 1.02
X3.25	Output signal	Channel 1.03
X3.26	Output signal	Channel 1.04
X3.27	Output signal	Channel 1.05
X3.28	Output signal	Channel 1.06
X3.29	Output signal	Channel 1.07
X3.30	–	0 V process voltage
X3.31	U P1	
X3.32	Output signal	Channel 1.08
X3.33	Output signal	Channel 1.09
X3.34	Output signal	Channel 1.10
X3.35	Output signal	Channel 1.11
X3.36	Output signal	Channel 1.12
X3.37	Output signal	Channel 1.13
X3.38	Output signal	Channel 1.14
X3.39	Output signal	Channel 1.15
X3.40	Z P1	0 V process voltage

Important:
A suitable equipotential bonding is to be created between the 0 V voltage of the ABB Procontic T300 system and the external 0 V voltage! There may **not** be a difference in the voltage.

The external 0 V connections must all be connected. They do **not** have a connection on the unit with the 0 V voltage of the ABB Procontic T300 system.

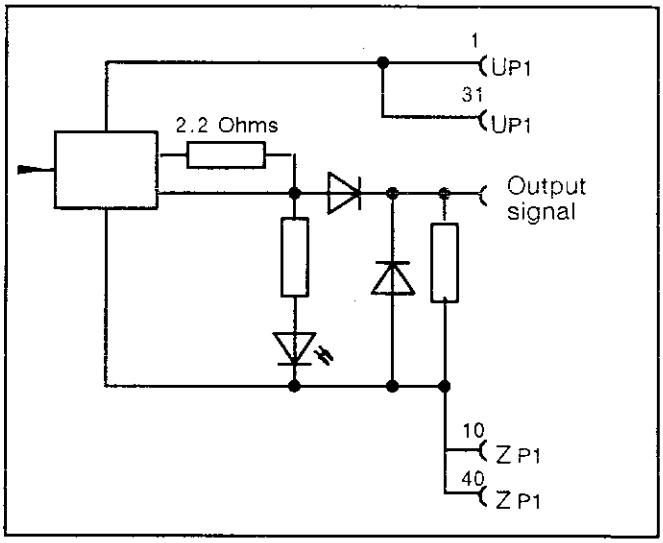
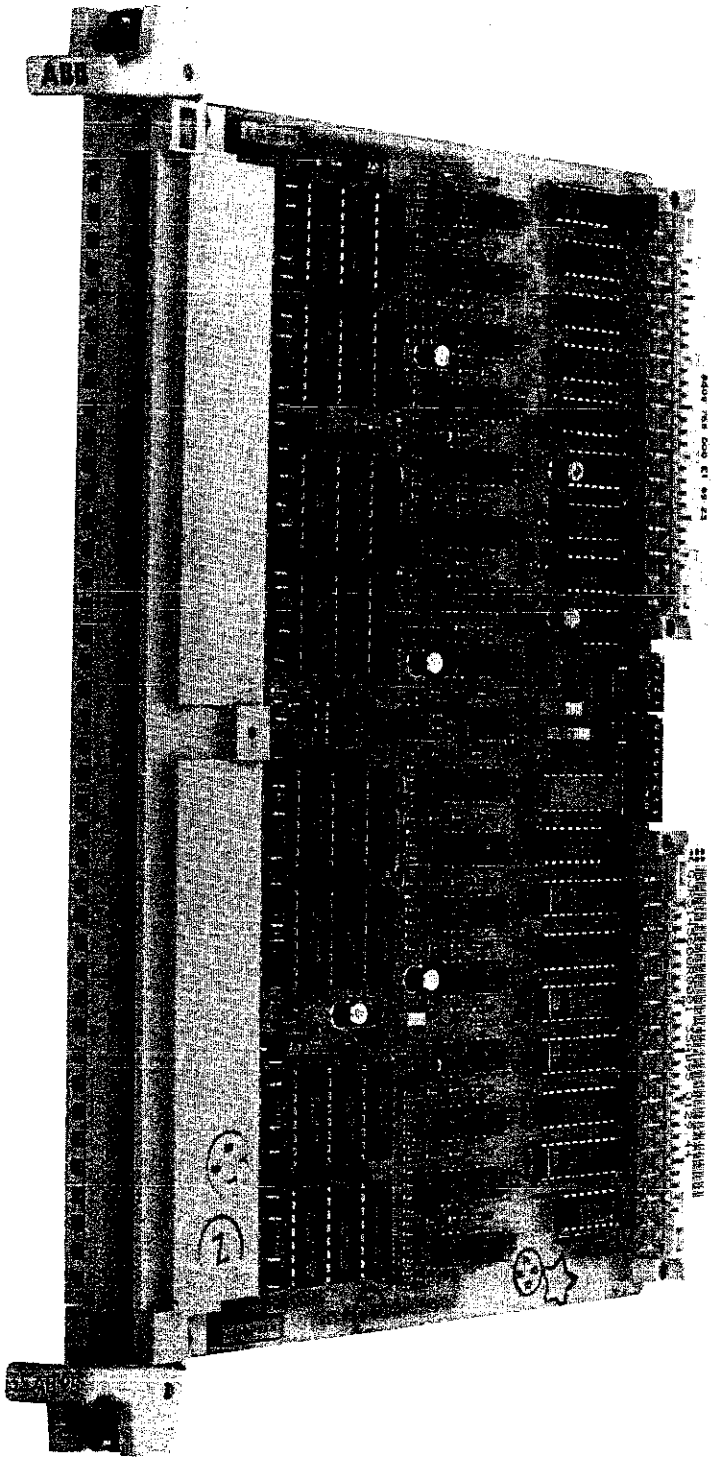


Fig. 15.3-3: Output connection

15.4 Binary output unit 35 AB 95 R1



90 01 72

15.4.1 Technical data

Supply voltage U_{B1}	+5 V ± 5 %
Current input I_{B1} with U_{B1}	< 0.4 A
Power loss	16 W (with 8 A residual current)
Fan operation	yes
Channels per unit	32
Short-circuit common signal output K	Signal output K leads to a 1 signal, if there is an over-current or a short-circuit (red LED) for one or several outputs. The signal output can be switched parallel.
Release input F	1 signal at the release input F (green LED) releases the output channels, 0 signal switches them off.
Input voltage	
Nominal value	+ 24 V
for release	+ 13 V ... + 33 V
for holding	- 33 V ... + 5 V
Input current (with release)	typically 5 mA
Line length (unscreened)	max. 200 m
Acknowledgement input Q	A 1 signal causes the output channel to be switched on again after removing the short-circuit, if the device is in the operating mode "external acknowledgement" (green LED).
Input voltage (ext.)	
Nominal value	+ 24 V
for acknowledgement	+ 13 ... + 33 V
Input current (with acknowledgement)	typically 7 mA
Line length (unscreened)	max. 200 m
Current supply (on the front):	
Supply voltage U_{P1}	+24 ± 30 %
Permitted excess of the supply current for 10 ms	+45 V
Output current	
1 signal with Imax	U_{P1} - 3 V
0 signal, output unloaded	< 0.4 V
Output current	
Nominal value	500 mA with U_{P1} = 24 V
Maximum value	650 mA with U_{P1} = 24 V + 30 %
Residual current with 0 signal	< 500 µA
Inductive load	100%
Demagnetization	via a free-wheeling diode
Line length (unscreened)	max. 400 m
Switch frequency	max. 11 Hz with max. 5 W
Short-circuit resistance	yes, automatic switch-on again after removing the short-circuit or acknowledgement via a binary input (X3.30)
Residual output current for unit	8 A
Electrical isolation	yes, via optocouplers in groups of 32
Parallel connection of output channels	max. 16 channels (total current 8 A)
Signalization of the power outputs	one yellow LED per channel
Signalization of the short-circuit signal	one red LED
Signalization of the release input	one green LED
Signalization of the acknowledgement input	one green LED
Electro-magnetic compatibility	in accordance with IEC 801/4
Thermal protection	The output drivers are switched off with too high a thermal load. Switch-on again time is max. 5 s.

Ambient temperature	0 °C ... + 55 °C
Storage temperature	– 25 °C... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 0160
Dimensions	1 pitch
Weight	0.3 kg
Order number	GJR5145600R1

Accessories:

Front plug 35 SK 90 R1	GJR5144900R1
Label set 35 SB 90 R5	GJR5144600R5

15.4.2 Description

The binary output unit 35 AB 95 is a passive subscriber on the MPST bus. 32 channels with a loadability of 500 mA are converted by the MPST bus to the front plug terminals. The 32 output channels are divided into 4 groups of 8 channels each. A maximum of 16 output channels can be switched parallel. The unit supplies 24 V signals and is resistant to short-circuits.The output signals can only be "written" (in words and in bytes).

A short-circuit signal is output to the MPST bus when reading the unit address and if a short-circuit occurs.

Diagnosis signal ADET

It can be ascertained with the signal ADET (address detect signal) and a corresponding diagnosis unit, whether an addressed unit is present, not present or present many times.

A signal ADET (Address detect signal) is output to the bus with a successful address comparison (unit addressed). This signal can be switched off (removing the resistor assembly for R197).

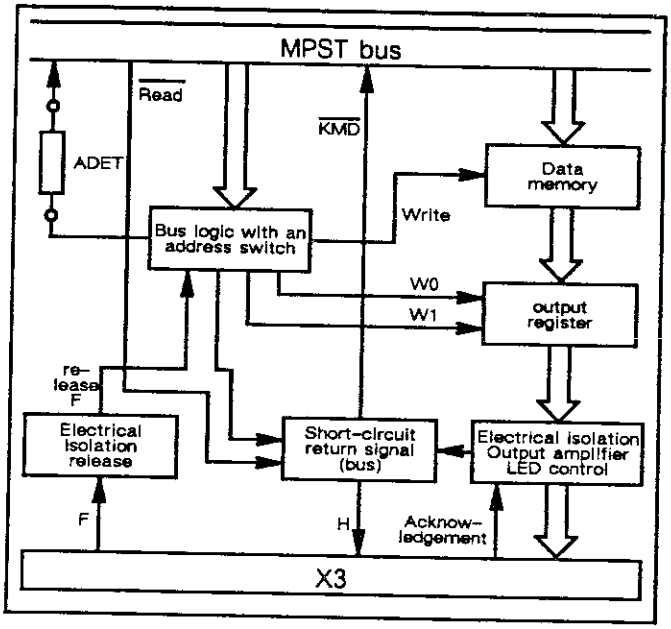


Fig.15.4-1 Block diagram

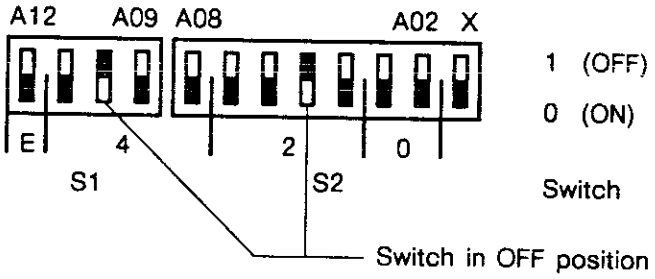
15.4.3 Unit addresses

15.4.3.1 Address setting

The addresses 'A02' to 'A12' of the card are set with the switches S1, S2 (4 bit and 8 bit DIL switches). The individual switch elements can be accessed by opening the transparent cover. See Fig. 15.4-2 for the position of the switches.

Example for setting the unit address:

Selected unit address: E220



Note:
The lowest switch element X of switch S2 is not connected.

(A15 ... A13: always equal 1 for in-/output units
A01 ... A00: selection of the channel group)

15.4.3.2 Address division

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
T300 code of the upper, passive address area (perm. wired up)			S1				S2								
			The unit address for switches S1 and S2 can be adjusted. Setting ON = 0												

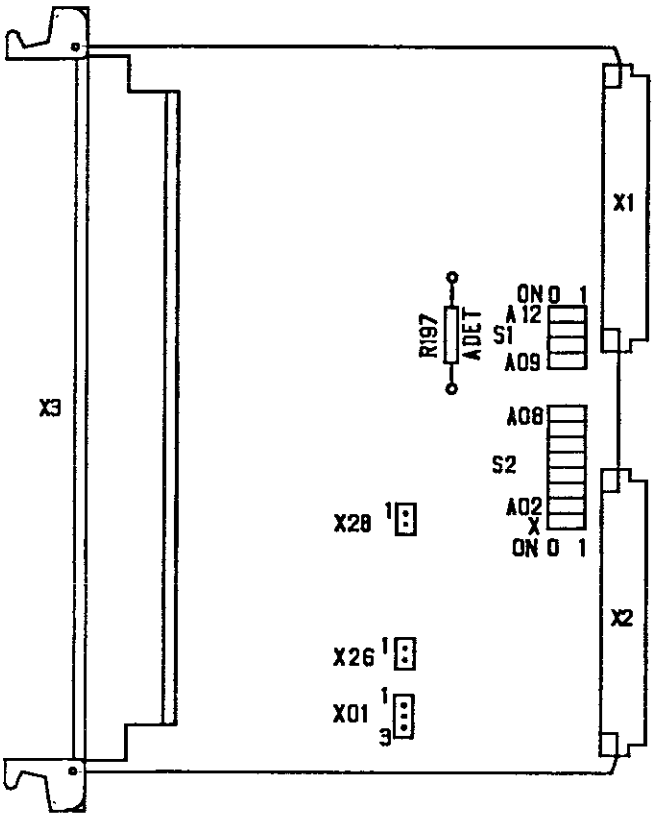
A01	A00	W0	Data	Output channel
0	0	0	D07 ... D00	0.07 ... 0.00
0	1	0	D15 ... D08	0.15 ... 0.08
1	0	0	D07 ... D00	1.07 ... 1.00
1	1	0	D15 ... D08	1.15 ... 1.08
0	0	1	D15 ... D00	0.15 ... 0.00
1	0	1	D15 ... D00	1.15 ... 1.00

15.4.3.3 Assembly positions

The assembly positions ADET (address detect signal, see Fig. 15.4-2 and Fig. 15.4-3) is equipped with the resistor R197 (100 Ohms) by the factory.

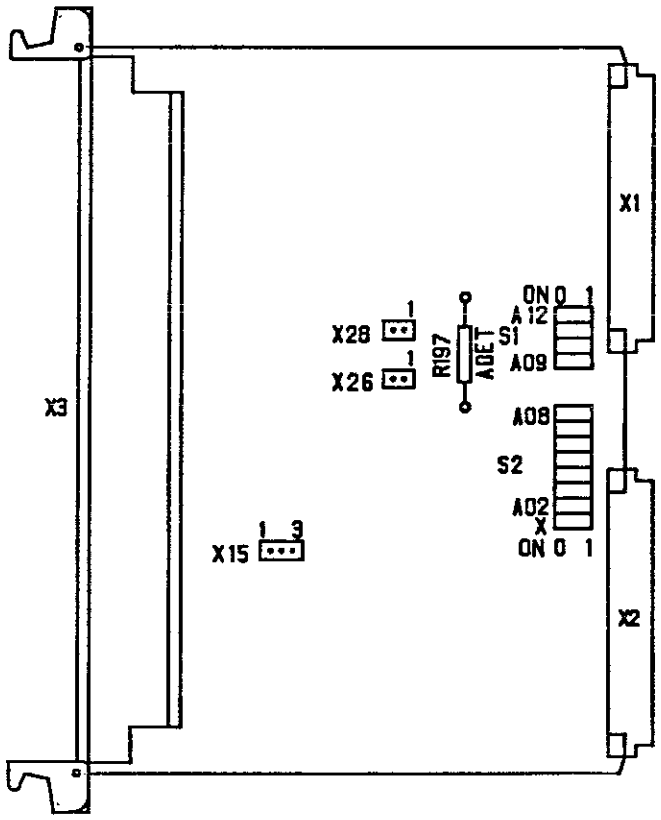
15.4.4 Mechanical structure

Double-size plug-in card in the Europe format 6 U, 1 pitch, 160 mm deep.



X = not connected

Fig. 15.4-2 Component side (top view) with the printed board GJR5145611P1 (solder side)



X = not connected

Fig. 15.4-3 Component side (top view) with the printed board GJR5145611P3 (solder side)

Displays:

32 LEDs	Yellow colour to display the output signals
1 LED	Red colour to display the short-circuit signal
2 LEDs	green colour to display the release and acknowledgement

Plug connectors:

X1, X2	32-polar MPST bus interface according to DIN 41 612, part 12, design C
X3	40-polar periphery interface (process data, +24 V, 0 V, free positions)

Plug connector X01 for printed circuit GJR5145611P1 (Fig. 15.4-2) and plug connector X15 for printed circuit GJR5145611P3 (Fig. 15.4-3) have the same function.

X01 or X15	Switching on the output channel again after removing the short-circuit:
	Jumpers 1-2 via acknowledgement input X3.30
	Jumpers 2-3 automatic acknowledgement
X26, X28	Short-circuit signal to the MPST bus:
X26	Jumpers 1-2, D15= 0 signal with short-circuit
or X28	Jumpers 1-2, D02= 0 signal with short-circuit

Attention: Only X26 and X28 may be inserted with the printed board GJR5145611P1 (Fig.15.4-2). X26 and X26 are not allowed to be inserted at the same time.

Factory settings:

Automatic acknowledgement (short-circuit): X01/2-3
or X15/2-3
Data bit D15 = 0 signal with short-circuit: X26/1-2
Data bit D02 = 0 signal with short-circuit : X28/1-2

15.4.5 Plug assignment

15.4.5.1 Front plug X3

Pin	Signal name	Meaning
X3.01	U P1	Process voltage
X3.02	Output signal	Channel 0.00
X3.03	Output signal	Channel 0.01
X3.04	Output signal	Channel 0.02
X3.05	Output signal	Channel 0.03
X3.06	Output signal	Channel 0.04
X3.07	Output signal	Channel 0.05
X3.08	Output signal	Channel 0.06
X3.09	Output signal	Channel 0.07
X3.10	Z P1	0 V process voltage
X3.11	Output signal	Short-circuit common signal K
X3.12	Output signal	Channel 0.08
X3.13	Output signal	Channel 0.09
X3.14	Output signal	Channel 0.10
X3.15	Output signal	Channel 0.11
X3.16	Output signal	Channel 0.12
X3.17	Output signal	Channel 0.13
X3.18	Output signal	Channel 0.14
X3.19	Output signal	Channel 0.15
X3.20	Z P1	0 V process voltage
X3.21	Input signal	Release input F
X3.22	Output signal	Channel 1.00
X3.23	Output signal	Channel 1.01
X3.24	Output signal	Channel 1.02
X3.25	Output signal	Channel 1.03
X3.26	Output signal	Channel 1.04
X3.27	Output signal	Channel 1.05
X3.28	Output signal	Channel 1.06
X3.29	Output signal	Channel 1.07
X3.30	Input signal	Acknowledgement Q
X3.31	U P1	process voltage
X3.32	Output signal	Channel 1.08
X3.33	Output signal	Channel 1.09
X3.34	Output signal	Channel 1.10
X3.35	Output signal	Channel 1.11
X3.36	Output signal	Channel 1.12
X3.37	Output signal	Channel 1.13
X3.38	Output signal	Channel 1.14
X3.39	Output signal	Channel 1.15
X3.40	Z P1	0 V process voltage

The ZP1 connections (0 V process voltage) must all be connected. They do not have a connection on the unit with the 0 V voltage of the ABB Procontic T300 system.

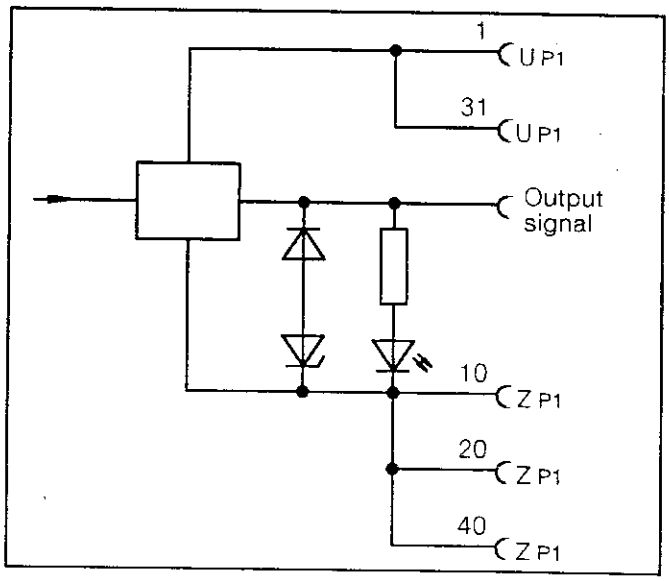


Fig.15.4-4 Output connection

15.4.5.2 MPST bus interface, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	UB1	+5 V voltage	X1. 2c	UB1	+5 V voltage
X1. 4a	UB1	+5 V voltage	X1. 4c	UB1	+5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{\text{PFD}}$	Power Fail Detect
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Bedeutung
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	$\overline{\text{D14}}$	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	ADET	Address Detect Signal	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage.	X2.32c	0 V	0 V voltage

15.4.6 Short-circuit and overload treatment

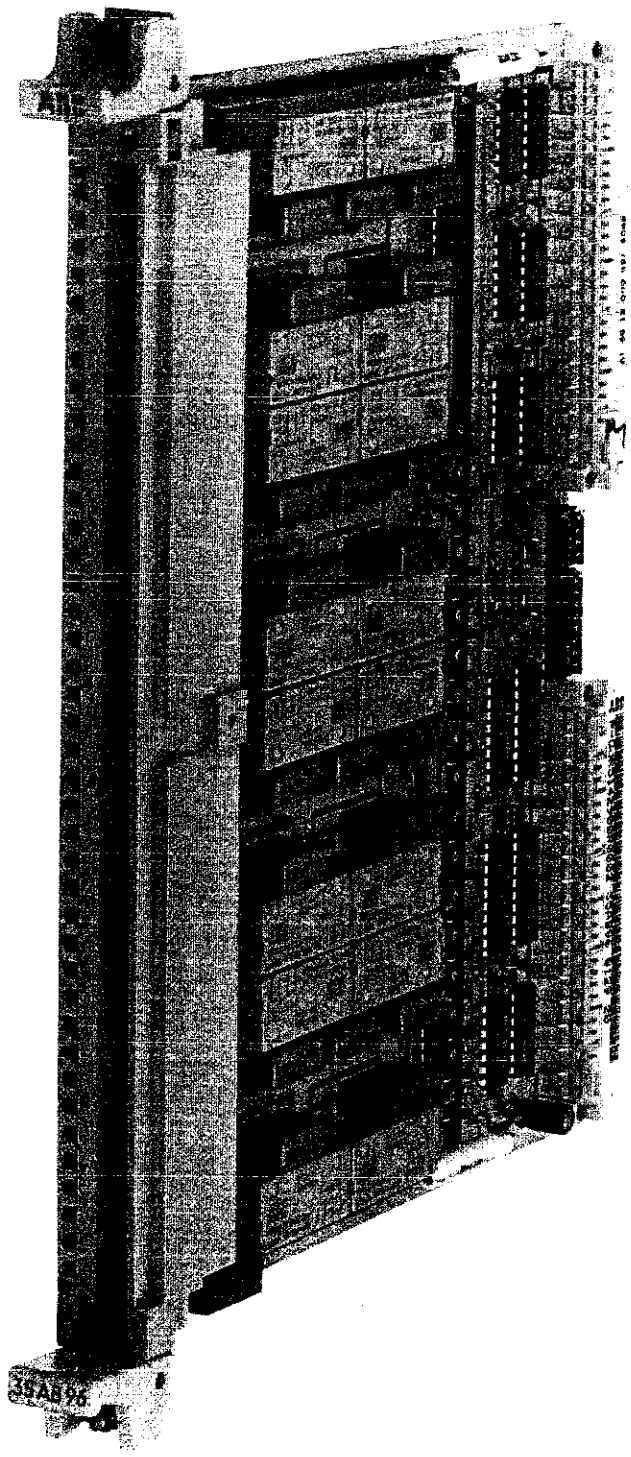
The following messages appear in the case of a short-circuit at the output or an overload:

- Signal K: 1 signal and
- Diagnoses/short-circuit signal to the MPST bus
  Under the set unit address the D15 data bit can be evaluated with the X26/ 1 - 2 jumper insert, or the D2 data bit can be evaluated with the X28/ 1 - 2 jumper inserted.
  D02 or D15 = 0 overload or short-circuit at one or several channals
  D02 or D15 = 1 no overload or short-circuit
  Note: With the automatic acknowledgement of the short-circuit, the short-circuit signal is not stored, i.e. D02 or D15 became '1' again.
  With the printed board GJR5145611P1 the short-circuit signal can be evaluated either with D15 or D02.

The corresponding channel can

- be switched on automatically (X01/2-3 or X15/2-3 bridged) or
- be switched on again after the acknowledgement via the acknowledgement input X3.30 (X01/1-2 or X15/1-2 bridged) with 1 signal after removing the short-circuit.

15.5 Binary output unit 35 AB 96 R1



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15.5.1 Technical data

Supply voltage UB1	+ 5 V ± 5 %
Current input IB1 with UB1	< 1 A
Power loss	5 W
Fan operation	no
Channels per unit	16
Switching voltage	approx. 12 V ≃ ... 250 V ≃
Voltage reduction, clearance between open contacts	< 0.5 V (conductive clearance between open contacts)
Frequency with AC	50 Hz or 60 Hz
Supply of the switching voltage	via front plugs
Nominal value of the current switched	2 A or 1 A (AC11)
Maximum value	1.1 A x nominal value
Load current (total)	16 A
Leakage current (output unloaded)	< 10 mA (blocked clearance between open contacts)
Lamp load (nominal current)	500 mA with AC
Switching capacity with DC	max. 50 W (demagnetization with an inductive load is also required externally)
Switch frequency with lamp load	0 ... 8 Hz ± 30 %
Operating frequency inductive load	max. 2 Hz with a full load
Demagnetizing an inductive load	RC element and/or a varistor (only effective with AC)
Electrical isolation	with relay, 4-polar make contacts, 3-polar changeover contacts
Short-circuit resistance	no
Signalization	yellow
Electro magnetic compatibility	IEC801/4
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	in accordance with VDE 0160
Dimension	1 pitch
Weight	0.5 kg
Order number	GJR5142900R1

Accessories:

Front plug 35 ST 90 R1	GJR5144900R1
Label set 35 SB 90 R7	GJR5144600R7

15.5.2 Description

The relay output unit 35 AB 96 is a passive user on the MPST bus. The unit converts 16 channels via a relay (12 make contacts and 4 changeover contacts) with a suitable loadability of the current switched of 2 A or 1 A (AC11) with a maximum switching capacity of 50 W from the MPST bus to the output terminals as ABB Procontic T300 outputs. The unit switches voltages of 12 V ... 250 V~.

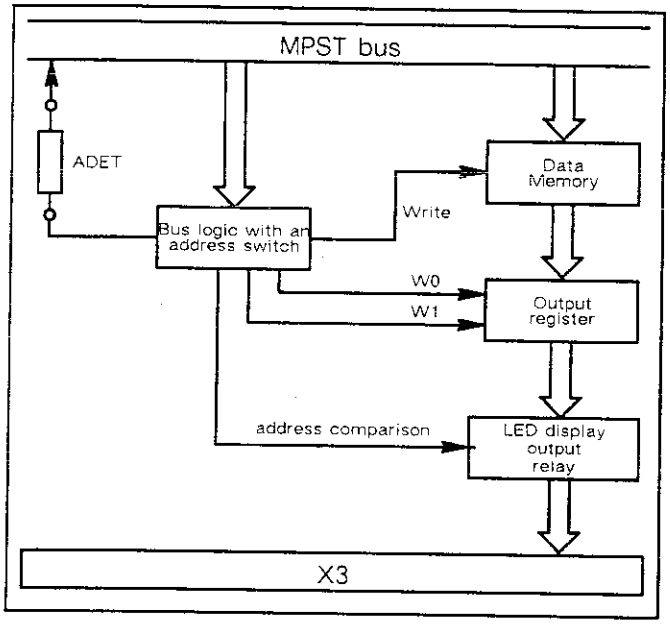


Fig.15.5-1 Block diagram

Diagnosis signal ADET
It can be ascertained with the signal ADET (Address detect signal) and a corresponding diagnosis unit whether an addressed unit is present, not present or present many times. The signal ADET is output to the bus with a successful address comparison (unit addressed). This signal can be switched off. (Remove the resistor assembly R37.)

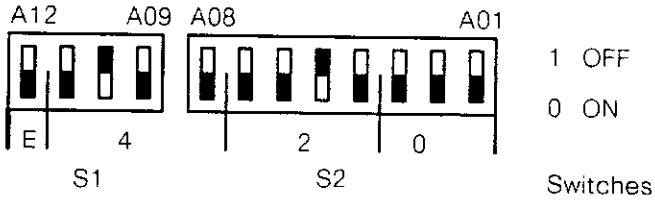
15.5.3. Unit addresses

15.5.3.1 Address setting

The addresses "A1" to "A12" of the card are set with the switches S1, S2 (4 bit and 8 bit DIL switches). The separate switch elements can be accessed by opening the transparent cover. See Fig. 15.5-2 for the position of the switches.

Example for setting the unit address:

Selected unit address: E420



A15 ... A13: always equal 1 for in-/output units
A00: selection of the channel group

15.5.3.2 Address division

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
T300 code of the upper, passive address area (perm. wired up)			S1				S2								
			The unit address for switches S1 and S2 can be adjusted. Setting ON = 0												

A00	W0	Data	Output channel
1	0	D07 ... D00	0.07 ... 0.00
0	0	D15 ... D08	0.15 ... 0.08
0	1	D15 ... D00	0.15 ... 0.00

15.5.3.3 Assembly positions

The assembly position ADET (Address detect signal), see Fig. 15.5-2, is equipped with the resistor R37 by the factory.

15.5.4. Mechanical structure

Unit in the double-sized Eurocard format 160 x 233.4 mm, 1 pitch.

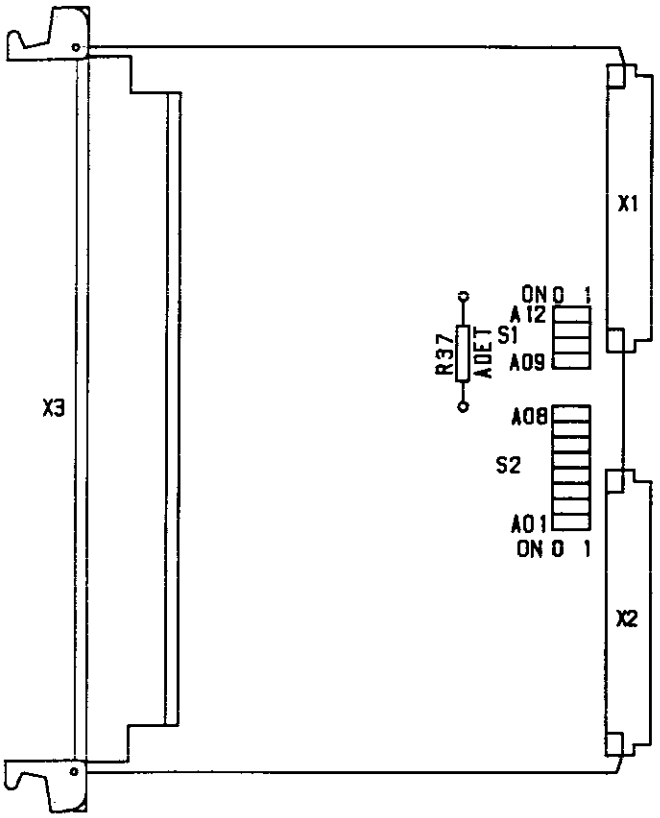


Fig.15.5-2 Component side (top view)

Displays:

16 LEDs, yellow colour, to display "relay applied".

Plug connectors:

X1, X2	32-polar MPST bus interface according to DIN 41 612, part 2, design C
X3	40-polar periphery interface (process data, +24 V, 0 V, free positions)

15.5.5 Plug assignment

15.5.5.1 MPST bus interface, plugs X1,X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U B1	5 V voltage	X1. 2c	U B1	5 V voltage
X1. 4a	U B1	5 V voltage	X1. 4c	U B1	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{\text{PFD}}$	Power Fail Detect
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	ADET	Address Detect signal	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	–	–
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

15.5.5.2 Front plug X3

Pin	Relay contact	Meaning
X3.01	–	–
X3.02	Common contact	Channel 0.00
X3.03	NO contact	Channel 0.00
X3.04	NC contact	Channel 0.00
X3.05	–	–
X3.06	Common contact	Channel 0.01,0.02,0.03
X3.07	NO contact	Channel 0.01
X3.08	NO contact	Channel 0.02
X3.09	NO contact	Channel 0.03
X3.10	–	–
X3.11	–	–
X3.12	Common contact	Channel 0.04
X3.13	NO contact	Channel 0.04
X3.14	NC contact	Channel 0.04
X3.15	–	–
X3.16	Common contact	Channel 0.05,0.06,0.07
X3.17	NO contact	Channel 0.05
X3.18	NO contact	Channel 0.06
X3.19	NO contact	Channel 0.07
X3.20	–	–
X3.21	–	–
X3.22	Common contact	Channel 0.08
X3.23	NO contact	Channel 0.08
X3.24	NC contact	Channel 0.08
X3.25	–	–
X3.26	Common contact	Channel 0.09,0.10,0.11
X3.27	NO contact	Channel 0.09
X3.28	NO contact	Channel 0.10
X3.29	NO contact	Channel 0.11
X3.30	–	–
X3.31	–	–
X3.32	Common contact	Channel 0.12
X3.33	NO contact	Channel 0.12
X3.34	NC contact	Channel 0.12
X3.35	–	–
X3.36	Common contact	Channel 0.13,0.14,0.15
X3.37	NO contact	Channel 0.13
X3.38	NO contact	Channel 0.14
X3.39	NO contact	Channel 0.15
X3.40	–	–

The connections 2, 3, 4 / 12, 13, 14 / 22, 23, 24 / 32, 33, 34 are designed as three-polar like changeover contacts; the connections 6, 7, 8, 9 / 16, 17, 18, 19 / 26, 27, 28, 29 / 36, 37, 38, 39 are designed as four-polar like make contacts.

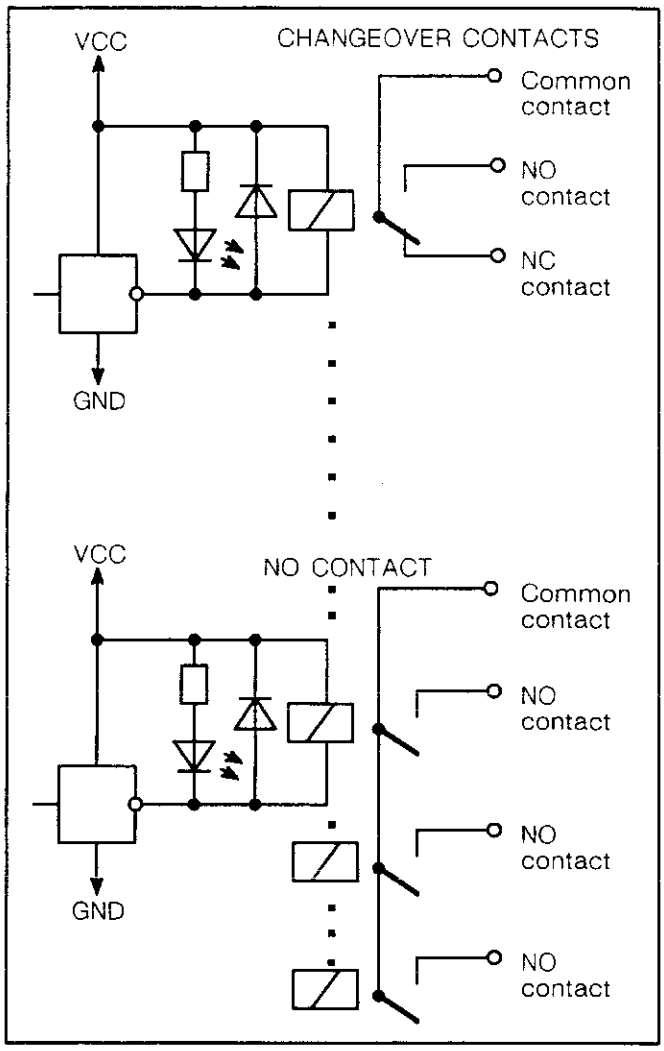
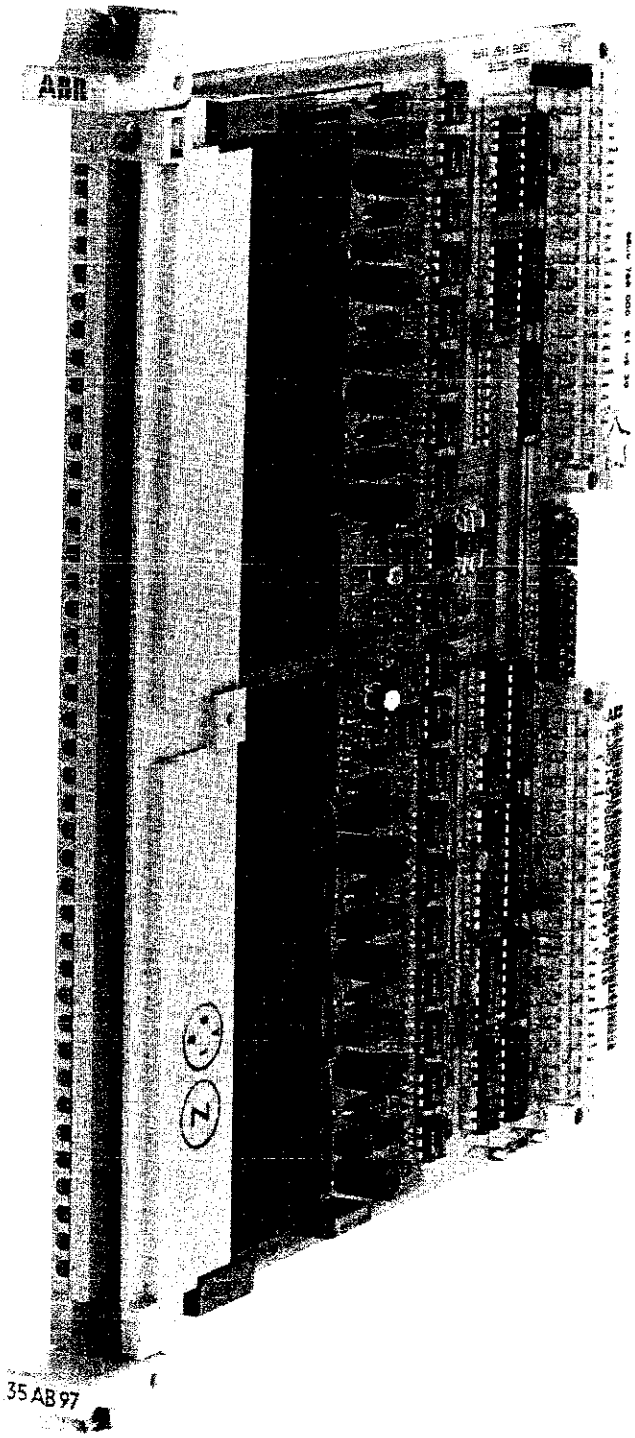


Fig.15.5-3 Output connection

15.6 Binary output unit 35 AB 97 R2



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15.6.1 Technical data

Supply voltage U_{B1}	+ 5 V ± 5 %
Current input I_{B1} with U_{B1}	typically < 0.3 A
Power loss	12 W (with 8 A residual current)
Fan operation	yes
Channels per unit	16
Short-circuit common signal output K	Signal output K has a 1 signal with overcurrent or a short-circuit (red LED) for one or several outputs. Signal output can be switched parallel.
Release input F	1 signal on the release input F (green LED) releases the output channels, 0 signal switches them off.
Input voltage	
Nominal value	+ 24 V
for release	+ 13 V ... + 33 V
for holding	- 33 V ... + 5 V
Input current (with release)	typically 5 mA
Line length (unscreened)	max. 200 m
Acknowledgement input Q	A 1 signal causes the output channel to be switched on again after removing the short-circuit, if the device is in the operating mode "external acknowledgement". (green LED)
Input voltage (external)	
(ext.) nominal value	+ 24 V
for acknowledgement	+ 13 ... + 33 V
Input current (acknowledgement)	typically 7 mA
Line length (unsreend)	max. 200 m
Current supply (on the front):	
Supply voltage U_{P1}	+ 24 V ± 30 %
Output voltage	
1 signal with Imax	U_{P1} - 3 V
0 signal, output unloaded	< 0.4 V
Output current	
Nominal value	2 A with UP1 = 24 V
Current switched, permitted range	0.01 ... 2 A
Residual current with 0 signal	max. 1 mA
Inductive load	100 %
Demagnetization	via a free-wheeling diode
Limit inductive cut-out voltage	UP1 = - 47 V
Operating frequency with an inductive load	2 Hz (with 1 A); 0,1 Hz (with 2 A)
Lamp load, nominal current	300 mA
Loadability of the front plugs	4 A per plug
Line length (unscreened)	max. 400 m
Switch frequency for lamps	max. 11 Hz with max. 10 W
Short-circuit resistance	yes, automatic switch-on again after removing the short-circuit or acknowledgement via the binary input (X3.30)
Residual output current for unit	8 A
Electrical isolation	yes, via optocouplers in groups of 8

Parallel connection of the output channels	max. 2 channels (4 A); the parallel connection of the following channels is allowed: 0.00 and 0.01, 0.02 and 0.03, 0.04 and 0.05, 0.06 and 0.07, 0.08 and 0.09, 0.10 and 0.11, 0.12 and 0.13, 0.14 and 0.15
Signalization of the power outputs	one yellow LED per channel
Signalization of the short-circuit signal	one red LED
Signalization of the release input	one green LED
Signalization of the acknowledgement input	one green LED
Electro magnetic compatibility	in accordance with IEC 801/4
Thermal protection	The output drivers are switched off with too high a thermal load.
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	in accordance with VDE 0160
Dimensions	1 pitch
Weight	0.5 kg
Order number:	GJR5145700R2

Accessories:

Front plug 35 ST 90 R1	GJR5144900R1
Label set 35 SB 90 R8	GJR5144600R8

15.6.2 Description

The binary output unit 35 AB 97 is a passive subscriber on the MPST bus. 16 channels with a loadability of 2 A are converted from the MPST bus to the front plug terminals. The 16 output channels are divided into 2 groups of 8 channels each. The unit supplies 24 V signals and is resistant to short-circuits. The output signals can only be "written" (in words and bytes).

A short-circuit signal is output to the MPST bus, if a short-circuit occurs when reading the unit address.

Diagnosis signal ADET
It can be ascertained with the signal ADET (Address detect signal) and a corresponding unit, whether an addressed unit is present, not present or present many times. The signal ADET is output to the bus with a successful address comparison (unit addressed). This signal can be switched off (remove the resistor assembly R197).

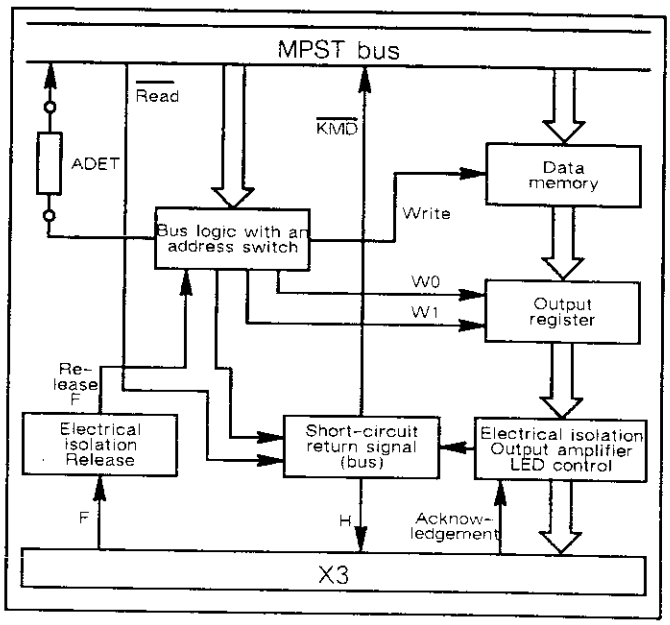


Fig.15.6-1 Block diagram

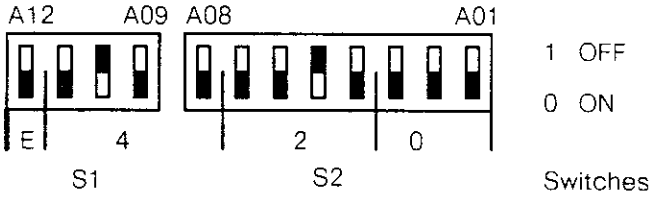
15.6.3 Unit addresses

15.6.3.1 Address setting

The addresses "A1" to "A12" of the card are set with the switches S1, S2 (4 bit and 8 bit DIL switches). The separate switch elements can be accessed by opening the transparent cover. See Fig. 15.6-2 for the position of the switches.

Example for setting the unit address:

Selected unit address: E420



(A15 ... A13: always equal 1 for in-/output units
A00: selection of the channel group)

15.6.3.2 Address division

The MPST bus address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X
T300 code of the upper, passive address area (perm. wired up)			S1 The unit address for switch S1 and S2 can be adjusted. Setting ON = 0				S2								

A00	W0	Data	Output channel
1	0	D07 ... D00	0.07 ... 0.00
0	0	D15 ... D08	0.15 ... 0.08
0	1	D15 ... D00	0.15 ... 0.00

15.6.3.3 Assembly positions

The assembly position ADET (address detect signal, see Fig.15.6-2 and Fig. 15.6-3) is equipped with a resistor R197 (100 Ohms) by the factory.

15.6.4 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

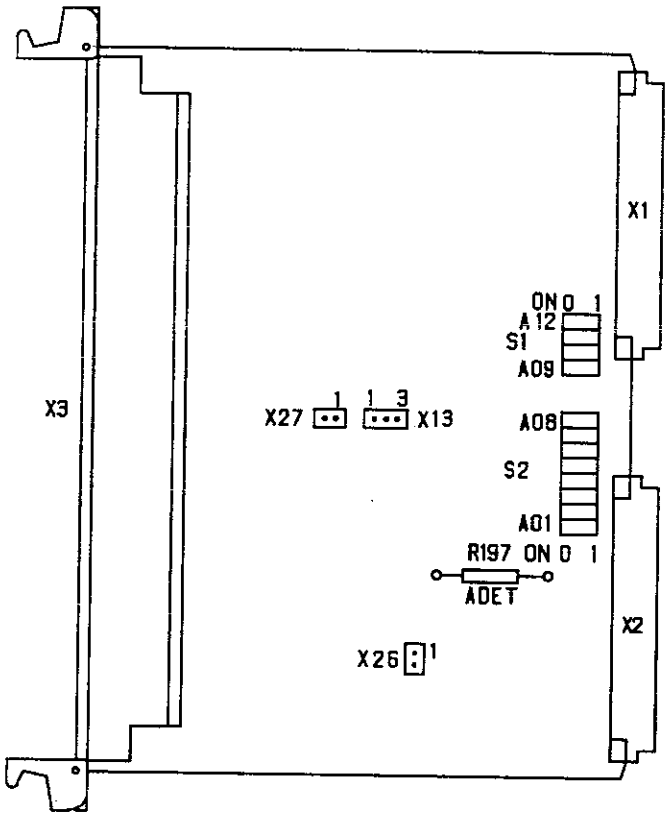


Fig. 15.6-2 Component side (top view) with the printed board GJR5145711P1 (solder side)

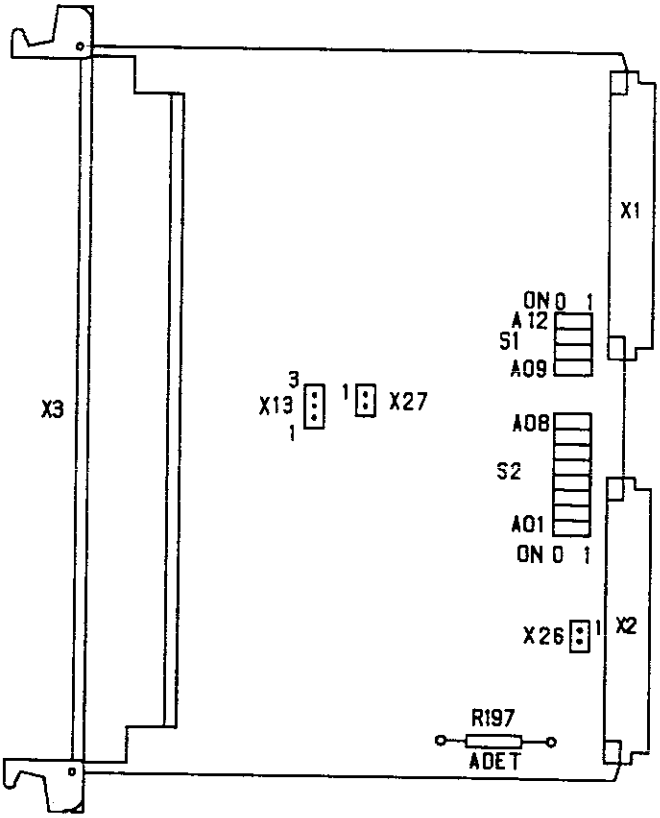


Fig. 15.6-3 Component side (top view) with the printed board GJR5145711P2 (solder side)

Displays:

- 32 LEDs, yellow colour, to display the output signals
- 1 LED, red colour, to display the short-circuit signal
- 2 LEDs, green colour, to display the release and acknowledgement

Plug connectors:

X1, X2	32-polar MPST bus interface according to DIN 41 612, part 2, design C
X3	40-polar periphery interface (process data, +24 V, 0 V, free positions)

X13 Jumpers 1-2: external acknowledgement.
Jumpers 2-3: automatic acknowledgement

X26 Short-circuit signal to the MPST bus
Jumpers 1-2: D15

X27 Jumpers 1-2: ZP1.0-ZP1.1 connection (0 V external)
Channel 0.00 ... 0.07 and 0.08 ... 0.15

Factory settings:

- Automatic acknowledgement (short-circuit): X13/2-3
- Data bit D15=0 signal for short-circuit: X26/1-2
- Connecting the process voltage ZP1 of the channel groups 0...7 with the channel groups 8...15: X27/1-2

15.6.5 Plug assignment

15.6.5.1 MPST bus interface, plugs X1,X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	UB1	5 V voltage	X1. 2c	UB1	5 V voltage
X1. 4a	UB1	5 V voltage	X1. 4c	UB1	5 V voltage
X1. 6a	–	–	X1. 6c	–	–
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	WO	Word transfer	X1.24c	$\overline{\text{PFD}}$	Power Fail Detect
X1.26a	–	–	X1.26c	–	–
X1.28a	–	–	X1.28c	–	–
X1.30a	–	–	X1.30c	–	–
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{\text{BOV}}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	–	–	X2.20c	–	–
X2.22a	ADET	Address Detect Signal	X2.22c	$\overline{\text{RS}}$	Reset
X2.24a	$\overline{\text{W}}$	Write	X2.24c	$\overline{\text{R}}$	Read
X2.26a	$\overline{\text{I/O}}$	I/O memory area	X2.26c	–	–
X2.28a	–	–	X2.28c	–	–
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

15.6.5.2 Front plug X3

Pin	Signal name	Meaning
X3.01	U P1	Process voltage
X3.02	Output signal	Channel 0.00
X3.03	UP1.0 (0.00, 0.01)	Process voltage
X3.04	Output signal	Channel 0.01
X3.05	ZP1.0 (0.00, 0.01)	0 V process voltage
X3.06	Output signal	Channel 0.02
X3.07	UP1.0 (0.02, 0.03)	Process voltage
X3.08	Output signal	Channel 0.03
X3.09	ZP1.0 (0.02, 0.03)	0 V process voltage
X3.10	–	–
X3.11	Output signal	Short-circuit common signal K
X3.12	Output signal	Channel 0.04
X3.13	UP1.0 (0.04, 0.05)	Process voltage
X3.14	Output signal	Channel 0.05
X3.15	ZP1.0 (0.04, 0.05)	0 V process voltage
X3.16	Output signal	Channel 0.06
X3.17	UP1.0 (0.06, 0.07)	Process voltage
X3.18	Output signal	Channel 0.07
X3.19	ZP1.0 (0.06, 0.07)	0 V process voltage
X3.20	–	–
X3.21	Input signal	Release input F
X3.22	Output signal	Channel 0.08
X3.23	UP1.1 (0.08, 0.09)	Process voltage
X3.24	Output signal	Channel 0.09
X3.25	ZP1.1 (0.08, 0.09)	0 V process voltage
X3.26	Output signal	Channel 0.10
X3.27	UP1.1 (0.10, 0.11)	Process voltage
X3.28	Output signal	Channel 0.11
X3.29	ZP1.1 (0.10, 0.11)	0 V process voltage
X3.30	Input signal	Quitterung Q
X3.31	U P1	Process voltage
X3.32	Output signal	Channel 0.12
X3.33	UP1.1 (0.12, 0.13)	Process voltage
X3.34	Output signal	Channel 0.13
X3.35	ZP1.1 (0.12, 0.13)	0 V process voltage
X3.36	Output signal	Channel 0.14
X3.37	UP1.1 (0.14, 0.15)	Process voltage
X3.38	Output signal	Channel 0.15
X3.39	ZP1.1 (0.14, 0.15)	0 V process voltage
X3.40	ZP1	0 V process voltage

The external 0 V connections (ZP1.0, ZP1.1) are interconnected with the closed jumper X27.

Important:
UP1 (X3.1) and ZP1 (X3.40) must always be connected. Otherwise, each output IC (2 channels each) must be supplied separately with UP1.0 or UP1.1 and ZP1.0 or ZP1.1 (0 V ext.) depending on the use (current load of the front contact).

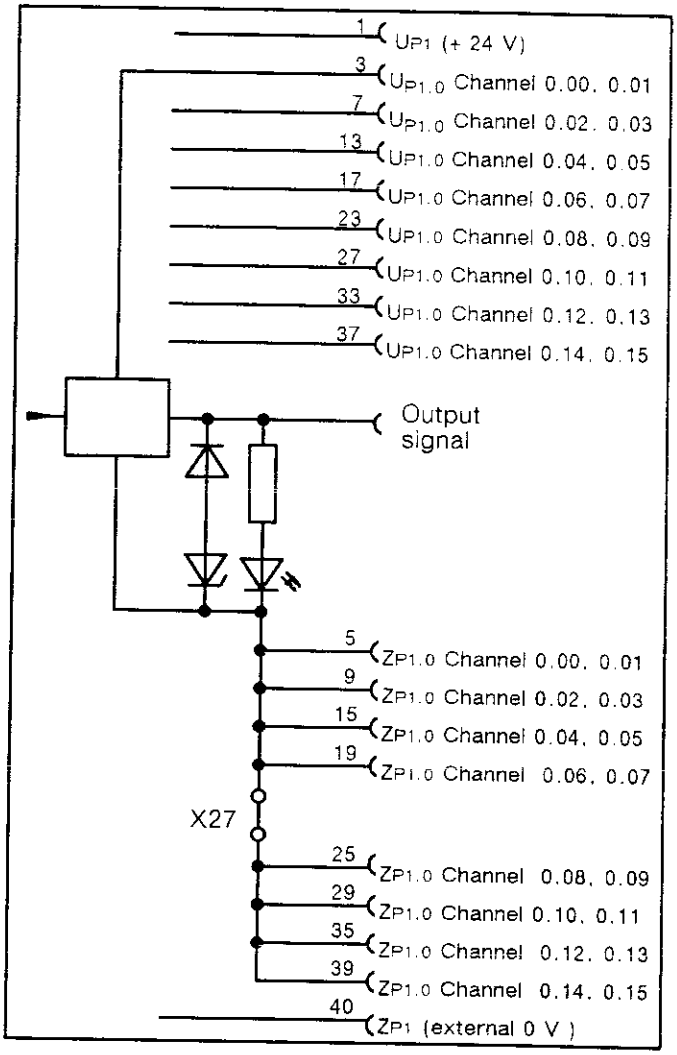


Fig.15.6-4 Output connection

15.6.6 Short-circuit and overload treatment

The following signals are output in the case of a short-circuit on the outputs or an overload:

- Signal output K: 1 signal and
- Diagnoses/short-circuit signal to the MPST bus
  Under the set unit address the D15 data bit can be evaluated with the X26/ 1 - 2 jumper insert.
  D15 = 0 overload or short-circuit at one or several channals
  D15 = 1 no overload or short-circuit
  Note: With the automatic acknowledgement of the short-circuit, the short-circuit signal is not stored, i.e. D02 or D15 became '1' again.

The corresponding channel can

- be switched on again automatically (X01/2-3 bridged) or
- be switched on again with 1 signal after an acknowledgement via the acknowledgement output X3.30 (X01/1-2 bridged) after removing the short-circuit.

16 Analog output units

35 AA 91 R2: Analog output unit, voltage ± 10 V, 16 bit resolution, 4-fold.

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16.1.2 Description 16.1- 3
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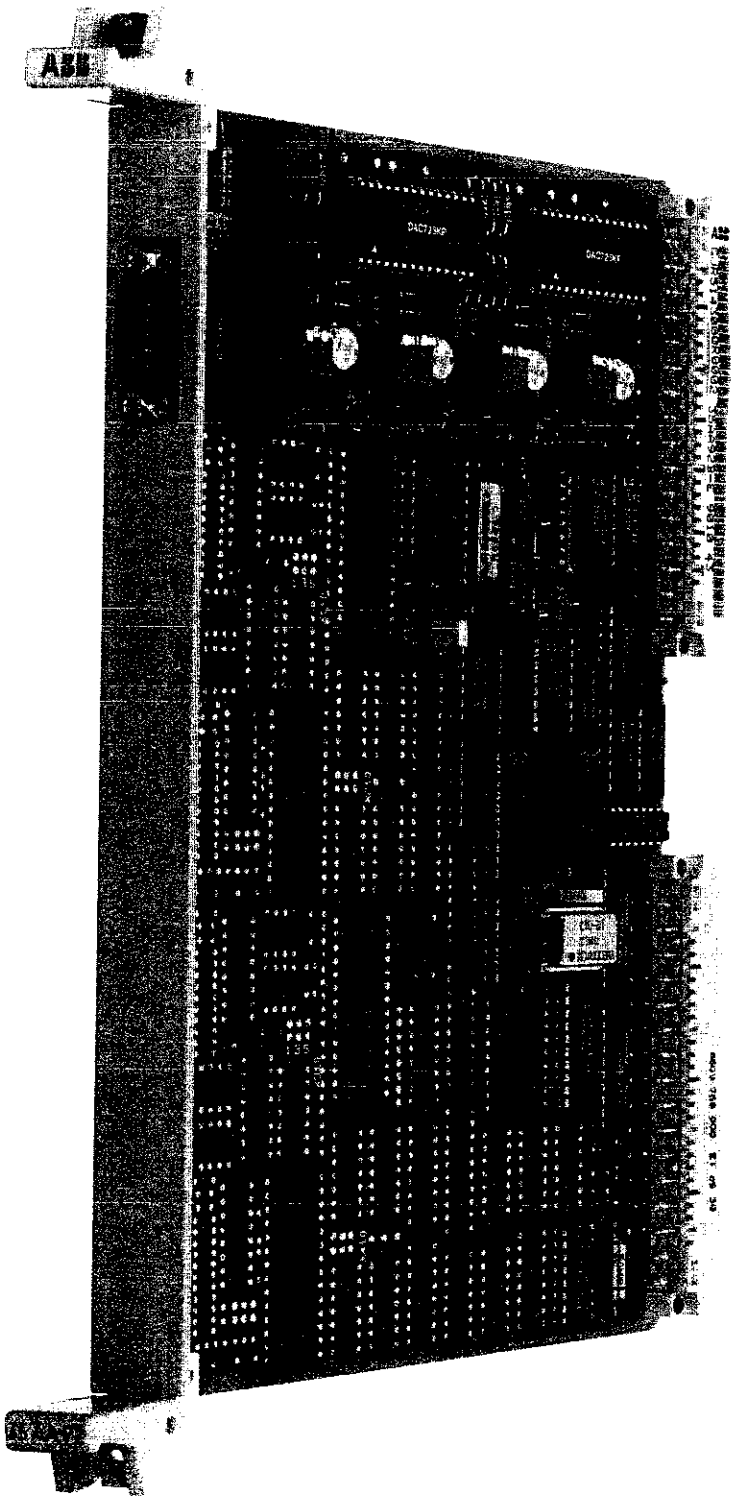
16.1 Analog output unit 35 AA 92 R2



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16.1.1 Technical data

U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+ 15 V ± 5 %
U_{B3} positive supply voltage	− 15 V ± 5 %
I_{B1} supply current for U_{B1}	0.4 A ± 20 %
I_{B2} supply current for U_{B2}	0.1 A ± 20 % plus I_{X7}
I_{B3} supply current for U_{B3}	0.1 A ± 20 % plus I_{X7}

I_{X7} is the output current of the analog amplifier taken from plug X7

Total power loss	6 W
Output data (non-floating):	
For digital value 7FFFH (+ FS)	+ 10 V − 1 LSB
For digital value 8000H (− FS)	− 10 V
Arithmetical resolution (1LSB)	0.305 mV
Monotony	14 bits
Delay of the output amplifier for the output signal change from +FS to −FS	< 200 µs
Loading resistor	> 5 kΩ
Output inductivity bifilar reactor	typically 140 µH
Effective inductivity	typically 1.5 µH
Zero point error:	
With factory zero balance	< 17 mV
With zero balance in the system	< 5 mV
Zero point drift in the permitted temperature range	< 10mV
Output voltage error:	
With factory zero balance	< 17 mV
With zero balance in the system	< 5 mV
Output voltage drift in the permitted temperature range	< 0.08%
Symmetry and linearity error	< 4 mV
Symmetry and linearity drift in the permitted temperature range	< 2 mV
Offset voltage, setting range	typically ± 15 mV
Output voltage, setting range	typically ± 25 mV
Ambient values:	
Ambient temperature	0 °C ... + 55 °C
Storage temperature	− 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 160
Weight	0.4 kg
Dimensions	1 pitch
Order number:	GJR5143000 R2

16.1.2 Description

The analog output 35 AA 92 R2 is a passive subscriber on the MPST bus and mainly executes the following functions:

- Saving for 16 bit speed nominal values in the registers, which can be written by the MPST bus.
- Conversion of the digital nominal value into an analog voltage and output at the drive amplifier (non-floating).
- Output of the output voltage of ±10 V with a unity control-factor setting
- Resetting the output value

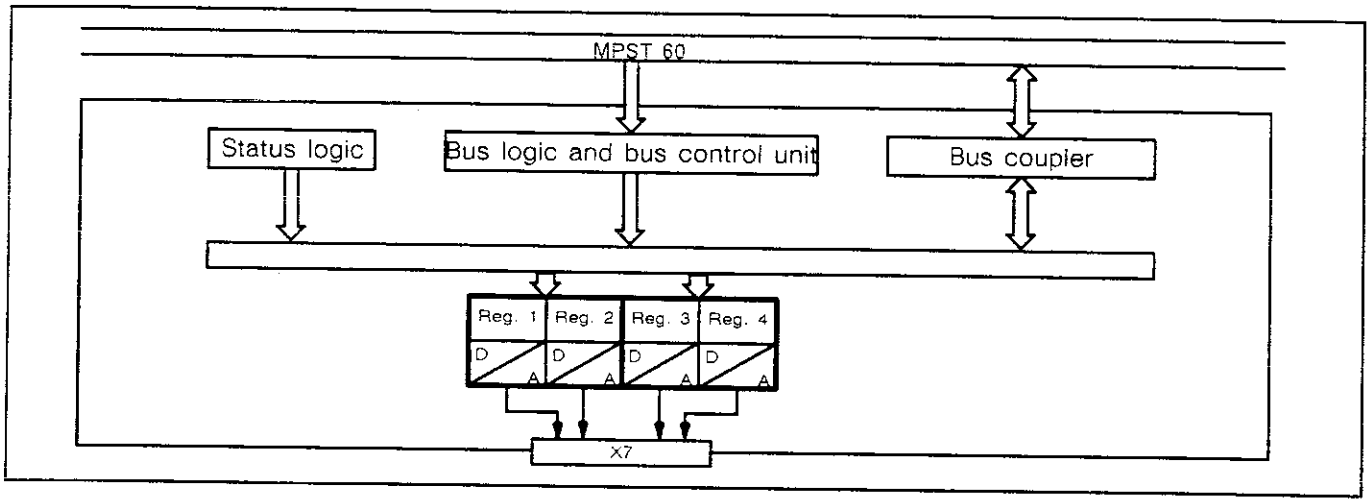

Fig.16.1-1 Block diagram of the analog output 35 AA 92 R2

16.1.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

Plug connectors:

X1, X2	32-polar bus interface according to DIN 41 612, Part 2, design C
X7	Analogue interface, AMP HDP 20, 9-polar

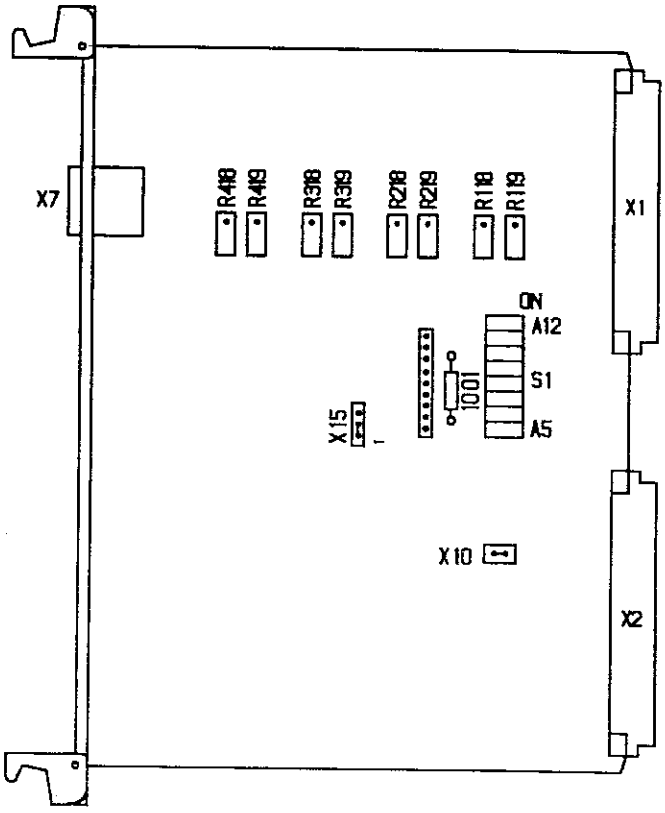

Fig. 16.1-2 Component side (top view)

Pins, which are not drawn, are measuring points, which may not be connected.

16.1.4 Plug assignment

16.1.4.1 MPST bus interface, plugs X1, X2

Plug X1:

Pin	Signal	Meaning	Pin	Signal	Meaning
X1. 2a	U_{B1}	5 V voltage	X1. 2c	U_{B1}	5 V voltage
X1. 4a	U_{B1}	5 V voltage	X1. 4c	U_{B1}	5 V voltage
X1. 6a	U_{B3}	- 15 V voltage	X1. 6c	U_{B2}	15 V voltage
X1. 8a	A00	Address bit 00	X1. 8c	A01	Address bit 01
X1.10a	A02	Address bit 02	X1.10c	A03	Address bit 03
X1.12a	A04	Address bit 04	X1.12c	A05	Address bit 05
X1.14a	A06	Address bit 06	X1.14c	A07	Address bit 07
X1.16a	A08	Address bit 08	X1.16c	A09	Address bit 09
X1.18a	A10	Address bit 10	X1.18c	A11	Address bit 11
X1.20a	A12	Address bit 12	X1.20c	A13	Address bit 13
X1.22a	A14	Address bit 14	X1.22c	A15	Address bit 15
X1.24a	-	-	X1.24c	-	-
X1.26a	-	-	X1.26c	-	-
X1.28a	-	-	X1.28c	-	-
X1.30a	-	-	X1.30c	-	-
X1.32a	ACKo	Acknowledge out	X1.32c	ACKi	Acknowledge in

Plug X2:

Pin	Signal	Meaning	Pin	Signal	Meaning
X2. 2a	D00	Data bit 00	X2. 2c	D01	Data bit 01
X2. 4a	D02	Data bit 02	X2. 4c	D03	Data bit 03
X2. 6a	D04	Data bit 04	X2. 6c	D05	Data bit 05
X2. 8a	D06	Data bit 06	X2. 8c	D07	Data bit 07
X2.10a	D08	Data bit 08	X2.10c	D09	Data bit 09
X2.12a	D10	Data bit 10	X2.12c	D11	Data bit 11
X2.14a	D12	Data bit 12	X2.14c	D13	Data bit 13
X2.16a	D14	Data bit 14	X2.16c	D15	Data bit 15
X2.18a	$\overline{BOV}$	Bus Operation Valid	X2.18c	RDY	Ready
X2.20a	-	-	X2.20c	-	-
X2.22a	-	-	X2.22c	$\overline{RS}$	Reset
X2.24a	$\overline{W}$	Write	X2.24c	$\overline{R}$	Read
X2.26a	$\overline{I/O}$	I/O memory area	X2.26c	-	-
X2.28a	-	-	X2.28c	-	-
X2.30a	0 V	0 V voltage	X2.30c	0 V	0 V voltage
X2.32a	0 V	0 V voltage	X2.32c	0 V	0 V voltage

16.1.4.2 Front plugs

Analog interface (plug X7):

PIN	Signal name	Meaning
X7.1	Ua1	Analogue voltage I
X7.2	0V1	0 V analogue I
X7.3	Ua2	Analogue voltage II
X7.4	0V2	0 V analogue II
X7.5	Ua3	Analogue voltage III
X7.6	0V3	0 V analogue III
X7.7	Ua4	Analogue voltage IV
X7.8	0V4	0 V analogue IV
X7.9	–	Screen

16.1.5 Unit addresses on the MPST bus

16.1.5.1 Address division

The MPST address lines are assigned as follows:

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
1	1	1	X	X	X	X	X	X	X	X	X	X	1	0	0
MPST code of the upper, passive address area (perm. wired up)			Unit address for S1 on the analogue output 35 AA 92 can be adjusted. (See also 16.1.6.1)								Address of the functional unit		Writing in the digital value		

16.1.5.2 Address overview

	Access	Address	Data
Function 1	Writing	XX**4H	D15...D00
Function 2	Writing	XX**CH	D15...D00
Function 3	Writing	XX *4H	D15...D00
Function 4	Writing	XX *CH	D15...D00

16.1.5.3 Addressing the functions

Address bit	4	3
Function 1	0	0
Function 2	0	1
Function 3	1	0
Function 4	1	1

** Bit4 of the address low byte must be set to 0.
* Bit4 of the address low byte must be set to 1.

16.1.6 Settings

16.1.6.1 Setting the unit address

DIL switch S1:

Example for address E500

This unit fills the address area from E500 to E51E. The next unit would then receive the address E520.

16.1.6.2 Setting the jumpers

Jumper **X10** The oscillator jumper must be inserted.

Jumper **X15** always in position 1–2

Assembly position **1001**:
Resistor (R = 150 k) must be soldered in.

16.1.7 Application informations

16.1.7.1 Balancing the analog unit

The advantage of the zero balance of the analog unit in the system is that the zero point error, which is caused by the tolerances of the supply voltages, no longer occurs.

The balancing is carried out, so that the output voltage for the potentiometers

R 119 for function 1	R219 for function 2
R 319 for function 3	R419 for function 4

is set to 0 V (± 0.1 mV) with the nominal value 0. Turning the potentiometer to the right enlarges the output voltage.

The gain balancing with + FS is required after the zero balance. The balancing is carried out, so that the output voltage for the potentiometers

R 118 for function 1	R218 for function 2
R 318 for function 3	R418 for function 4

is set to + 10 V (± 1 mV) with the set value 7FFFH. Turning the potentiometer to the right causes an enlargement of the output voltage. At least a 4 1/2-digit digital voltmeter is to be used for the balancing. The symmetry with – FS (nominal value = 8000H) is to be checked afterwards. The difference between the amounts of + FS and – FS must be $\leq$ 2 mV. The difference can be set to 1 mV when using a 5 1/2-digit measuring device. The balancing should be carried out with a connected load and using a screened measuring line. The potentiometers are to be secured with fuse lacquer after the balancing.

16.1.7.2 Differences between rubrics R1 and R2

There is no functional difference between the units of R1 and R2.

	Rubric	
Comment	R1	R2
IB2	0.15 A	0.1 A
IB3	0.15 A	0.1 A
D/A converter IC/axis	1 item	0.5 item
Zero point error *)	< 10 mV	< 17 mV
Output voltage error *)	< 10 mV	< 17 mV
Output voltage drift	< 15 mV	< 15 mV
Symmetry and linearity drift	< 4 mV	< 2 mV
EMC improvement		yes

*) Factory balancing

17 Communication processors

35 KP 90 R101: Communication processor for the connection to the PROFIBUS
in preparation

35 KP 91 R101: Communication processor for the connection to the MASTER via an EXCOM interface
in preparation

35 KP 92 R101: Communication processor for the connection to the VERITRON® converter,PAD type.

17.3 Communication processor 35 KP 92 R101 ..... 17.3- 1

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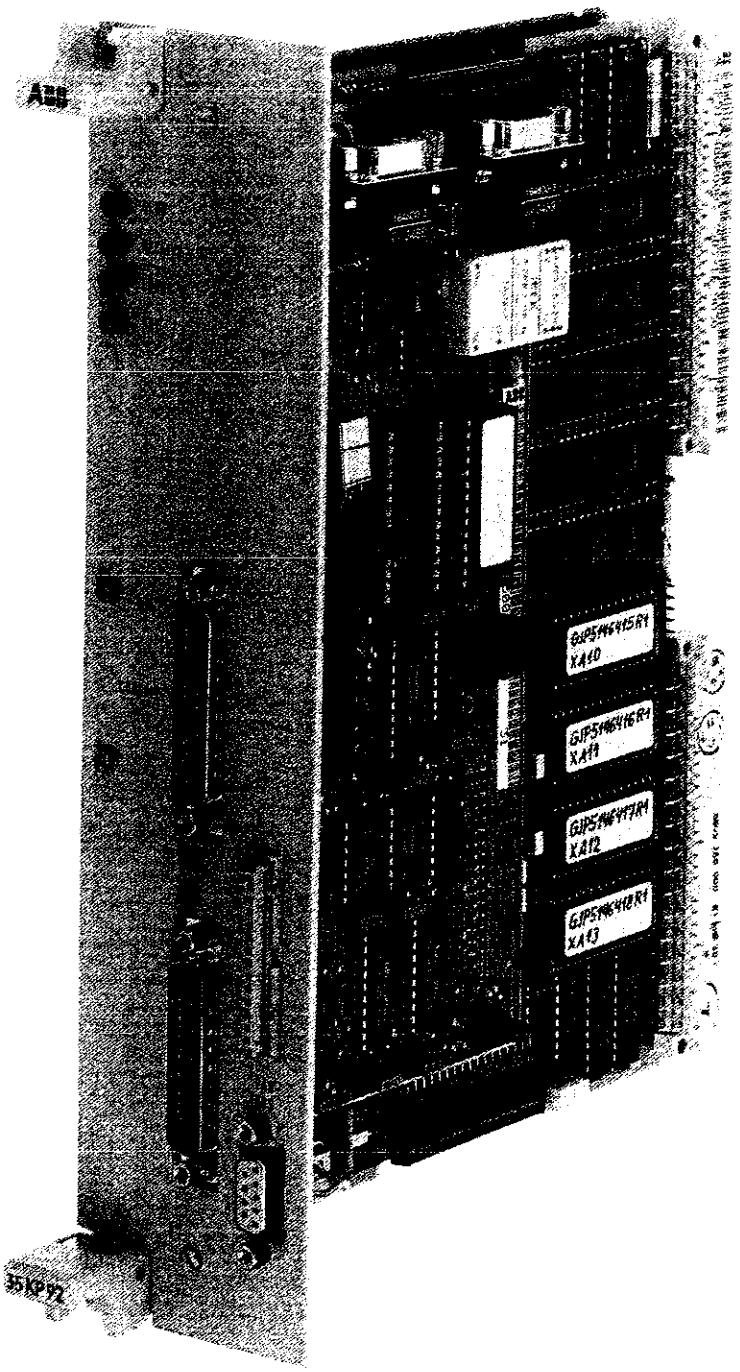
17.3.2 Description 17.3- 2

17.3.3 Overview system configuration and data change 17.3- 2

17.3.4 Notes for planning 17.3- 2

17.3.5 PAD components and contact address 17.3- 2

17.3 Communication processor 35 KP 92 R101



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17.3.1 Technical data

U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+15 V ± 5 %
U_{B3} negative supply voltage	−15 V ± 5 %
I_{B1} for U_{B1}	3.6 A ± 30 %
I_{B2} for U_{B2}	0.1 A ± 30 %
I_{B3} for U_{B3}	0.1 A ± 30 %
Power loss	max. 30 W
Communication with PAD:	
Number of PADs per communication processor	1 ... 5
Number of fast data words (nominal values) per PAD	4
Number of slow data words (nominal values) per PAD	0 ... 10
Number of fast data words (actual values) per PAD	4
Number of slow data words (actual values) per PAD	0 ... 10
Cycle time for updating fast data words	3 ms/PAD
Interface console:	
Transmission level	RS-232-C
Baud rate	9600 Baud
Transmission protocol	8 bit, no parity
PAD bus:	
Baud rate	375 kbits/s
Transmission level	RS 485
Transmission protocol	HDLC/SDLC
Coding	NRZI
Max. cable length	200 m
Line	two-wire, twisted, shielded, Zo ≥ 120 Ω
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity	F
Mechanical stress when installed	VDE 160
Dimensions	3 pitches
Weight	2.2 kg
Order number	GJR5146400R101

17.3.2 Description

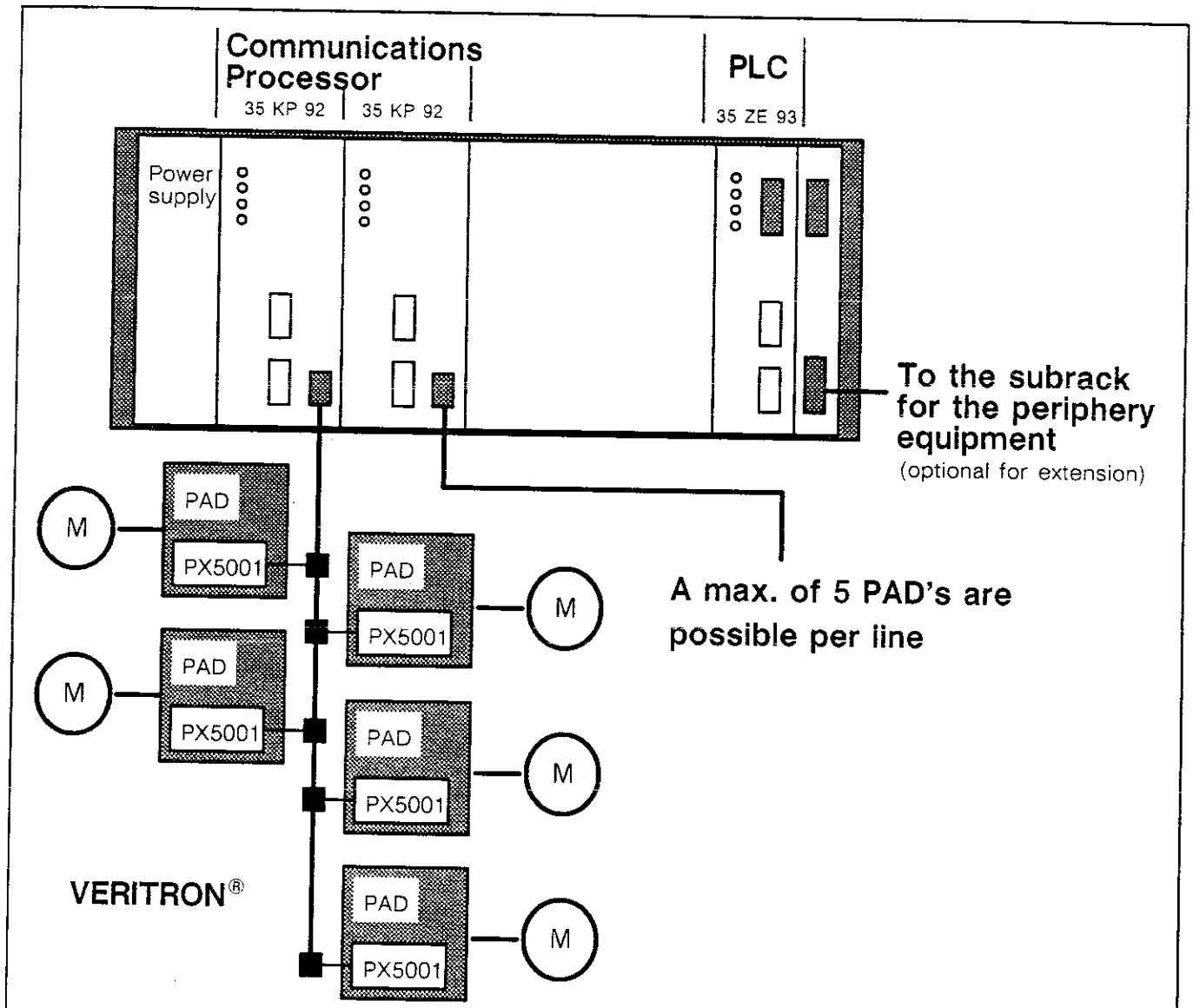
The communication processor 35 KP 92 R101 allows the digital connection between the ABB Procontic T300 system and the VERITRON® converters, PAD type.

A 35 KP 90 R101 communication processor allows a processor (e.g. PLC) to access a maximum of 5 VERITRON® converters, PAD type.

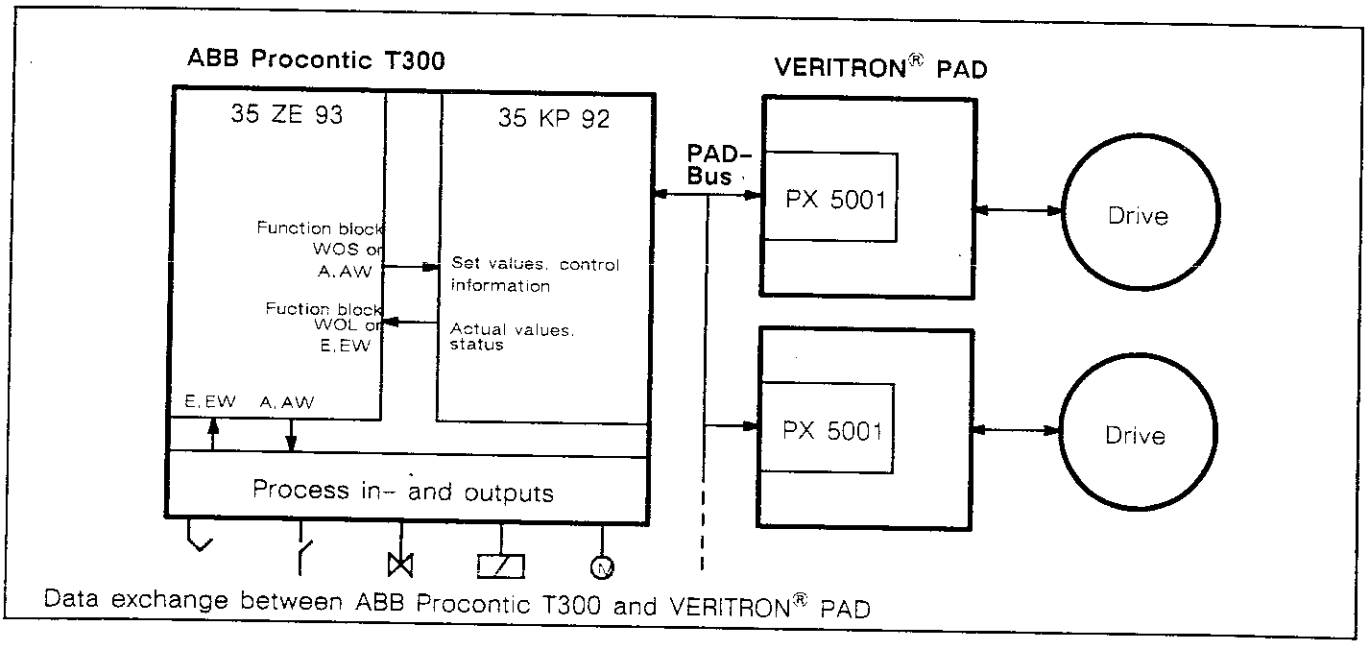
The drive amplifiers are connected via a rapid, serial RS 485 bus over the digital coupling

The extend of deliveryy of the 35 KP 92 R101 contains the 35 KP 92 R101 communication processor, a disk with a PLC example program for the 907 PC 31 and the functional description 'Communication Processor 35 KP 92 R101'. This description contains in detail the 35 KP 92 R101. It can also be requested under the order number GATS 1315 09 R1001.

17.3.3 Overview system configuration and data change



Example for the system configuration with 35 KP 92



Data exchange between ABB Procontic T300 and VERITRON® PAD

17.3.4 Notes for planning

Unit address

The 35 KP 92 R101 occupies 4 kbyte in the active address area of the MPST bus. The unit address of the 35 KP 92 R101 communication processor is factory preset on 3F00H (segment address of the active subscribers '0FH'). The communication processor occupies 4 kbyte from the setting segment address on. The user has to test his system configuration, that another unit has the same address area.

MPST bus clock

The MPST bus clock may only be availiable on one T300 processor (normally on the PLC). The 35 KP 92 R101 is factory preset without the MPST bus clock.

Subrack

Several 35 KP 92 R101 may be inserted in a T300 subrack (**only basic** subrack).

The communication processors have to be inserted to the left, in the basic subrack, of all processors (PLC, IR etc.), of all preprocessors (e.g. OMS-F) and of all units working with an interrupt (e.g. 35 EB 92).

17.3.5 PAD components and contact address

Contact address for Business Unit ABB Drives:

ABB Antriebstechnik GmbH
Postfach 1180
D-6840 Lampertheim
Telephone: 06206 503-393 (Sales)
Telephone: 06206 503-374 (Service)
Telefax: 06206 503-561
Telex: 4 624 411 605 bbd

VERITRON® -
Double converter
with microprocessor
Type series PAD/PSD
Three phase connection
30 A- ... 1650 A-
Order No.: see operating instructions

Projection catalogue with basic operating instructions:Double converter
Double converter
with microprocessor
Type series PAD/PSD
Three phase connection
30 A- ... 1650 A-
Description No.: D EA 5247 89 E
Order No.: GNV 95247 89 E

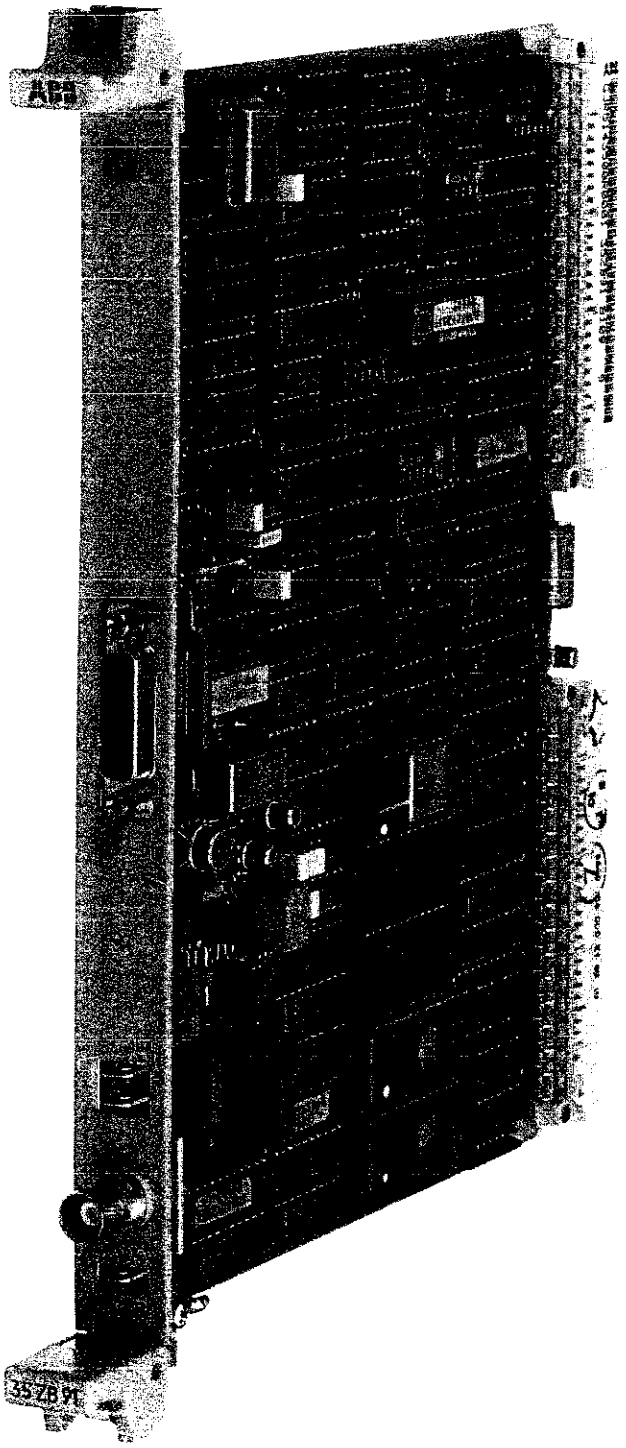
Subprint communications unit PX 5001
Order or.: 523526

18 Coupler

35 ZB 91 R1: Coupler between the ABB Procontic T300 and the ABB Procontic field bus ZB10.

18.1 Coupler between ABB Procontic T300 system and ABB Procontic field bus ZB10, 35 ZB 91 R1 ..... 18.1- 1
18.1.1 Technical data 18.1- 2
18.1.2 Description 18.1- 3

18.1 Coupler between the ABB Procontic T300 system and the ABB Procontic field bus ZB10, 35 ZB 91 R1



90 07 02

18.1.1 Technical data

Current supply:	
U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+ 15 V ±5 %
I_{B1} for U_{B1}	typically 1.4 A, max. 2.1 A
I_{B2} for U_{B2}	typically 10 mA, max. 15 mA
External supply via faston plugs:	
U_{P1} positive supply voltage	24 V, min. 19.2 V, max. 31.2 V
I_{P1} for U_{P1} without a branch unit	typically 10 mA
I_{P1} for U_{P1} with a branch unit	typically 0.1 A, max. 0.15 A
Power loss P	typically 7 W
Ambient conditions:	
Ambient temperature	0 °C ... + 55 °C
Storage temperature	- 25 °C ... + 75 °C
Humidity rating	F
Mechanical stress when installed	VDE 0160

Technical data of the ABB Procontic field bus

The unit 35 ZB 91 R1 fulfills	the general technical data of the ABB Procontic field bus ZB10
Transmission speed	150 kbits/s
Data scope	The coupler can transmit the complete data image of the ZB10. Sending 250 source data telegrams to the ZB10 Receiving 250 source data telegrams from the ZB10 A special memory area of 512 words is available for list data.
Cut-in behaviour	No source data telegrams are sent for approx. 1 s, after the coupler has been switched on. Source data, which are not yet written, are sent as 0.

Tecnical data of the ABB Procontic T300

The unit 35 ZB 91 R1 fulfills	the general technical data of the ABB Procontic T300
In- and output values	according to DIN 66264
Weight	0.36 kg
Dimensions	1 pitch
Order number	GJR5143500R1

Accessories

Branch line cable (89 IZ 20 R1000)	GJR2362600R1000
Branch line cable (89 IZ 20 R3000)	GJR2362600R3000
EPROMs for the allocation table (2 are required)	GJTN160212P1

18.1.2 Description

The ZB10/T300 coupler 35 ZB 91 R1 connects the ABB Procontic T300 to the ABB Procontic field bus ZB10.

Two interfaces are selectively available for the ZB10:
- Direct connection to the ZB10 in the 50 Ω version (TRIAX). The branch connection is integrated; the connection is made via a BNC socket on the front panel of the 35 ZB 91.
- Line interface to connect a separate ZB10 branch unit. The connection to this branch unit is a 15-polar plug-in branch line with a socket on the front panel.

The 35 ZB 91 R1 unit is a subscriber incapable of management on the ZB10 bus. It appears on the MPST bus as an in-/output unit. The address area and the data scope are adjustable in levels.

Data to be exchanged are stored in an image memory (RAM), to which the ZB10 and the ABB Procontic T300 have central access.

The selection of the data to be exchanged, the direction of transmission and the distribution into ZB10 telegrams is pregiven with an allocation table.

16 bit data are exchanged in close succession. The data are not processed.

A separate segment of 512 words of the image memory is provided for the exchange of list data. The address area can be set separately.

More details concerning the 35 ZB 91 R1 coupler are included in leaf 3.1, ABB Procontic field bus ZB10, Hardware (GATS135001R1001), in leaf 3.2, ABB Procontic field bus ZB10, planning (GATS135002R1001).

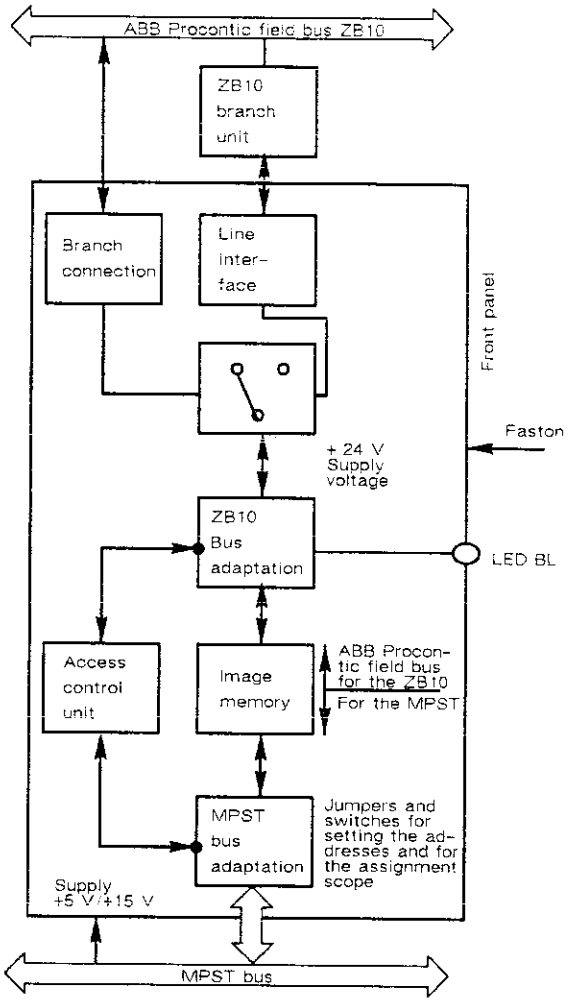


Fig.12.1-1: Block diagram of the 35 ZB 91 R1 coupler

19 Service auxiliary units

35 SH 90 R1: Bus extension.
35 SH 91 R1: Bus display.
35 SH 94 R1: Axis simulator.

Contents, chapter 19

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19.1.2 Description 19.1- 2
19.1.3 Mechanical structure 19.1- 2

19.2 Bus display 35 SH 91 R1 . 19.2- 1
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19.2.2 Description 19.2- 2
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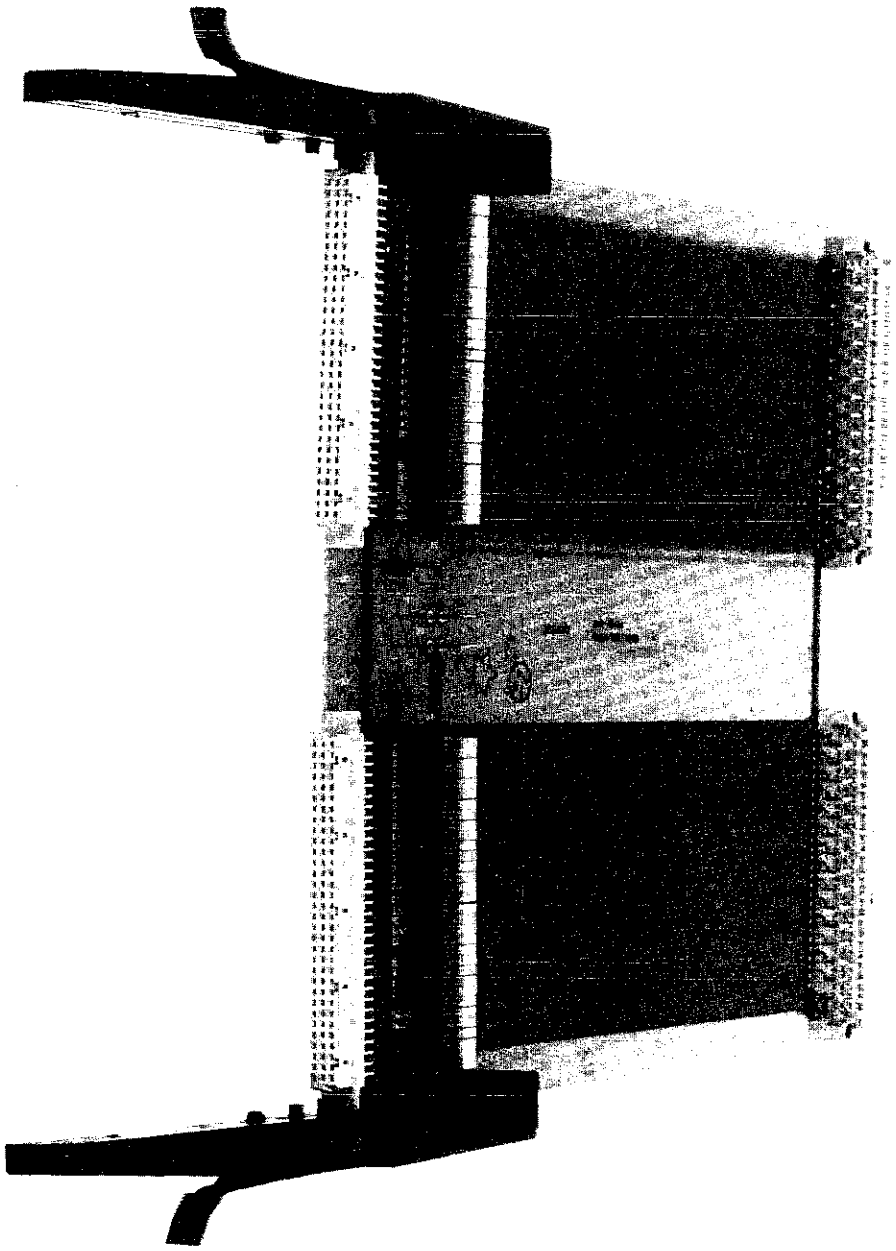
19.1 Bus extension 35 SH 90 R1



85 15 91

19.1.1 Technical data

Ambient temperature	0 °C ... 55 °C
Storage temperature	-25 °C ... 75 °C
Humidity rating	F
Mechanical stress when installed	according to VDE 0160
Dimensions	1 pitch
Weight	0.3 kg
Order number	GJR5136700R1

19.1.2 Description

The bus extension card 35 SH 90 is a test auxiliary unit. It serves to extend the bus in the subrack to the front and offers the possibility to separate and to measure all bus lines separately. The unit sitting on the bus extension card projects over the subrack, so that the measuring procedure and other operations can be carried out without problems. The connections X9.1 (+5 V) and X9.2 (0 V) are available as 6.3 mm faston pins.

19.1.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm,1 pitch.

The bus extension card is provided with a mechanical holder or guide at the front on the top and bottom, in order to prevent the sample from falling down.

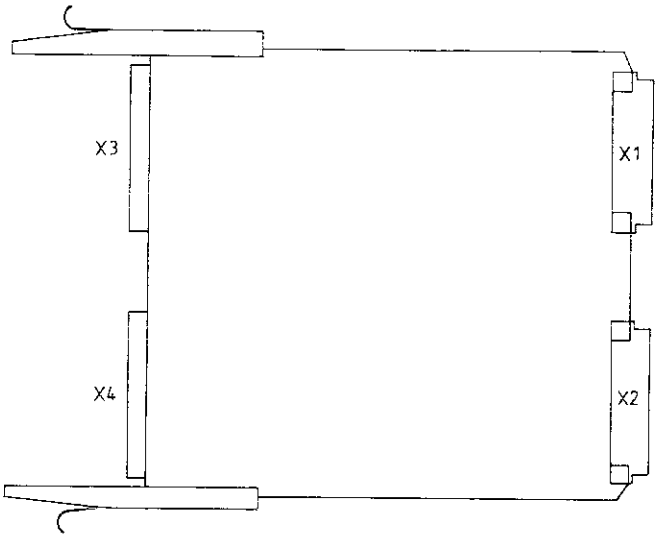
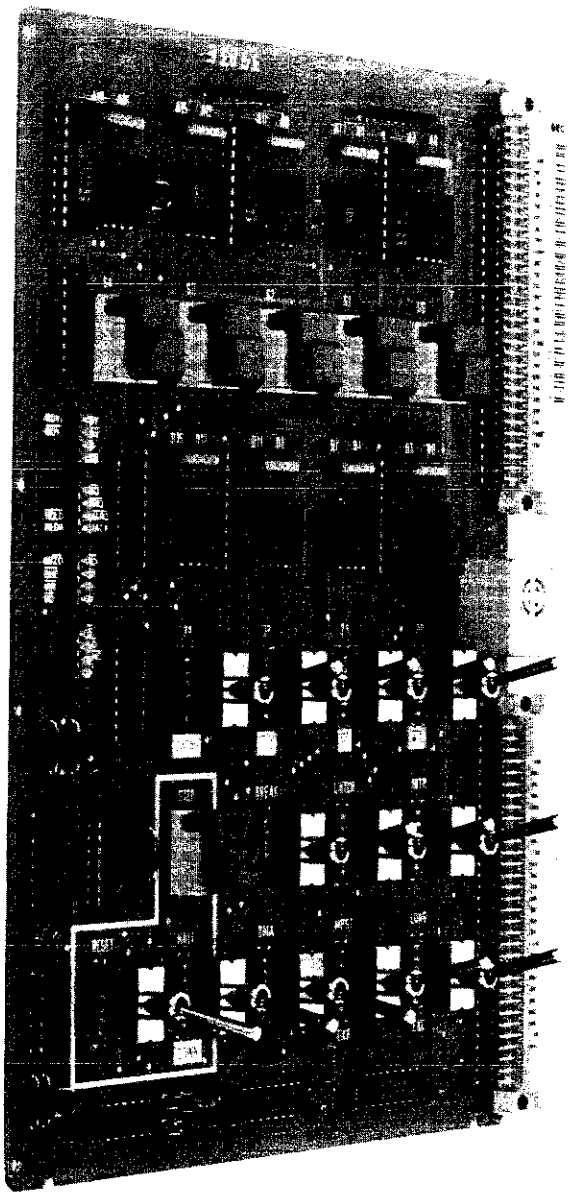


Figure 19.1-1 Top view

19.2 Bus display 35 SH 91 R1



90 01 89

19.2.1 Technical data

U_{B1} positive supply voltage	+5 V ± 5 %
U_{B2} positive supply voltage	+15 V ± 5 %
Typical supply currents	
I_{B1} for U_{B1}	1.7 A, max. 2.0 A
I_{B2} for U_{B2}	0.1 A, max. 0.2 A
Ambient temperature	0 °C ... 55 °C
Storage temperature	-25 °C ... 75°C
Humidity rate	F
Mechanical stress when installed	according to VDE 160
Interfaces	
Fan-in of X1 and X2	I_{iH} < 0.04 mA
	I_{iL} < 1.6 mA
Exception: Data and addresses!	I_{iH} < 0.06 mA
	I_{iL} < 0.2 mA
Fan-out of X1 and X2	I_{oL} > 8.0 mA
	I_{oH} > 0.4 mA
Exception: $\overline{RS}$, RDY	
Fan-out RDY	I_{oL} = 40 mA
Fan-out $\overline{RS}$	I_{oL} = 20 mA
	I_{oH} = -0.1 mA
Dimensions	1 pitch
Weight	0.4 kg
Order number	GJR5136500R1

19.2.2 Description

The bus display 35 SH 91 is an auxiliary test unit which displays the status of the addresses, data and control signals of the MPST bus.

The unit is used together with the extension card 35 SH 90 so that optimum operation and a good display reading is guaranteed.

Possible display	Possible commands
A00 ... A15, D00 ... D15, RDY, $\overline{BOV}$, $\overline{BB}$, $\overline{RBB}$, $\overline{SRQ}$, $\overline{HSRQ}$, $\overline{DMARQ}$, DMACK $\overline{I/O}$, $\overline{PFD}$, $\overline{SYNC}$, $\overline{CC}$	RESET HALT STEP

19.2.2.1 Application

The displays continuously display the bus status.

A further RESET signal "warm start" can be created with the RESET switch independently of the RESET signal "cold start", which the power supply unit creates, when it is switched on.

Single-step mode:
The processor currently active on the T300 bus is stopped after setting the HALT switch and starting the next valid cycle ($\overline{BOV}$=0). The stopped bus cycle is continued and the next one stopped, when the STEP key is pressed. The single-step mode is left by resetting the HALT switch and pressing the STEP key.

19.2.3 Mechanical structure

Unit in the double-size Eurocard format 160 233.4 mm, 1 pitch.

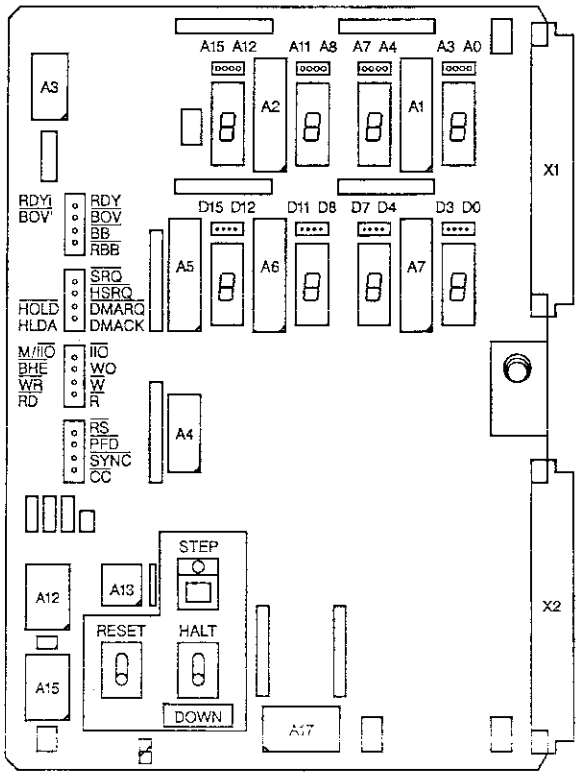
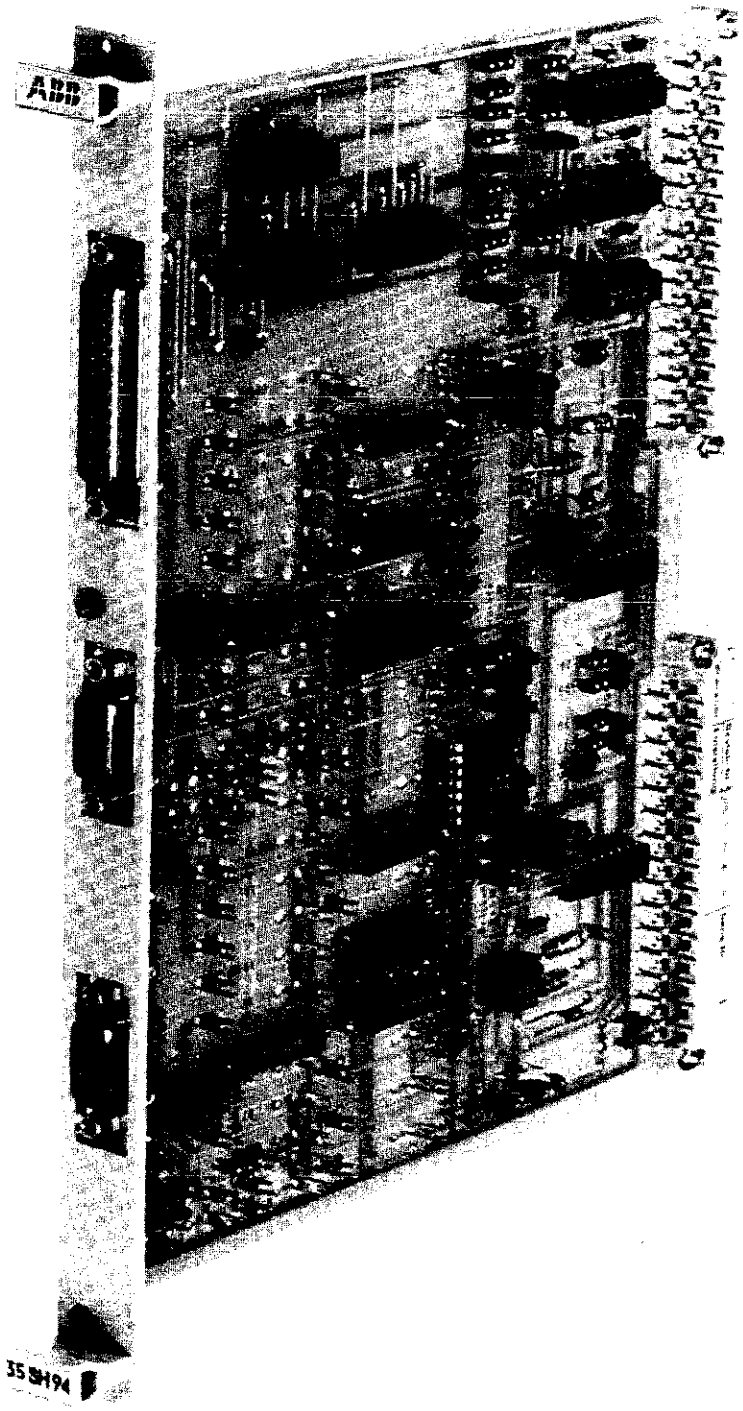


Figure 19.2-1 Component side (Top view)

19.3 Axis simulator 33 SH 94 R1



85 15 93

19.3.1 Technical data

U_{B1} positive supply voltage	+ 5 V ± 5 %
U_{B2} positive supply voltage	+ 15 V ± 5 %
U_{B3} negative supply voltage	− 15 V ± 5 %
I_{B1} for U_{B1}	60 mA ± 20 % + output currents
I_{B2} for U_{B2}	< 1 mA + output currents
I_{B3} for U_{B3}	< 1 mA + output currents
Total power loss	max. 0.5 W
Input values	
Loading resistors E11 and E21	min. 5 kOhm
Loading resistors for creating the sign	1 kOhm to +5 V
Output values	
Actual value and zero pulse	Fan-out = 5 x 74 LS... (TTL)
Integration output A1 and A52	5 mA
Dimensions	1 pitch
Weight	0.4 kg
Order number	GJR513684OR1 and GJR5136840R2

19.3.2 Description

The axis simulator 35 SH 94 is a service auxiliary unit and a passive subscriber at the MPST bus.

The axis simulator 35 SH 94 simulates the part of an axis belonging to the machine, i.e. the control unit (servo amplifier) plus the motor plus the actual value digit emitter (pulse encoder).

The connection X5 of the axis simulator is an integrating analogue output and generally serves to control a recorder.

The axis card supplies a nominal value of max. ± 10 V to the control unit. This voltage serves as an input parameter for the axis simulator 35 SH 94 via the plug-and-socket connection X4. The unit now makes the actual value pulses available for the plug-and-socket connection X3 by an internal, linear voltage/frequency conversion. The pulses are usually supplied by the actual value pulse encoder for the axis card.
If the simulator does not work correctly, it is possible to say whether the malfunction is linked to the axis card or to the machine using the simulation of the machine-specific units of the control unit, motor and actual value pulse encoder.
The axis simulator 35 SH 94 can simulate two axes at the same time and independently of each other!

The plug-and socket connections X3 and X4 of the axis simulator are connected 1:1 with the plug-and-socket connections X3 and X4 of the axis card 35 AE 90. Due to the altered plug arrangement of the axis card 35 AE 92 special plug-and-socket connections are to be used for testing this card!

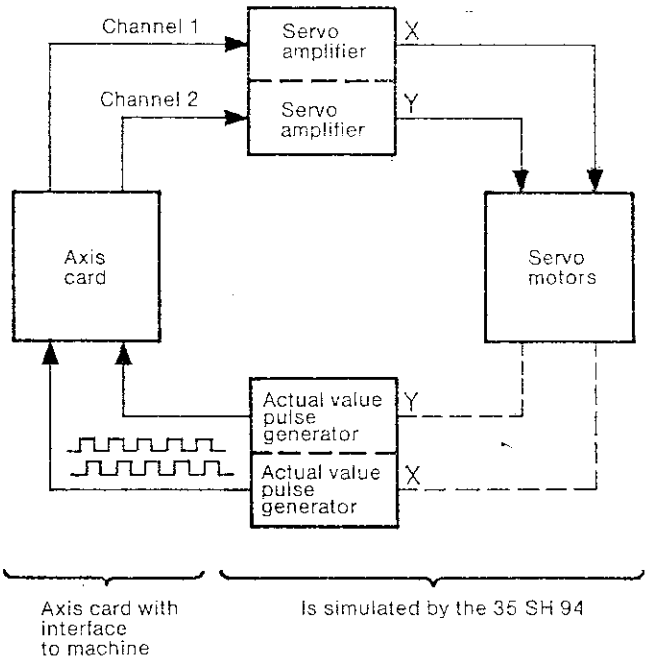


Figure 19.3-1 Functional principle

19.3.2.1 Sign

The sign for the forward or reverse movement is created internally on the simulator. A positive voltage at the nominal value input (analogue input) X4 of the unit means a positive jog direction and a negative voltage in accordance with the negative jog direction.

Attention: The positive jog direction is achieved by a negative voltage at the nominal value input X4 for units of rubric 1, the negative jog direction by positive voltage.

The polarity of the sign can be determined by an external TTL signal by changing the jumpers X74/75 to X/Z75 (channel 1) or X76/77 to X/Z77 (channel 2). An open input or an H signal means a positive jog direction and an L signal negative jog direction.

19.3.2.2 Control behaviour

The user in the position to imitate a machine- specific control parameter as close to reality as possible by means of the component positions 01 to 23 for channel 1 or 51 to 73 for channel 2. A fine adjustment of the control parameters can be carried out with the potentiometers R3 and R7 (channel 1) or R4 and R8 (channel 2). See also the circuitry extract in chapter 7.3.5.

19.3.2.3 Output frequency

The output frequency of the internal U/f converter is adjusted to 250 kHz with 10 V nominal value voltage. This frequency is available as a maximum actual value frequency, which has been reduced four times (62.5 kHz) at the output of the axis simulator for the actual value pulse (plug-and-socket connection X3).

The output frequency of the internal U/f converter can be reduced in steps of 2, 5, 10, 20, 50 and 100, so that actual value frequencies between 62.5 kHz and 625 kHz are available.

T	Jumpers 5	10	50	100	1	2	5/100	20	50/100	$f_{U/f}$ (kHz)
1	X		X		X					250
2	X		X			X				125
5	X		X				X			50
10		X	X				X			25
10	X		X					X		25
20		X	X					X		12.5
50		X	X						X	5
100		X		X					X	2.5

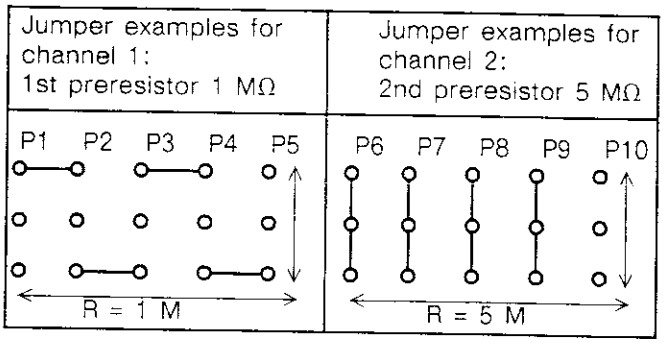
19.3.2.4 Analogue output

The analogue output of each axis consists of an integrator with a secondary OP amplification level.

An output voltage is be received by integration, which is proportional to the path Sx respectively Sy, which is covered by the axes.

The analogue output voltage at X5 will drift 15 V according to the + or – direction with a static input voltage U_x or U_y at the plug-and-socket connection X4!

The preresistor of the integrator (C=0.47 µF) can be altered between 1 MΩ and 5 MΩ by means of four jumpers.



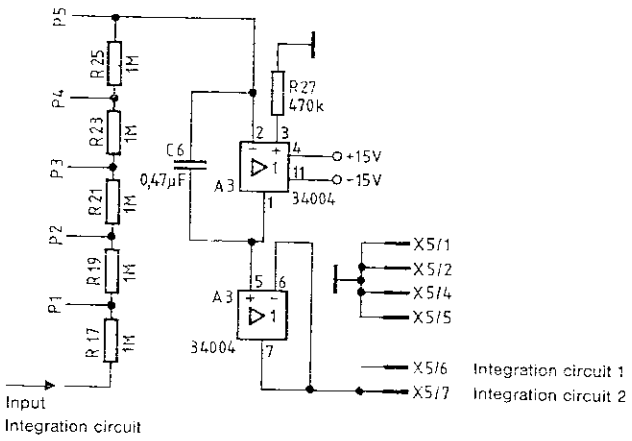


Fig. 7.3-2 Integration circuit for channel 1

19.3.3 Mechanical structure

Unit in the double-size Eurocard format 160 x 233.4 mm, 1 pitch.

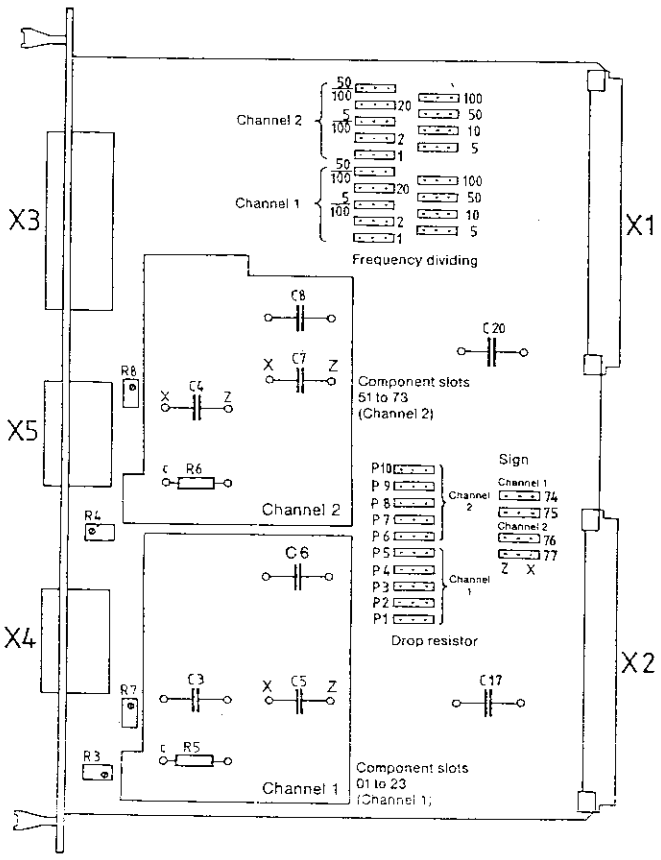


Fig. 19.3-3 Component side (top view)

19.3.4 Plug assignment

Assignment of the plug X3

Code	Connection	Meaning	
A11	14	Path axis 1	0° +
A12	15	Path axis 1	0° –
A13	16	Path axis 1	90° +
A14	17	Path axis 1	90° –
A15	18	Zero mark for axis 1	+
A16	19	Zero mark for axis 1	–
A21	20	Path axis 2	0° +
A22	21	Path axis 2	0° –
A23	22	Path axis 2	90° +
A24	23	Path axis 2	90° –
A25	24	Zero mark axis 2	+
A26	25	Zero mark axis 2	–

Assignment of the plug X4

Code	Connection	Meaning
E11	6	Analogue input 1
E21	7	Analogue input 2
E13	1	0 V to analogue input 1
E13	2	
E23	4	0 V to analogue input 2
E23	5	
E14	8	TTL signal for sign 1
E24	9	TTL signal for sign 2

Assignment of the plug X5

Code	Connection	Meaning
A51	6	Integration output 1
A52	7	Integration output 2
A53	1	0 V to output 1
A54	2	
A55	4	0 V to output 2
A56	5	

19.3.5 Settings

As has already been described in section 7.3.2.2, the user can imitate the control parameters of his machine as close to reality as possible, using the unit 35 SH 94.

The assembly positions 01 to 23 (Z–X, Z–c, Z–e and d–e) are available, for channel 1, the assembly positions 51 to 73 (Z–X, Z–c, Z–e and d–e) for channel 2. The solder tags are connected to each other.

The fine adjustment of the parameters is carried out with the potentiometers R3 and R7 (channel 1) or R4 and R8 (channel 2).

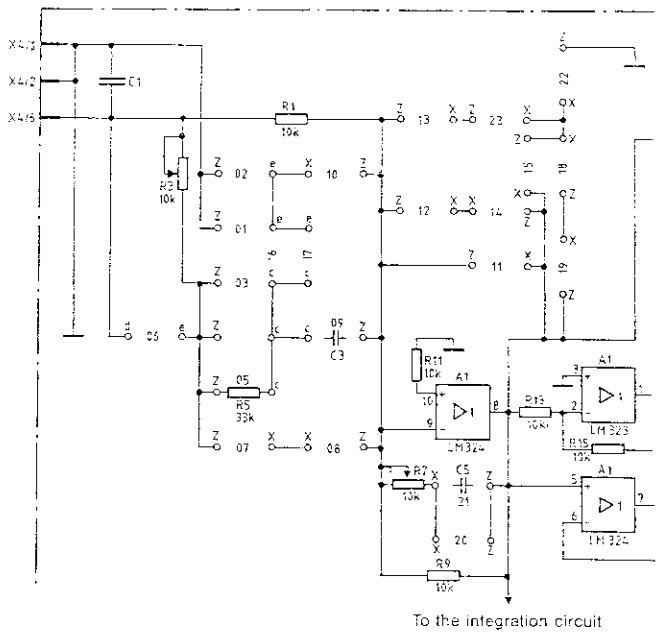


Fig. 19.3–4 Circuitry of the assembly positions 01 to 23 (for setting the control parameters for channel 1).

Note: The codes of the assembly positions for channel 2 are each higher than for channel 1 by the numerical value 50, i.e. within the values 51 ... 73.

20 System cables

35 SK 93 R1:	Connection cable for RS422 interface,	length 5 m.
35 SK 93 R11:	Extension cable for the system cable 35 SK 93 R1.	length 5 m.
35 SK 94 R2	Connection cable for RS232 interface,	length 5 m.
35 SK 95 R1	Connection cable for RS232 interface,	length 0.25 m.
35 SK 97 R1	Extension cable for the system cable 35 SK 94,	length 3 m.

20.1 Connection cable 35 SK 93 R1 ..... 20.1- 1

20.1.1 Technical data 20.1- 1

20.2 Extension cable 35 SK 93 R11 ..... 20.2- 1

20.2.1 Technical data 20.2- 1

20.3 Connection cable 35 SK 94 R2 ..... 20.3- 1

20.3.1 Technical data 20.3- 1

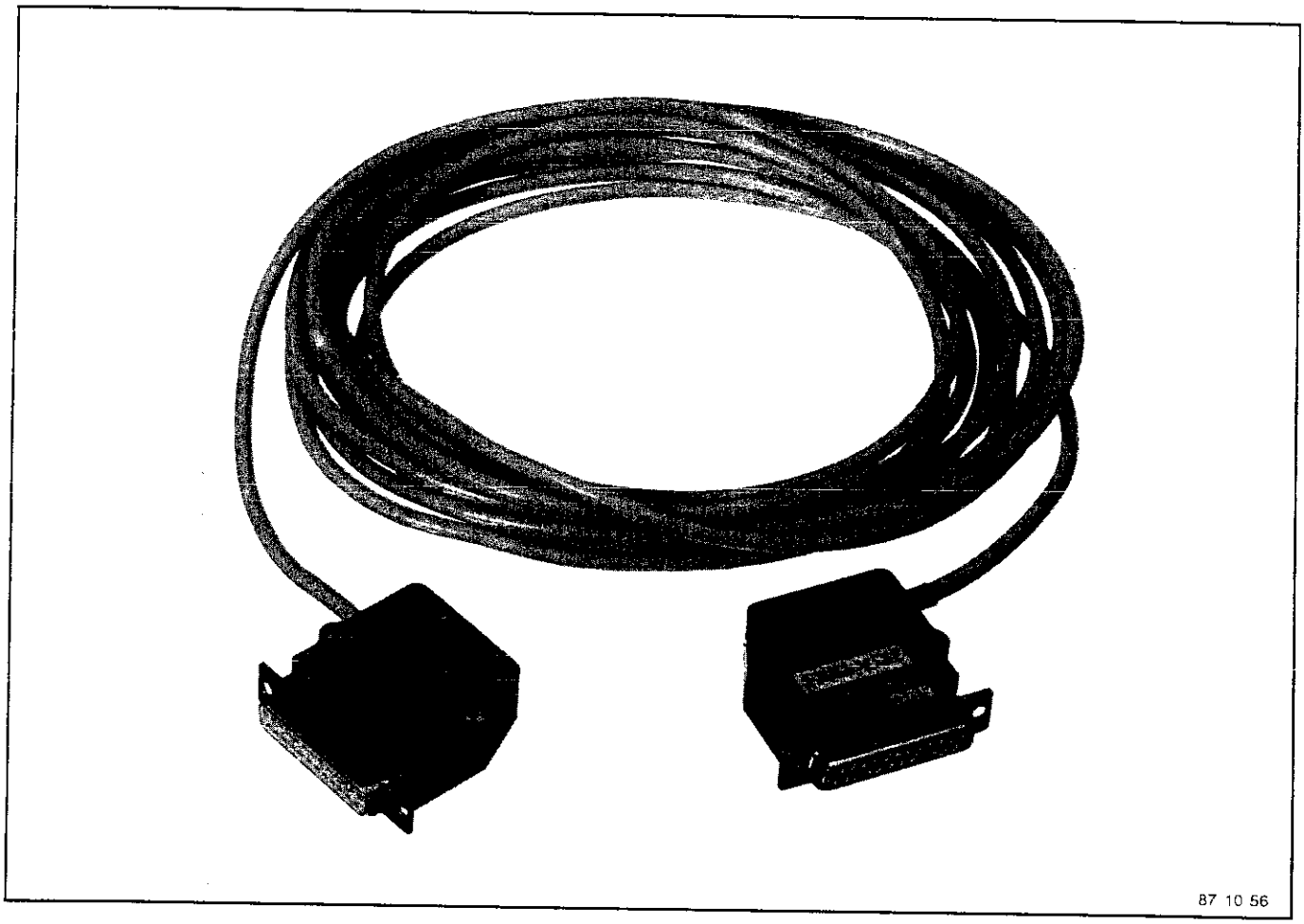
20.4 Extension cable 35 SK 95 R1 ..... 20.4- 1

20.4.1 Technical data 20.4- 1

21.5 Connection cable 35 SK 97 R1 ..... 20.5- 1

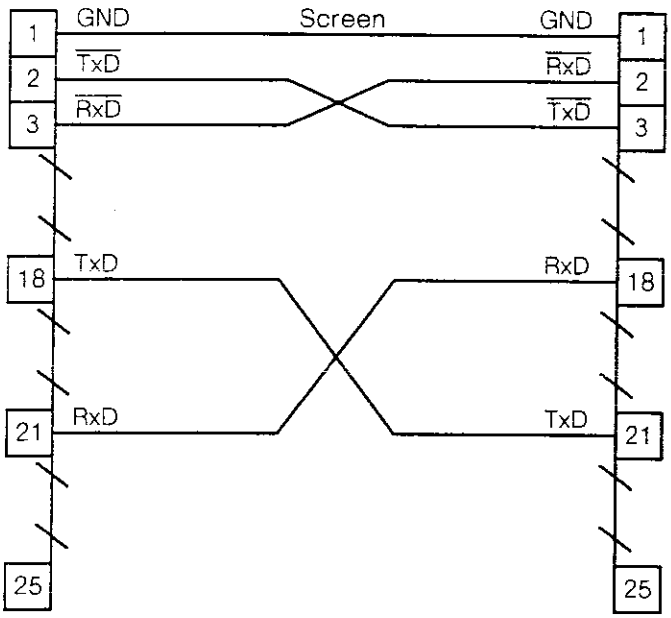
21.5.1 Technical data 20.5- 1

20.1 Connection cable 35 SK 93 R1



20.1.1 Technical data

Purpose of use	Connection cable for serial RS422 interfaces
Structure	25-polar D subminiature sockets at both ends
Length	5 m
Weight	0.4 kg
Order number	GJR5135400R1



20.1-1 Connection diagram of the 35 SK 93 R1

20.2 Extension cable 35 SK 93 R11

20.2.1 Technical data

Purpose of use	Extension cable for 35 SK 93 R1
Structure	25-polar D subminiature socket and plug
Length	5 m
Weight	0.4 kg
Order number	GJR5135400R11

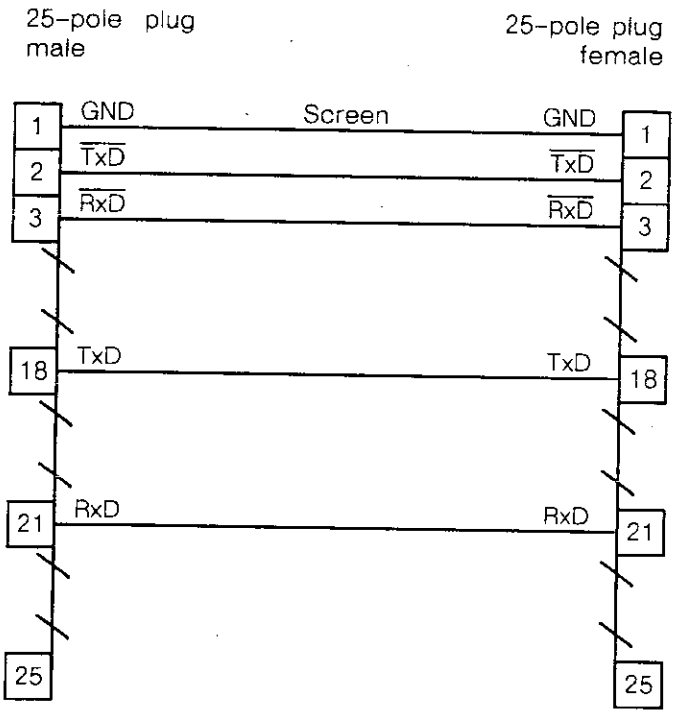
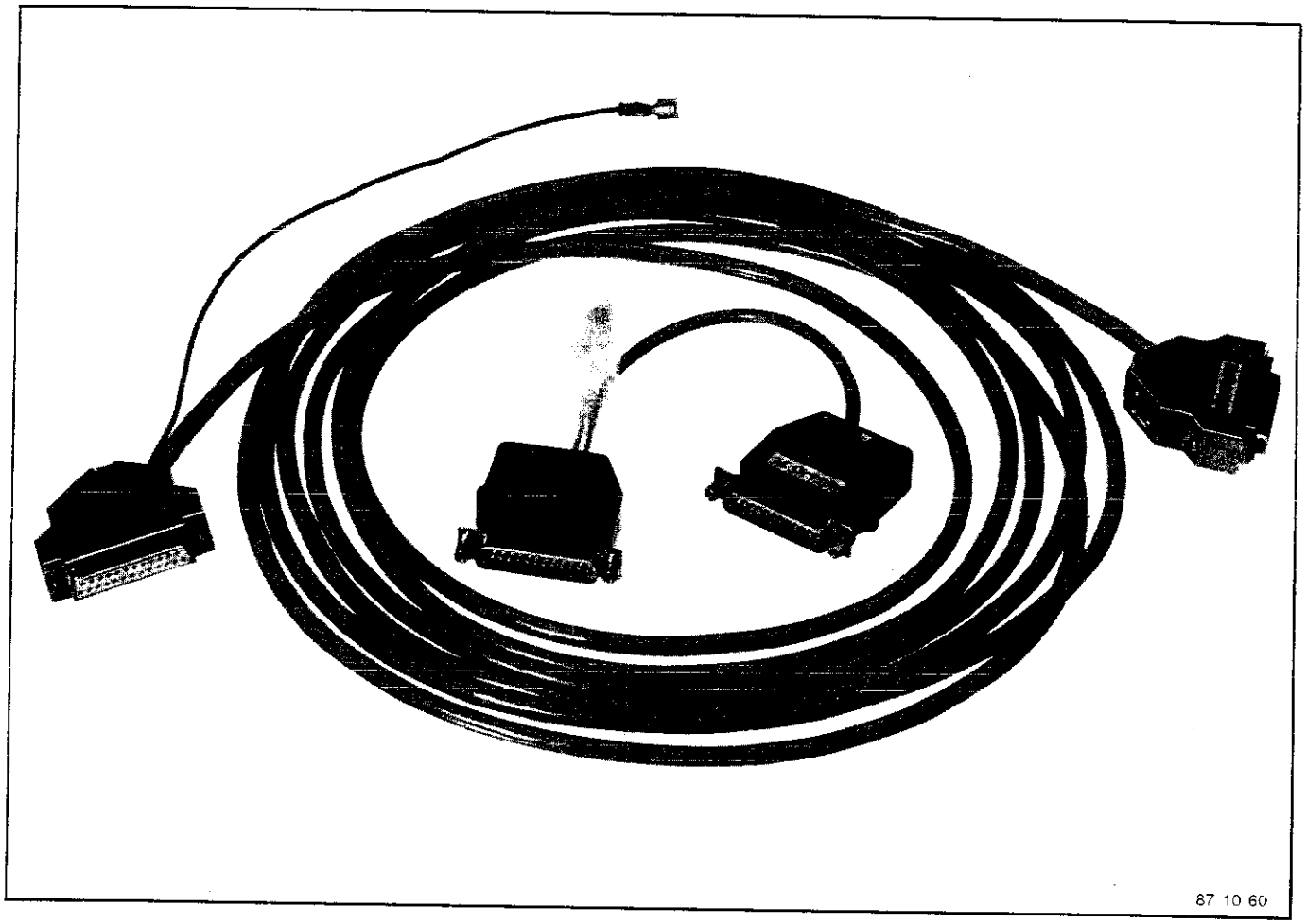


Fig. 20.2-1 Connection diagram for the 35 SK 93 R11

20.3 Connection cable 35 SK 94 R1,R2,R3 and R4



20.3.1 Technical data

Purpose of use	Connection cable for serial RS232 interfaces (Connecting the data interface 35 DS 91 to the programming unit)
Structure	25-polar D subminiature sockets at both ends. Additional cable with a length of 0.3 m and a faston connection 6.3 mm at one end. The connections 6, 8 and 20 are bridged at both ends. Shielded socket casing made from plastic coated with metal.
Length	Rubric 1 2,5 m * Rubric 2 5.0 m # Rubric 3 10.0 m * Rubric 4 20.5 m *

* Not ex fabric, prices and delivery times upon request.
# Extension cable for R2 is 35 SK 95

Weight	0.4 kg
Order number	GJR2370500R2

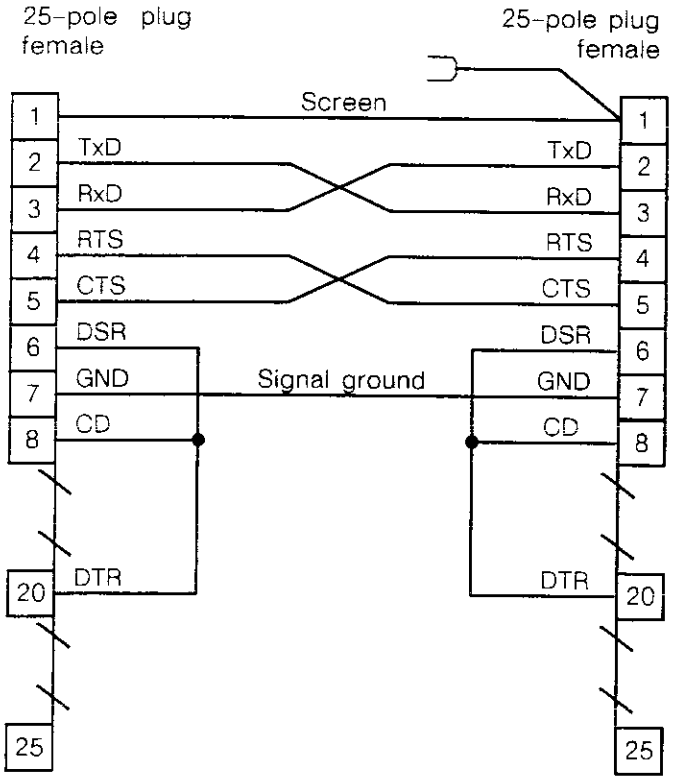


Fig. 20.3-1 Connection diagram for the 35 SK 94 R2

20.4 Extension cable 35 SK 95 R1

(See 20.3, Connection cable 35 SK 94 for the photograph)

13.4.1 Technical data

Purpose of use	Extension cable for 35 SK 94 R2
Structure	25-polar D subminiature plugs at both ends The connections 6,8 and 20 are bridged at both ends. Shielded socket casing made from plastic coated with metal.
Length	0.25 m
Weight	0.15 kg
Order number	GJR2371000R1

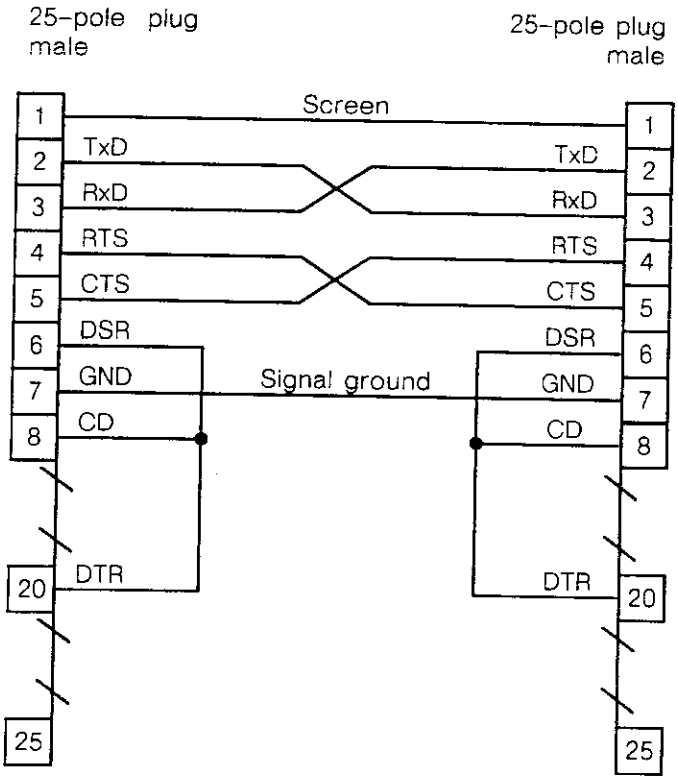
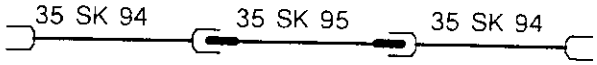
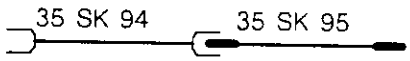


Fig. 20.4-1 Connection diagramm for the 35 SK 95 R1

a. Extension cable for 35 SK 94 R2



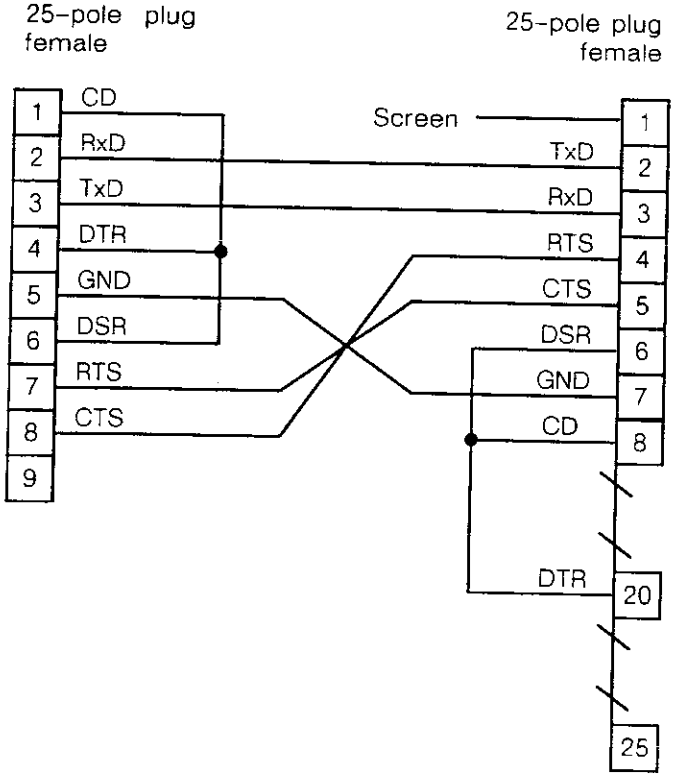
b. As supplement for 35 SK 94 R2, if a cables needed with a female plug at the one end and a male plug on the other end.



20.5 Connection cable 35 SK 97 R1

20.5.1 Technical data

Purpose of use	Connection cable for serial RS232 interfaces (Connecting the data interface 35 DC 90/91 to the programming unit)
Structure	9-polar D subminiature socket on the connection side for the programming unit; 25-polar D subminiature socket on the connection side for the data interfaces. The connections are soldered, the shielded socket casing made from plastic coated with metal is screwed down.
Length	Type of cable: LiYCY 5 x 0.14/15 3.0 m
Weight	0.3 kg
Order number	GJV3073902R1



Socket assignment

Pin	Signal name	Pin	Signal name	Colour code	Note
X1.1	CD	X2.6	DSR	Black	Bridges in plug X1 and X2
X1.4	DTR	X2.8	CD	Black	
X1.6	DSR	X2.20	DTR	Black	
		X2.1	Screen	White	
X1.2	RxD	X2.2	TxD	Green	
X1.3	TxD	X2.3	RxD	Brown	
X1.5	GND	X2.7	GND	Yellow	
X1.7	RTS	X2.5	CTS	Grey	
X1.8	CTS	X2.4	RTS	White	

Note: The 25-polar plug is bridged between the connections 6, 8 and 20.

Fig.20.5-1 Connection diagram for the 35 SK 97

21 Accessories

35 FB 90 R1	Dummy cover
35 ST 90 R1	Front plug
35 SB 90 R*	Label strip
07 LB 20 R1	Lithium battery
35 LE 90 R1	Lithium battery module

21.1 Dummy cover 35 FB 90 R1 ..... 21.1- 1
21.1.1 Technical data 21.1- 2
21.1.2 Description 21.1- 2

21.2 Front plug 35 ST 90 R1 ..... 21.2- 1
21.1.1 Technical data 21.2- 2
21.1.2 Description 21.2- 2
21.2.3 Mechanical structure 21.2- 3

21.3 Label strips 35 SB 90 ..... 21.3- 1
21.3.1 Technical data 21.3- 2
21.3.2 Description 21.3- 2

21.4 Lithium battery 07 LB 20 R1 ..... 21.4- 1
21.4.1 Technical data 21.4- 1
21.4.2 Description 21.4- 2
21.4.3 Handling the battery 21.4- 2

21.5 Lithium battery module 35 LE 90 R1 ..... 21.5- 1
21.5.1 Technical data 21.5- 1
21.5.2 Description 21.5- 2
21.5.3 Handling the battery module .. 21.5- 2

21.1 Dummy cover 35 FB 90 R1

90 01 86

21.1.1 Technical data

Dimensions	261.5 mm x 20 mm
Weight	approx. 0.030 kg
Order number	GJR5135200R1

Note:
The required fixing screws with toothed washers are included in the delivery scope.

21.1.2 Description

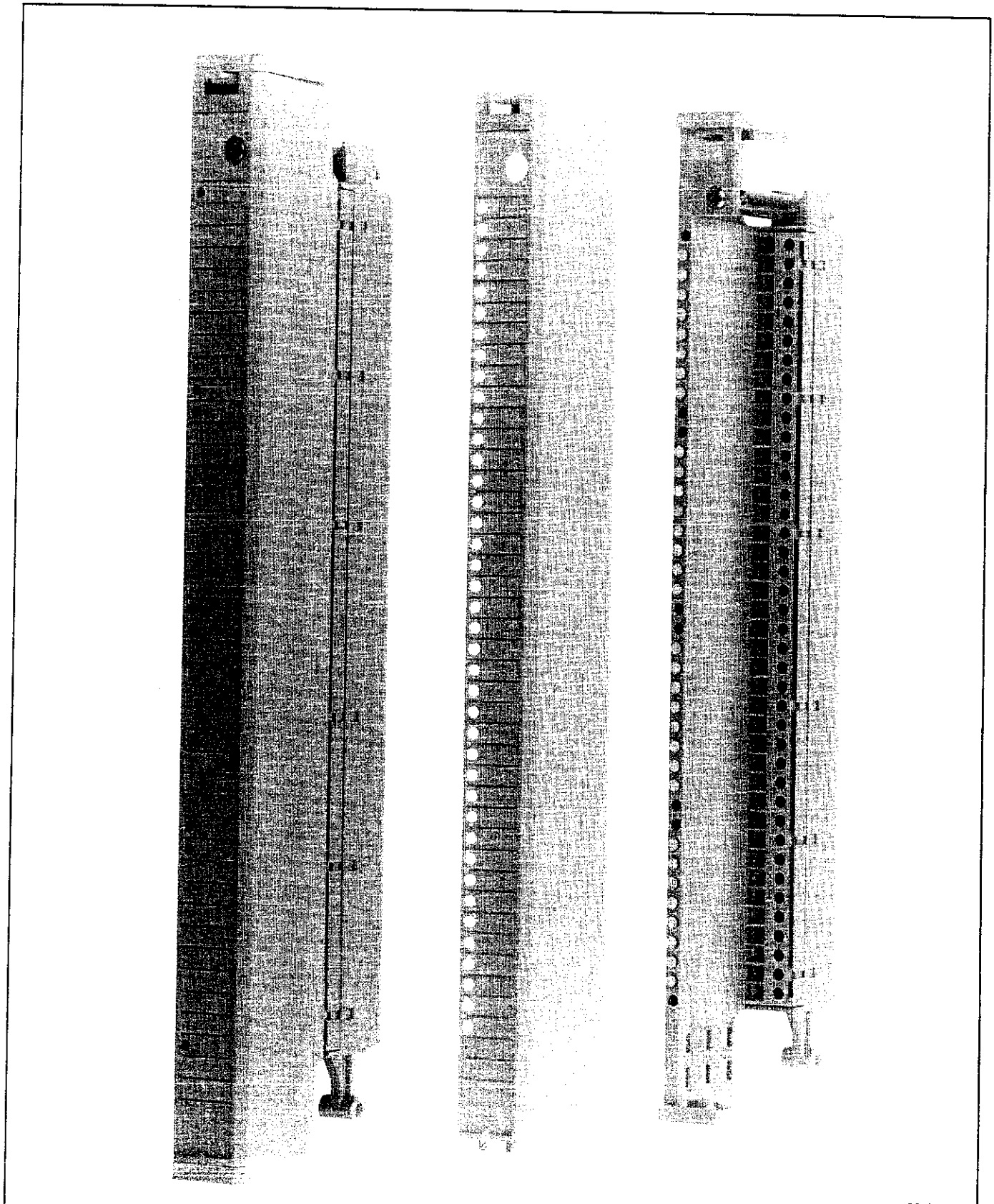
The 35 FB 90 dummy cover serves to cover free plug positions of a subrack. The bus bar and the socket strip located on the bus bar are both protected from contamination in this way.

One dummy cover is required for each free plug position.

Assembly example:

5 plug positions of a total of 21 plug positions of a subrack are used for a power supply unit 35 NE 90. It is assumed that 12 ABB Procontic T300 single components are required. 4 dummy covers 35 FB 90 are therefore required to cover the free plug positions 21 – 17.

21.2 Front plug 35 ST 90 R1



90 06 89

21.2.1 Technical data

Pole number	40
Connection grid	5.08 mm
Current loadability	
at +70°C	4 A
at +20°C	5.5 A
Permitted operating voltage	$\leq$ 250 V
Volume resistance	$\leq$ 15 mOhm
Insulation resistance	$\geq 10^{11}$ Ohm
Test voltage	
Contact/mass	2.5 kV
Contact/contact	1.55 kV
Plug and disconnect forces	$\leq$ 100 N
Mechanical lifetime	50 plug cycles
Permitted ambient temperature	-55°C to + 125°C
Humidity rating	F
Order number	GJR5144900R1

Accessories:

Label strip 35 SB 90 for 35 ST 90 with 9 insertion strips and 9 sticky strips each for

Unit	**Order number**
35 EB 91 R1 (35 SB 90 R1)	GJR5144600R1
35 EB 91 R2 (35 SB 90 R2)	GJR5144600R2
35 EB 92 R1 (35 SB 90 R3)	GJR5144600R3
35 EB 92 R2 (35 SB 90 R4)	GJR5144600R4
35 AB 94 R1 (35 SB 90 R5)	GJR5144600R5
35 AB 95 R1 (35 SB 90 R6)	GJR5144600R6
35 AB 96 R1 (35 SB 90 R7)	GJR5144600R7
35 AB 97 R1 (35 SB 90 R8	GJR5144600R8

21.2.2 Description

The front plug 35 ST 90 is required to connect I/O cards of the ABB Procontic T300 with periphery subassemblies.

The front plug is equipped with 40 connection possibilities for a cable with a maximum cross-section of 1.5 mm².

The following can be connected:

approx. 40 x 1.0 mm²
or approx. 27 x 1.5 mm²
or approx. 36 x 0.75 mm² and 4 x 1.5 mm²
or approx. 34 x 0.75 mm² and 6 x 1.5 mm²

Wire cross-section	Wire end ferrule
0.75 mm² 1.0 mm²	0.75 - 10 1.0 - 10 or 1.0 -12
Single core	Stripped length
1.5 mm²	10 - 12 mm

The plug connector of the front plug is premounted on the respective I/O card by the factory.

The socket connector of the front plug 35 ST 90 can be prefabricated by the user. It is generally only mounted on the corresponding I/O unit, when it is to be taken into use.

The socket connector contacts the plug connector with the center of rotation at the bottom. A leading contact of the frame contact (connection 40) is achieved in this way.

21.2.3 Mechanical structure

Assembly width	20.32 mm
Fixing method	Fixing screws
Contact material:	
Plug	Cu Zn 37F45
Socket	Cu Sn 6
Contact surface:	
Plug	Nickel coated with galvanic zinc
Socket	Coated with galvanic zinc
Insulation material	Thermoplast reinforced with glass fibres Colour RAL 7032, flame resistant UL94V-0
Type of connection:	
Plug connector	Flat plug sleeve 2.4 x 0.8
Socket connector	Screw connection TOP 1.5

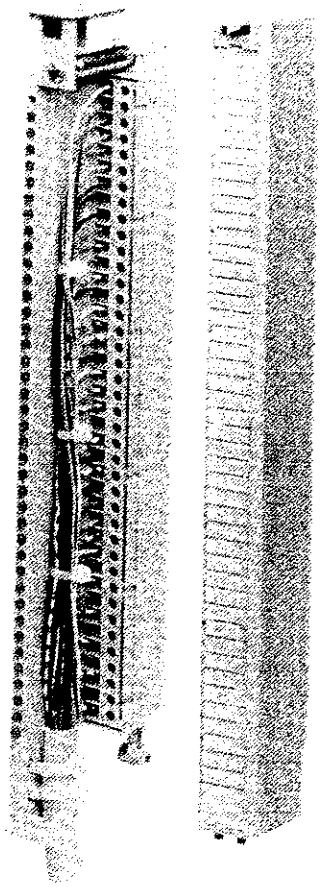


Fig. 21.2-1 Example of the wiring of the 35 ST 90

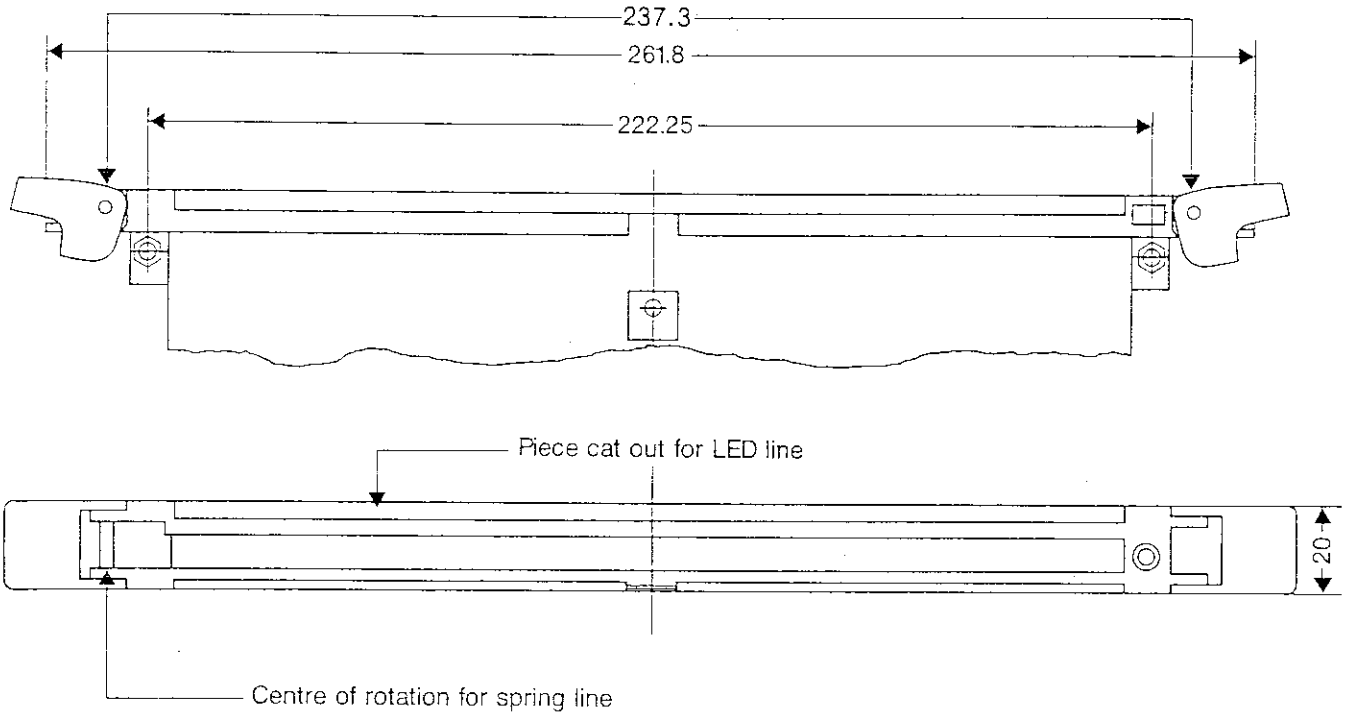


Fig. 21.2.-2 View and dimension of the socket connector

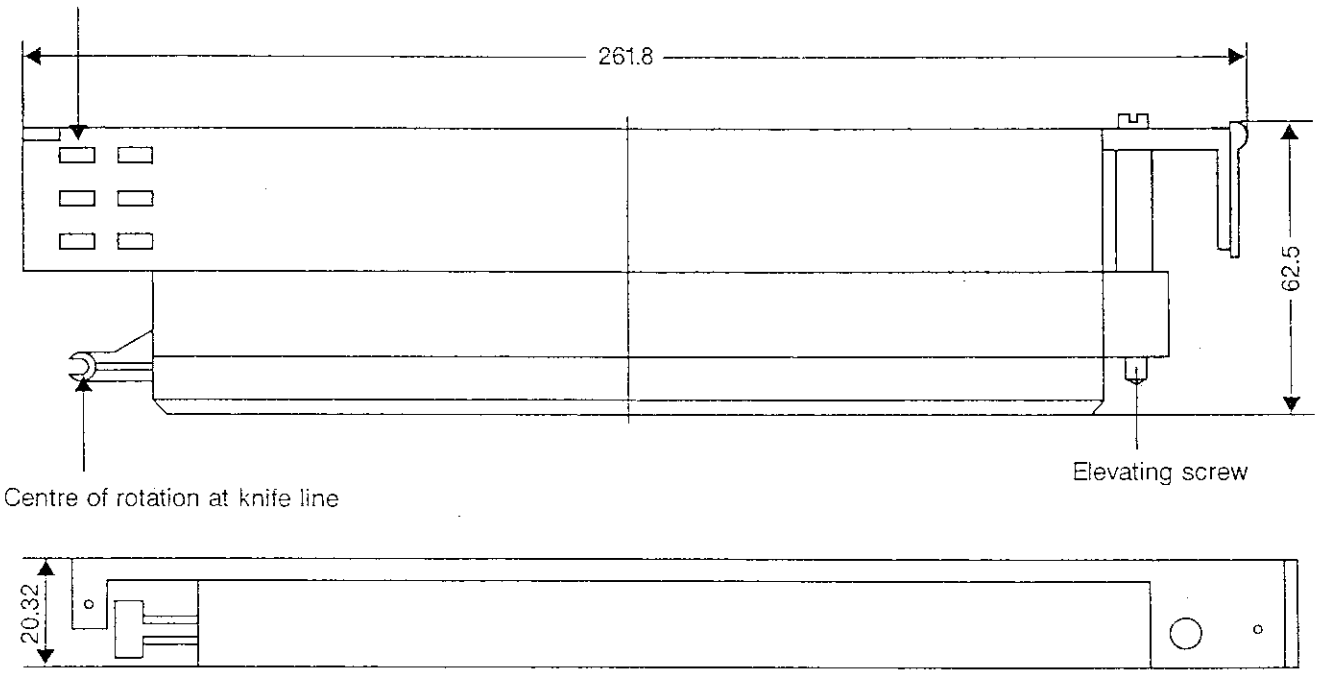
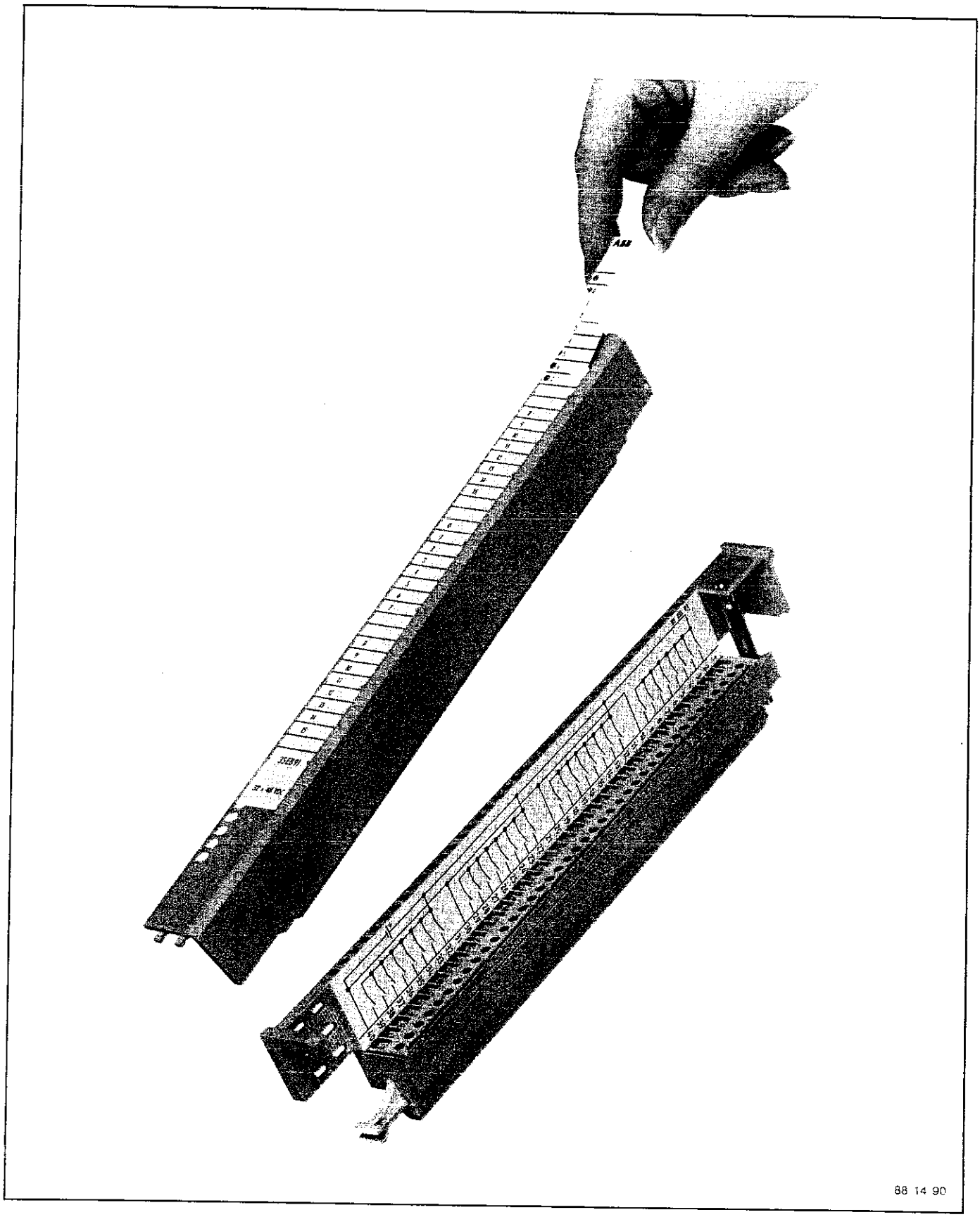


Fig. 21.2-3 View and dimensions of the plug connector

21.3 Label strip 35 SB 90



88 14 90

21.3.1 Technical data

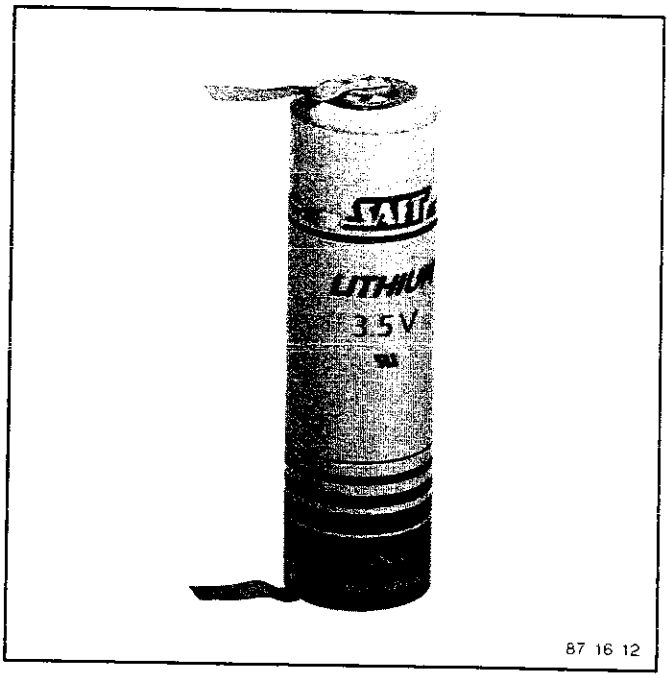
Label strip for 35 ST 90 with 9 insert strips and 9 sticky strips each for

Unit	Order number
35 EB 91 R1	GJR5144600R1
35 EB 91 R2	GJR5144600R2
35 EB 92 R1	GJR5144600R3
35 EB 92 R2	GJR5144600R4
35 AB 94 R1	GJR5144600R5
35 AB 95 R1	GJR5144600R6
35 AB 96 R1	GJR5144600R7
35 AB 97 R1	GJR5144600R8

21.3.2 Description

If there is a connection with periphery units via the front plug 35 ST 90, a label set 35 SB 90 can be ordered. It consists of insert strips and sticky strips.

21.4 Lithium battery 07 LB 20 R1



21.4.1 Technical data

Storage temperature	– 50 ... + 75 °C (note the self-discharge)
Ambient temperature when in operation	– 50 ... + 75 °C (note storage and transport information)
Background voltage	3.7 V
Nominal voltage	3.6 V / IL = 1 mA
Nominal voltage independent of the temperature	approx. – 1 mV/°K
Capacity independent of the temperature (I = 10 mA)	approx. – 10 % with T = 75 °C approx. – 15 % with T = 0 °C approx. – 5 % with T = – 40 °C
Self-discharge	approx. 50 % with T = 40 °C, storage time 1.5 years
Order number	GJR5223500R1

21.4.2 Description

The lithium battery serves to maintain RAM information for the corresponding unit (e.g., 35 DS 91, 35 ZE 93, 35 PS 91 etc.), if the respective unit is no longer supplied by the system.

21.4.3 Handling the battery

1 Only use batteries tested by ABB and avoid short-circuits, since these destroy the batteries.

2 Assembly: Sold in the battery (see point 4).

3 Changing the battery: The battery may only be assembled or dismantled with the supply voltage switched on in order to avoid any data loss.

4 Only for the battery change
Soldering the battery in and out may only be carried out with an electrically isolated soldering station. The soldering should take place with the voltage connected, if this is possible, since the memory contents of the RAMs are otherwise lost or the diode circuited in series will be destroyed.

Soldering out the battery: first solder out the positive pole and then the negative pole.

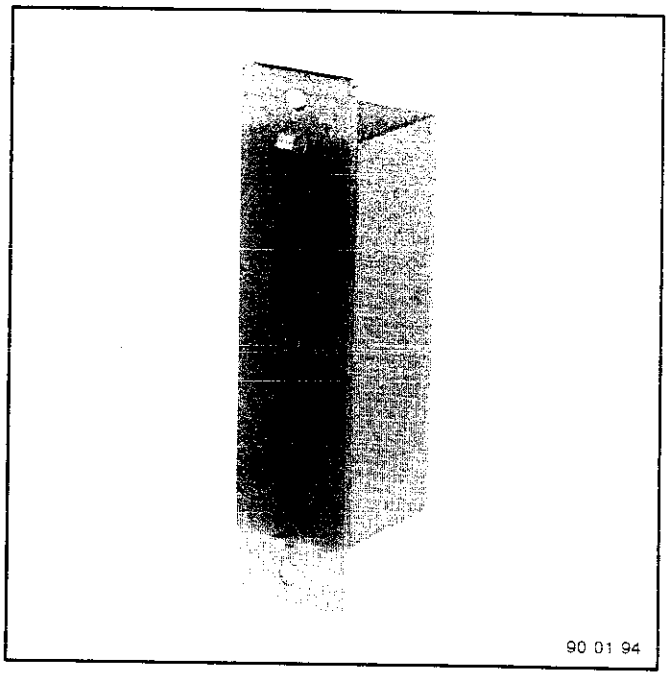
Soldering in the battery: first solder in the negative pole and then the positive pole.

Note: The corresponding environmental protection conditions are to be observed when changing the batteries!

5 Battery test: The voltage of the lithium battery may not sink below 2.9 V during 5 s with a load of 3.9 KΩ.

6 Battery lifetime: 1 year (assembled with mains voltage), 3 months (assembled without mains voltage).

21.5 Lithium battery module 35 LE 90 R1



21.5.1 Technical data

Storage temperature	– 50 ... + 75 °C (note the self-discharge)
Ambient temperature when in operation	– 50 ... + 75 °C (note the storage and transport information)
Background voltage	3.7 V
Nominal voltage	3.6 V / IL = 1 mA
Nominal voltage independent of the temperature	approx. – 1 mV/°K
Capacity independent of the temperature (I = 10 mA)	approx. – 10 % with T = 75 °C approx. – 15 % with T = 0 °C approx. – 5 % with T = – 40 °C
Self-discharge	approx. 50 % with T = 40 °C, storage time 1.5 years
Order number	GJR5146300R1
Accessories	
Lithium battery 07 LB 20 R1	GJR5223500R1

21.5.2 Description

The lithium battery module 35 LE 90 R1 serves to maintain RAM information for the corresponding units (e.g., 35 DS 91, 35 ZE 93, 35 PS 91 etc.), if the respective unit is no longer supplied by the system.

21.5.3 Handling the battery module

1 Use only lithium battery modules tested by ABB and avoid short-circuits, since these destroy the batteries.

2 Assembly: Completely insert the lithium battery module on the front panel (positive pole at the top), fix it with the supplied screws M3x6 and the spring washers.

3 Changing the lithium battery module: The lithium battery module may only be assembled and dismantled with the supply voltage switched on in order to avoid any loss of data.

4 Changing the lithium battery: Change the lithium battery in the dismantled lithium battery module.

Soldering the battery in and out may only be carried out with an electrically isolated soldering station, else the diode circuited in series will be destroyed.

Soldering the battery out: First solder out the positive pole and then the negative pole.

Soldering the battery in: First solder in the negative pole and then the postive pole.

Note: The corresponding environmental protection conditions are to be noted for changing the batteries!

5 Battery test: The voltage of the lithium battery may not sink below 2.9 V during 5 s with a load of 3.9 $K\Omega$.

6 Battery lifetime: 1 year (assembled with mains voltage), 3 months (assembled without mains voltage).

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